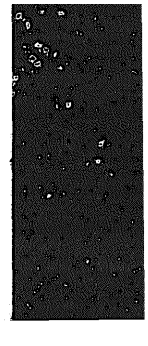
TM 11-7010-200-10-3-1

TECHNICAL MANUAL

OPERATION AND MAINTENANCE INSTRUCTIONS

OPTICAL CHARACTER READING SYSTEM
RP/GYX
AN/UYQ ( )

HEADQUARTERS, DEPARTMENT OF THE ARMY
NOVEMBER 1979



TM 11-7010-200-10-3-1

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 30 November 1979

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By Order of the Secretary of the Army

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NG: NONE

USAR: NONE

For explanation of abbreviations see, AR 310-50.

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INTRODUCTION

1. GENERAL. - The information contained in this manual describes the Optical Character Reader RP238/GYX, manufactured under contract number DAAB03-75-C-0619.

2. SCOPE AND PURPOSE OF MANUAL. - This manual contains all information necessary for the installation, operation, maintenance, adjustment, and repair of the equipment. The contents of chapters 1 through 7 are described below. The appendix to the manual contains the logic, schematic and wiring diagrams, and the reference photographs.

Chapter 1. Description of Equipment. - This chapter provides a general description of the equipment, its security classification, and its characteristics,

Chapter 2. Installation.- This chapter contains installation procedures for the equipment, The installation procedures include installation planning, logistics, step-by-step procedures for initial checkout, and preparation for reshipment.

Chapter 3. Operating Instructions. - This chapter contains information required to operate the equipment, including a description of the operating controls, indicators and error messages, and operating instructions.

Chapter 4. Principles of Operation, - This chapter provides the functional system operation and the functional operation of electronic circuits in the order of signal

flow. The principles of operation of mechanical assemblies are also described.

Chapter 5. Preventative Maintenance. - This chapter provides all the necessary preventive maintenance procedures that should be performed to prevent major equipment failures, Included in this chapter are preventive maintenance schedules, instructions for minor parts replacement, and minor adjustments and

Chapter 6. Corrective Maintenance. - This chapter contains instructions for locating and correcting faults in the equipment.

Illustrated Parts Breakdown. - This manual contains no Illustrated Parts Breakdown. All data relative to Figures 7-1 through 7-35 referred to in this publication will be found in T.O. 31S5-4 516-4 and are listed as figures 1 through 35.

3. RELATED PUBLICATIONS. - The following is a list of documents used in the preparation of this manual.

MILITARY STANDADS:

MIL-STD-12	Abbreviations for Use on Drawings and in Technical-Type Publications.
MIL-STD-15	Electrical and Electronic Symbols.
MIL-STD-188	Military Communication System, Technical Standards.
MIL-STD-806	Graphic Symbols for Logic Diagrams,

HANDBOOKS:

H4-1	Federal Code to Manufacturers (Name to Code)
H4-2	Federal Code to Manufacturers (Code to Name)

H6-1	Federal Item Identification Guide for Supply Cataloging.

AMERICAN ASSOCIATION STANDARDS:

USAY32.16-1965	Electrical and Electronic Reference Designations.

CHAPTER 1

DESCRIPTION OF EQUIPMENT

1-1. SECURITY CLASSIFICATION. The Optical Character Reader RP238/GYX, hereafter referred to as the ALPHA, including all its assemblies and subassemblies, is unclassified.

1-2. PURPOSE OF EQUIPMENT. - The ALPHA (Figure 1-1) is a high speed optical character scanner capable of reading 80 characters per second and converting this input into machine language, The scanned characters are outputted in the data codes normally required in telecommunications. ALPHA reads separate sheets up to 11 inches wide in OCR-A and OCR-B fonts, Its minimum error rate is less than one in 25,000 characters and can be much higher depending upon the quality of the input material.

1-3. PHYSICAL DESCRIPTION OF EQUIPMENT. - The Optical Character Reader RP238/GYX is completely contained in a single cabinet, 46 inches in height, 28 inches wide, and 28 inches deep; total weight is approximately 400 pounds. (The cabinet is mounted on four casters which allow it to move easily.) The Read Head, Keyboard, Page Feeder, and Control Panels are located in the control console assembly at the top of the unit. The Read Head, Keyboard, and Panels are mounted in the hinged console which when opened exposes the paper drive rollers and the back of the Page Feeder. The base of the cabinet contains all of the electronic components in the system, which consists of the power supplies, microprocessor, external memory, and the interface.

The Operator controls are mounted in two panels, one on each side of the Keyboard. In addition, a separate test panel, mounted on the interior of the cabinet, contains the controls necessary to test and exercise the equipment for diagnostic purposes.

The cabling connections (power and data) to the unit are located at the lower rear section of the cabinet on a single panel. Two conduit elbows are provided, one each for the power and data cables. Connections are made to terminal blocks on the interior of the cabinet. A convenience receptable is also located on the power input panel for auxiliary external equipment. Fusing for the main AC input and convenience receptacles is located adjacent to the power input cable and convenience receptacle.

All of the circuits in the ALPHA are shown in Figures A-1 through A-33. The major assemblies of ALPHA are identified in Figures A-34 through A-41. Figures A-34 and A-35 illustrate externally identifiable features and major assemblies. Figure A-36 shows major internal assemblies as seen from the left side with the sheet metal enclosure removed. The location of paper control assemblies 1A7 and 1A5, as seen from inside, is clearly identified; paper control assemblies 1A7 and 1A5 are shown separately in Figure A-37. Circuit cards located in the control console are identified in Figure A-38. Figures A-39 and A-40 show the location of logic cards and the transformer in the lower portion of ALPHA. Figure A-41 shows how to access the upper assemblies,

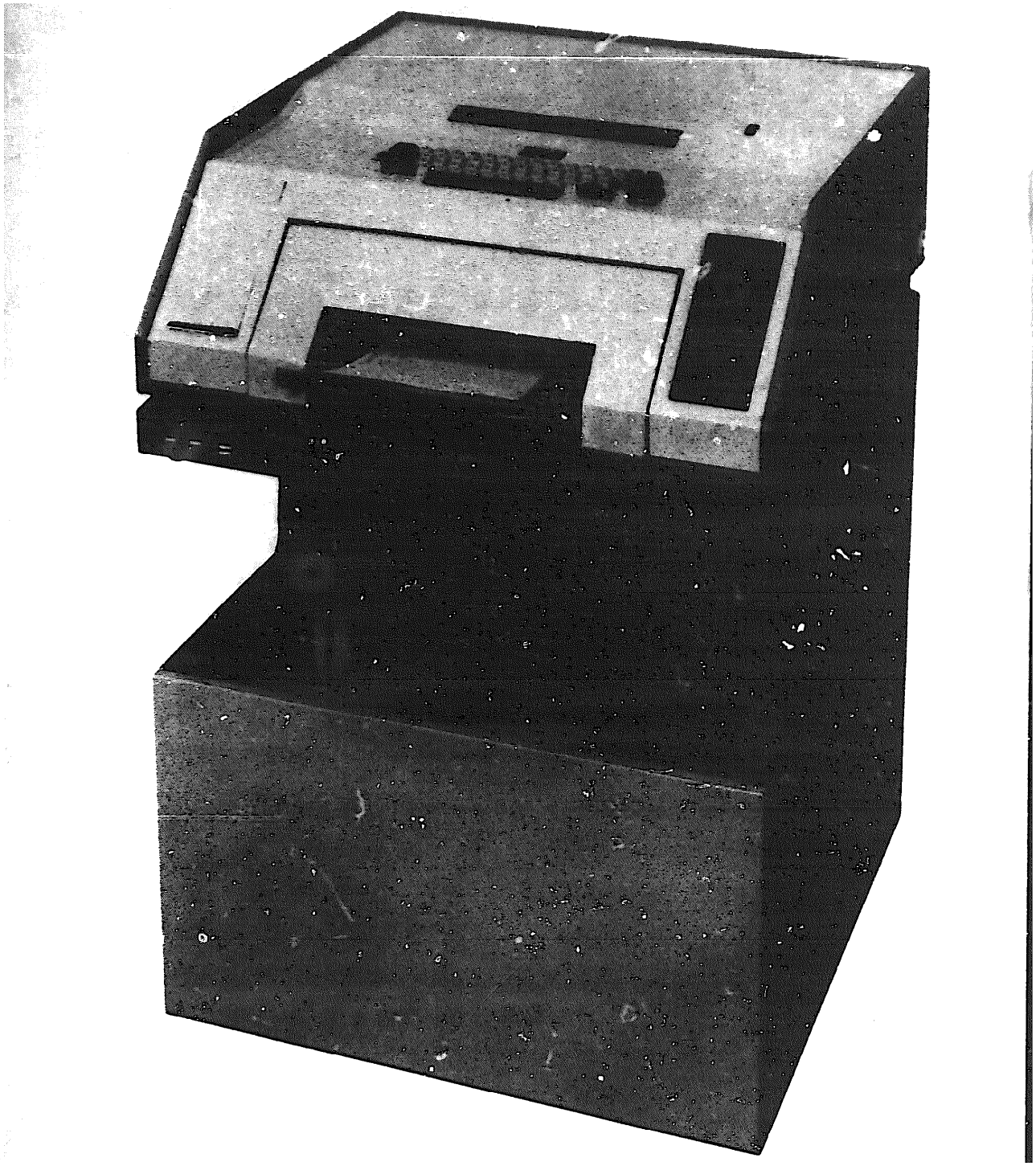


Figure 1-1. - Optical Character Reader RP238/GYX (ALPHA)

a. Cabinet. - The ALPHA is housed in a cabinet whose overall dimensions are shown in Figure 2-2 and the weight listed in Table 1-1. The cabinet assembly consists of a hinged top cover, a steel outer skin, and a tubular steel inner frame. Internal structural members are welded to the frame to support heavier subassemblies.

(1) Cabinet Access. - Cabinet access is gained through two hinged panels, one (27 inches wide and 25 inches high) at the rear and a smaller one (28 inches wide and 17 inches high) at the front. The top Control Console Assembly is hinged and allows complete access to the two components mounted to the top of the frame.

(2) Finish. - The entire Cabinet Assembly is primed with zinc chromate primer (83-T-3). The base (skin and frame) is then painted black (89-T-38). The Control Console Assembly is painted two tone; gold (TK23397) at the sides, and white (TK20416) at the top in the area of the operator controls.

b. Major Assemblies.- The integrated Power Supply Assembly (1A1) is mounted to the base of the tubular frame. Behind the rear hinged access door is the vertically mounted, hinged wire-wrap board containing all of the microprocessor circuits. A printed circuit card cage is mounted to the board. The External Memory Assembly (1A4) is mounted on a hinged panel behind the lower removable front panel. The Control Console Assembly (1A6) contains the keyboard and control panels.

When this assembly is raised, it exposes the Read Head and Paper Drive Assembly (1A7). The Page Feeder Assembly (1A5) is located at the top of the main frame in a slot in the control console. (See Figure A-34.)

(1) Power Supply Assembly (1A1). - The Power Supply Assembly consists of four (4) individual power supplies (+5, -9, -12, +12) on a single integrated chassis. A vertically mounted test card monitors the various supplies and "senses" failures. Additional protective circuits and tooting fans are also mounted on this chassis.

CAUTION. - Care should be exercised when metal tools are used near the capacitor bank on the power supply. The capacitors in the bank store Low voltage-high current. Damage may result if any metal is shorted across the capacitors.

(2) Main Wire Wrap Board (1A3). - The main wire wrap board is vertically mounted and contains all of the micro-processor Integrated Circuits (IC) In addition, a card cage is mounted perpendicular to the main board and holds all of the printed circuit plug-in cards. Signal connections between the main board and other circuits are accomplished through ribbon cable assemblies.

(3) Read Head and Paper Drive Assembly (1A7). - The Read Head and Paper Drive Assembly is the heaviest component in the ALPHA. It is supported by a solid steel support welded

to the main frame. All of the components related to movement of the Read Head and paper movement are mounted on the assembly. Also, the mirror viewing system is mounted on the Paper Drive Assembly.

(4) Page Feeder Assembly (1A5). - The Page Feeder Assembly is mounted on top of the main frame and fits into a recess in the top Control Console Assembly. A single knurled screw secures the assembly in place. All electrical connections are made via a single connector mounted at the rear of the unit which mates with a suitable receptable on the main frame. The Page Feeder Assembly is completely self-contained, requiring only external power and signal commands.

(5) Control Console Assembly (1A6). - The Control Console Assembly contains the keyboard, LED display, and both the control and format panels. Each of these components, except the control panel, is immediately accessible through the console. The format panel is covered by a hinged panel. The Control Console Assembly is hinged at the rear, spring counter-balanced, and swings up like a clam shell. This allows access to all moving parts of the Read Head and Paper Drive Assembly and the format and control panel printed circuit cards which are mounted to the console.

(6) External Memory Assembly (1A4). - The External Memory Assembly is assembled on a single vertical board which is mounted on a hinged frame. The assembly is accessed through a removable panel at the lower front portion of the cabinet.

c. Viewing Window. A witwing window is located on the top surface of the top Control Console Assembly. The location of the window and internal mirror system allows the operator the greatest possible visual access to the scanned line. An adjustment is provided to manually position the viewing mirror.

1-4. EQUIPMENT FUNCTION -aLPHA is an optical recognition system which scans typed sheets and converts the text into a form that can be applied to numerous output devices such as an interface, computer, teletypewriters, etc. Refer to the system block diagram, Figure 1-2, while reading the functional description that follows:

The too sheet in the Page Feeder Tray is lifted by a vacuum assembly and moved to the Paper Handler Assembly through a series of rollers and belts. During this time, mechanical devices and electronic circuits are used to assure a single sheet feed. The page to be read is placed face up on the input platform and pushed into the slot, top edge first, where it is taken up by a pair of feed rollers driven by a Digital Servo. The page remains in the same plane throughout the time that it is in the machine and is ejected into a hopper at the rear after it has been read.

Upon being taken up by the feed rollers, the page advances until the Read Head senses the top edge of the paper. The Read Head is mounted on a lightweight carriage which rides on a pair. of transverse rails allowing the Read Head to scan from the left edge to the right edge of the page. The carriage is

driven by a second Digital Servo via flexible cables and carries a small lens, a 128 bit self-scan array of photodiodes, a small PC Card, and an illumination system consisting of a lamp and fiber optic assembly. The carriage can accelerate to its constant scanning speed in 1/2 inch of travel at an acceleration of 3 gs.

The Paper Handler positions the sheet so that the first line of the text is positioned under the scanning element (Read Head Assembly) which scans (reads) the first line of text character by character. The characters are identified by recognition circuits, then temporarily stored in a line buffer.

If there were any unrecognized or crossed out characters, the Read Head Carriage will stop moving and a pointer attached to it identifies the unrecognized or crossed out character; an LED (Light Emitting Diode) display will show the preceding, questionable, and following characters, and an alarm will sound. The ALPHA will then wait for the operator to take corrective action through the keyboard. Once this action is finished, the completed line is then transferred to the core memory module. Then it is code converted by the microprocessor and the output is sent to the external device serially.

ALPHA then reads the next line by moving the paper up until the next line is under the scanning element and then moving the Read Head across it. The process continues until end of page criteria has been met. When the scanning of a page is completed,

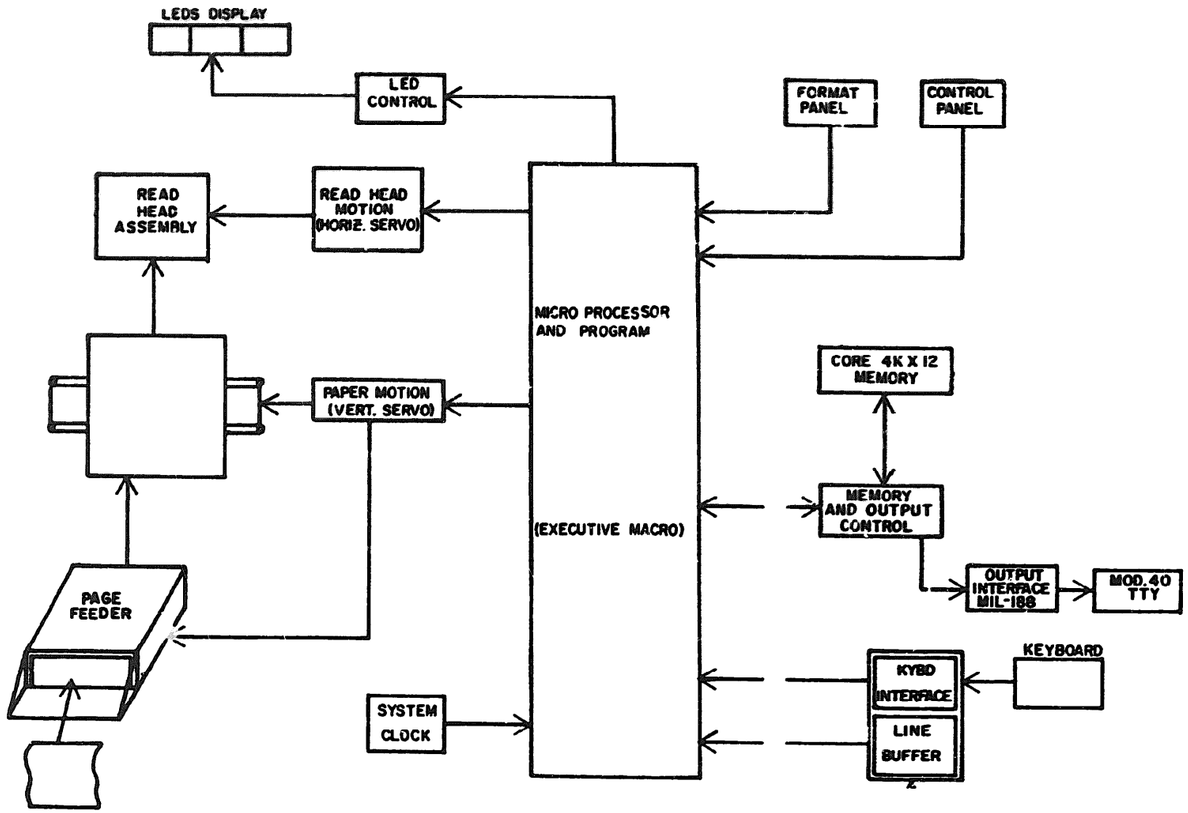


Figure 1-2. Simplified System Block Diagram

it is ejected and the Page Feeder then picks up the next sheet from the tray and forwards it to the Paper Handler section where the process is repeated.

When all the sheets in the Page Feeder Tray have been processed, ALPHA may be stopped by pressing STOP or RESET. If STOP or RESET is not pressed, the machine will automatically go into the Standby Mode after one minute.

1-5. **TECHNICAL CHARACTERISTICS.** - The technical characteristics of the Optical Character Reader RP238/GYX are listed in Table 1-1.

1-6. **EQUIPMENT SUPPLIED/REQUIRED BUT NOT SUPPLIED.** - The equipment supplied with the ALPHA is listed in Table 1-2. . The equipment required but not supplied is listed in Table 1-3. .

TABLE 1-1

Technical Characteristics

PHYSICAL CHARACTERISTICS	
Dimensions:	
Height.	46 inches (max.)
Width.	28 inches (max.)
Depth.	28 inches (max.)
Weight:	400 pounds
ELECTRICAL CHARACTERISTICS	
Power Requirements:	
Voltage.	115 ± 23 Vac. or 230 ± 48 Vac.
Current:	
Start.	7.5A @ 115 Vac.
	5.0A @ 230 Vac.
Operate.	4.0A @ 115 Vac.
	2.5A @ 230 Vac.
Power.	460 Watts
Frequency.	50 + 2.5 Hz or 60 + 3 Hz.
Phase.	Single
Signal Requirements (Inputs):	
Typewritten:	
Size.	5 in. wide X 7 in. long to 11 in. X 11 in., up to 50 sheets; 11 in. wide X 24 in. long, single sheets.

TABLE 1-1

Technical Characteristics (continued)

Variable values:	
Keyboard variable.	Values varied by use of keyboard.
Top margin.	00.5 inches from top of sheet to bottom margin minus 00.1 inches.
Left margin.	00.4 inches from left edge of sheet to right margin minus 00.1 inches.
Right margin.	Left margin plus 00.1 inches to 10.5 inches from left edge.
Bottom margin.	Top margin plus 00.1 inches to 25.1 inches from top of sheet.
Header sheet variable:	Values varied by use of header sheets.
End line.	1 to 120 blank spaces from last character.
Null line.	No character 00.1 to 6.3 inches from left margin.
Lines per inch.	6, 5, or 4.
Page end.	1 to 254 blank lines, from the line, at the spacing in use.
Keyboard:	Modified American Communications teletype; upper case and symbols only.

TABLE 1-1

Technical Characteristics (continued)

Clock:	
Amplitude.	+6V, -6V.
Frequencies.	75, 150, 300, 600, 1200, 1800, 2400, 7200, and 9600 Hz.
Signal Requirements (Outputs):	
Clock:	
Amplitude.	+6 to -6 (+/ - 1 volt) as per MIL-STD-188-100.
Asynchronous rate.	75, 150, 300, 600, 1200, 1800, 2400, 7200, 9600 Baud.
Isochronous rate.	Up to 128 Kilobit/Sec.
Data:	
Amplitude.	+6 to -6 (+/ - 1 volt).
Asynchronous.	75 to 9600 Baud.
Isochronous.	Up to 64 Kilobit/Sec.
Code.	5 to 8 level, 1 or 2 stop bits w/ / start bit.
Display:	Three 5 X 7 LED characters.
Tones:	800 Hz audible signal indicating a defective character in text and 400 Hz audible signal indicating a machine or text input error.

TABLE 1-1

Technical Characteristics (continued)

ENVIRONMENTAL CHARACTERISTICS	
Temperature:	
Operating.	10 to 26 degrees Centigrade.
Air Shipment.	-20 to +71 degrees Centigrade.
Humidity.	95% at +25 degrees Centigrade.
Maximum Altitude.	10,000 feet.

TABLE 1-2

Equipment Supplied

Description	Ref. Des.	Part No.
Major Assemblies		
Cabinet and Top Cover Assembly		102057
Power Supply Assembly		102240
Main Wire Wrap Board Assembly		102516
External Memory Assembly		102374
Page Feeder Assembly		101899
Control Console Assembly		102319
Read Head and Paper Drive Assembly		102328
RAD Test Panel Assembly		102206
Printed Circuit Cards		
Read Head Digital Circuit Card		102926
LED Generator Circuit Card		102152
Reference Alphabet Circuit Card (OCR A)		103395-1
Reference Alphabet Circuit Card (OCR B)		103395-2
Memory and Output Control Circuit Card		102407
Executive 4K Macro Circuit Card		102430
Buffer Zero and MIL-188 Interface Circuit Card		103231
Core Memory Assembly		715395-1A
Printed Wiring Board		102368
Control Panel Circuit Card		102202
Format Panel Circuit Card		102206-1
Executive 4K Macro-Memory Circuit Card		102430
Tempest (SRECO) Circuit Card		102905-2

TABLE 1-2

Equipment Supplied (continued)

Description	Ref. Des.	Part No.
LED Display and Circuit Card		102190
Read Head and Analog Circuit Card		102923
RAD Test Panel Circuit Card		102206-2
Interconnecting Cable Assemblies		
Cable Assembly	1W1A	102465-1
Cable Assembly	1W1B	103319
Cable Assembly	1W1C	102465-3
Cable Assembly	1W1D	102465-4
Cable Assembly	1W1E	102465-5
Cable Assembly	1W1F	102465-6
Cable Assembly	1W1G	102465-7
Cable Assembly	1W1H	103320
Cable Assembly	1W1J	102465-9
Cable Assembly	1W1K	102465-10
Cable Assembly	1W1L	103321
Cable Assembly	1W1M	102465-12

TABLE 1-3

Equipment Required But Not Supplied

Description	Part No.
Test Set	102870
Diagnostic Board Assembly	103390-2
Extender Board Assembly	102933
Cable Assembly J5, J6	102876
Power Cable	102940
Cable Assembly (40 Card)	102939
Cable Assembly (20 Card)	102938
Shorting Plug (Cambion)	2871-2-0312
Jumper Clip, WHT (E-Z Hook)	304-18W
Jumper Clip, GRY	304-18W
Jumper Clip, VIO	304-18W
Jumper Clip, BLU	304-18W
Jumper Clip, GRN	304-18W
Jumper Clip, YEL	304-18W
Jumper Clip ORN	304-18W
Jumper Clip, RED	304-18W
Jumper Clip BRN	304-18W
Jumper Clip BLK	304-18W
Dip Clip (Pomona Elec.)	3916
Accessory Box	102930
Accessory Box (Durphy)	DZA-206
Permabond #102 Adhesive	-
Manual	

CHAPTER 2

INSTALLATION

2-1. SITE SELECTION - The general space considerations for siting the equipment are shown in figure 2-1. The figure illustrates the minimum area required for access during operation or maintenance. If possible, space larger than the minimum area indicated is desirable to provide suitable working areas around the equipment. Provision must also be made to meet at least the minimum requirements listed below.

a. A level floor area approximately 6 feet wide by 8 feet deep.

b. The floor must be able to support a weight of 1000 pounds (or 150 pounds per square foot).

c. Adequate lighting and ventilation.

d. Provision for the power requirement in Table 1-1.

2-2. SITE PREPARATION - Before the ALPHA arrives at its destination, mark the exact installation location on the site,

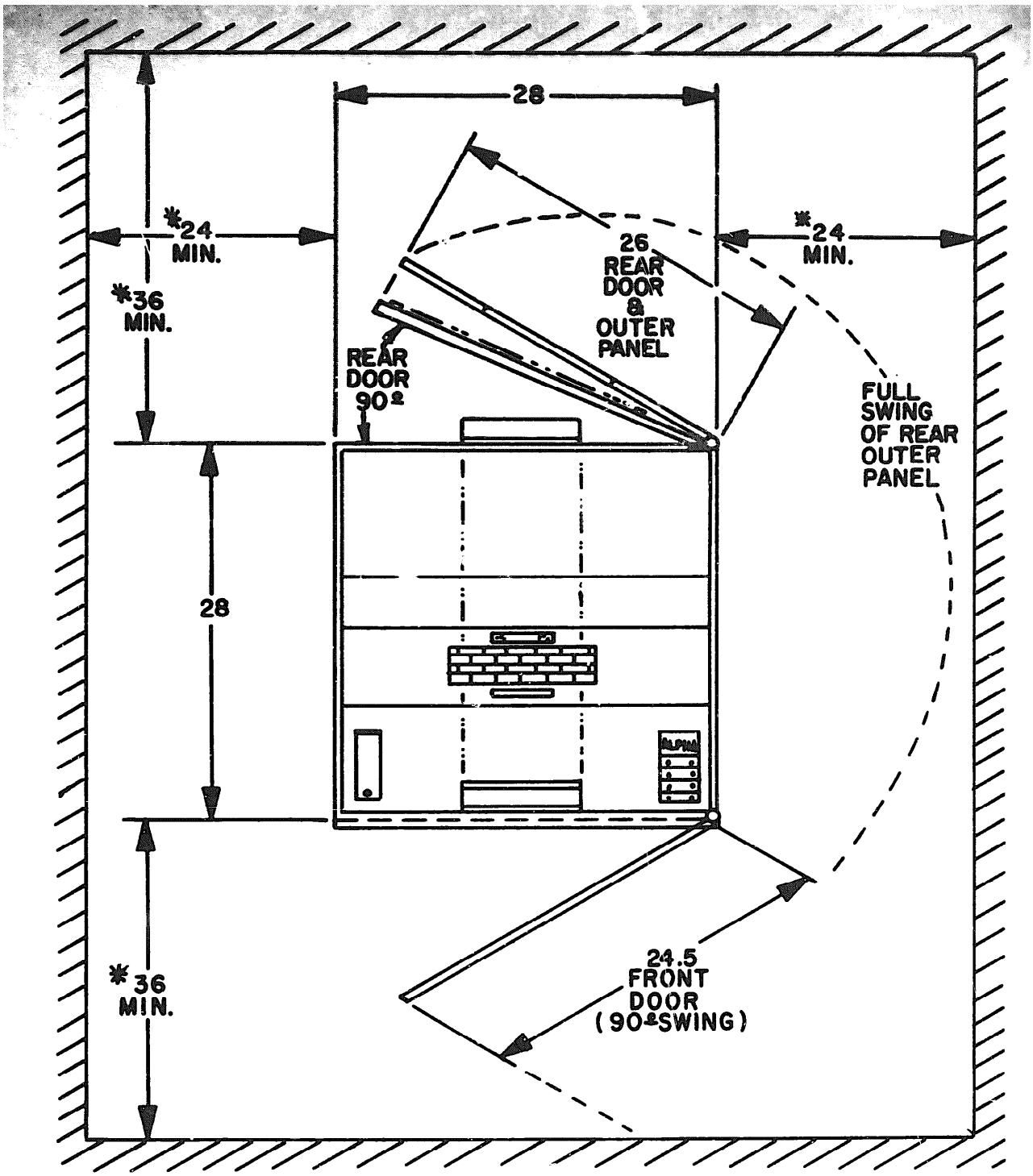
w

W

move the ALPHA

w

m w A fork



NOTES:
1. DIMENSIONS ARE IN INCHES.
* 2. AREA DIMENSIONS REQ'D. TO HOUSE THIS UNIT.

Figure 2-1. Typical Installation Area

suitable device is needed to move the equipment. Refer to table 1-1 for the weight of the unit and figure 2-2 for the maximum dimensions of the equipment when planning to move it through doorways, elevators, corridors, and other confined areas. Inspect the crate for any visible damage in shipment.

CAUTION. - Care should be exercised when moving the ALPHA. This equipment contains electromechanical components and assemblies which may be damaged if improperly handled.

2-3. REPACKING. - The equipment is shipped in a crate standing upright, The skid is located on the bottom of the equipment crate. Uncrating should be performed while the ALPHA is standing on the skid (vertical) rather than lying horizontal. Remove and store the shipping crate and packing materials for future use, Printed circuit plug-in boards are shipped installed. Follow the appropriate procedure outlined (domestic or overseasi for unpacking the equipment.

2-4. a. Domestic Unpackaging (Figure 2-3).

(1) Cut the four metal bands securing the packing carton to the wooden shipping pallet. Discard the bands.

(2) Open the top flaps of the packing carton and remove the three accessible blocks of foam packing.

(3) Carefully lift off the packing carton from the ALPHA Cabinet.

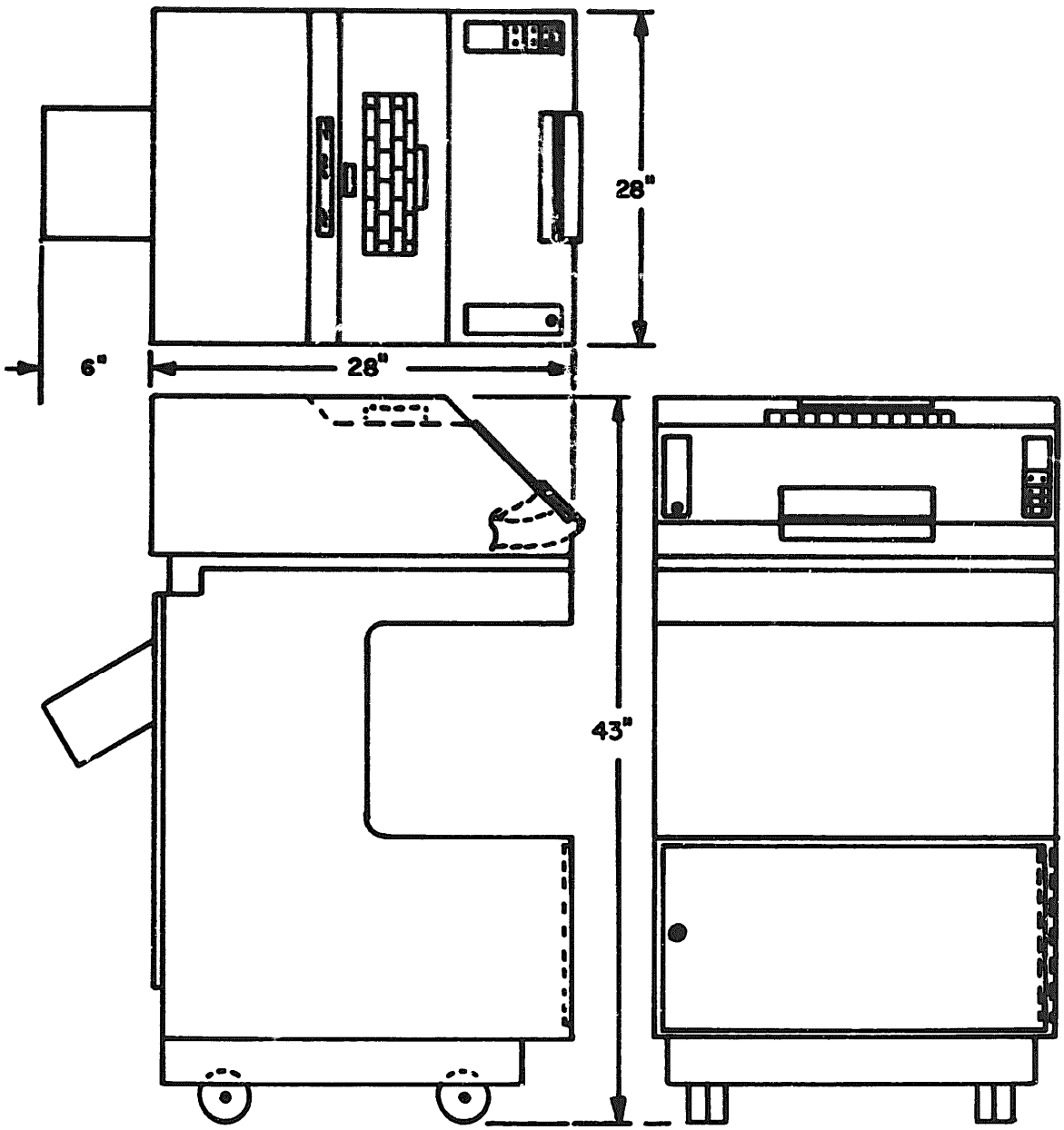


Figure 2-2. - Outline Drawing

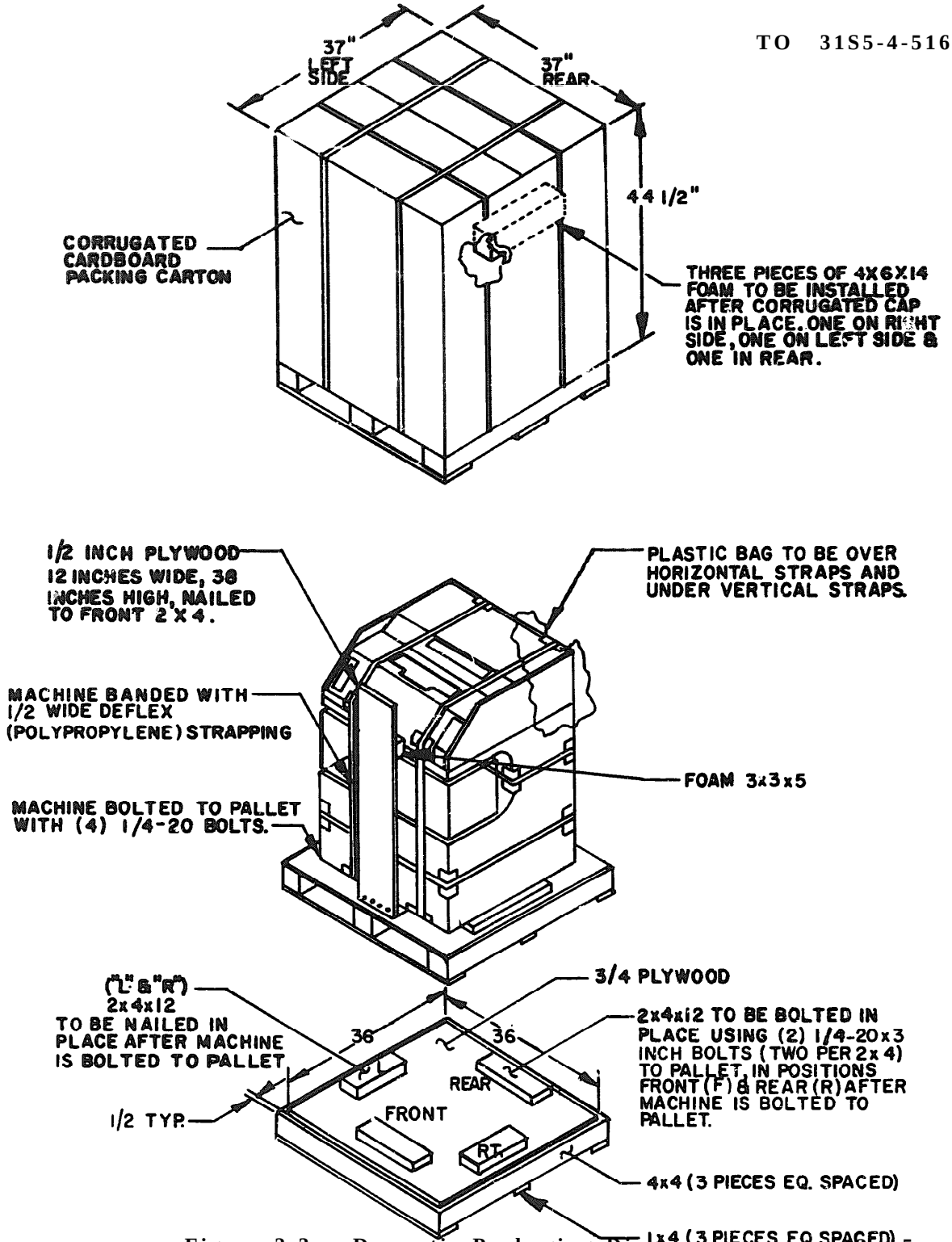


Figure 2-3. - Domestic Packaging Diagram

(4) Remove and discard the two vertical strips of banding holding the plastic bag in place. Lift off the plastic bag, fold and store.

(5) Remowe and discard the two horizontal bands securing the accessory carton in place,

(6) Remove the vertical strip of plywood and foam holding the stack feeder in place, Remove the accessory carton from the cabinet shelf space.

(7) Lift off the front lower cabinet panel, then open the rear access door.

(8) Remove the two bolts securing the front machine block 2 X 4.

(9) Remove the four bolts from the ALPHA base to the shipping pallet, Carefully roll the machine off the pallet.

(10) Where possible, reassemble all parts of the shipping materials for ease of storage.

(11) Place the equipment in its final operating position.

b. Overseas Unpackaging (Figure 2-4).

(1) Cut and fold back the steel straps around the outside of the wooden container.

(2) Remove the nails from the bottom of the wood container with a nail puller.

(3) Lift the wsod container off the skid.

(4) Remove moisture-vaporproof barrier bag and foam padding from the outside of the equipment.

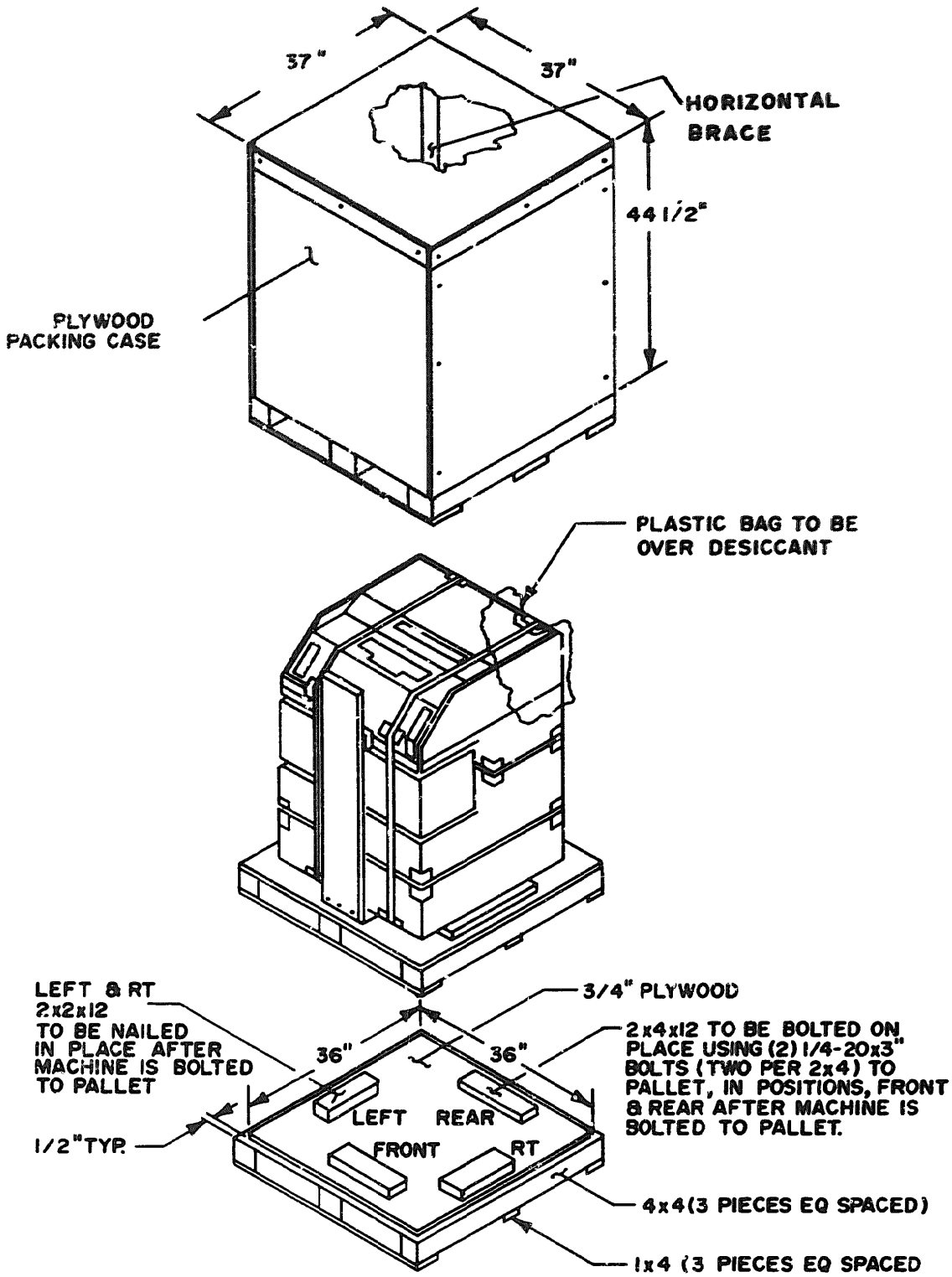


Figure 2-4. - Overseas Packaging Diagram

(5) Remove dessicant bags and humidity indicator from the unit.

(6) Lift the Optical Character Reader from the skid.

(7) Place the equipment in its final operating position.

(8)

from the exterior and interior of the ALPHA.

(9) Remove carton containing ancillary parts from the interior of the ALPHA. These items are installed on the unit during the equipment installation procedures,

2-5. EQUIPMENT INSPECTION ON DELIVERY. - When the equipment has been unpacked and moved to its operating position, inspect each assembly and subassembly carefully for possible damage in transit. Report evidence of damage immediately as required, A visual inspection of the equipment should include the following.

a. Check for dented or sprung covers or other visible signs of external damage.

b. Check for cracked or shattered glass.

c. Open access doors on the front of the equipment and inspect the seating of all assemblies.

d. Check all wiring harnesses for evidence of damage.

e. Check the equipment received against the master shipping list to make certain that all the materials have been received.

f. Check that all packing materials, dust, and other foreign matter has been removed from the equipment, Pay particular attention to points of electrical contact.

g. Report any irregularities and/or damage to the responsible procuring activity,

2-6. PRE-INSTALLATION INSPECTION. - After general inspection, check the mechanical function of switches, slides, and latches and the tightness of cable connectors and wiring. Refer to figures A-34 and A-35 during the following inspect-ion.

The control panel RESET-STOP and START-CONTINUE switches (figure A-41) should click as they are toggled up and down (each switch is spring loaded to return to the center position). Swing the format panel cover up and check the operation of the toggle and rotary switches. These switches should click positively into each position and remain there. The momentary switch should return after being pressed and released. The cover should swing down and latch positively. Check the keyboard by pressing and releasing each key; action should be smooth and silent and each key should return to its original position when released. The mirror in the viewing window above the keyboard should tilt smoothly as the mirror adjust lever is moved back and forth.

Loosen adjustable paper guide hand screws; the two paper guides should slide smoothly back and forth. When the hand screws are tightened, the guides should stay firmly in place. Loosen the two control console hand screws (on the left and right side below the control console overhang), the control console should swing back smoothly for a limited distance and stay in place, With the control console back, check all cable connectors and terminal board wiring for tightness. Slowly swing the console back down. When the hand screws

are tightened, the console should again stay firmly in place.

Open the rear access door by pressing against the latch. the latch should release as the thumb slides into the recess.- The door should swing out smoothly. The main wire wrap assembly, now exposed, should also swing out smoothly after it is unlatched. Check for loose or disconnected cable connectors on the wire wrap assembly; replace or tighten, as required. Check the nuts holding the power connections on the wire assembly; tighten if necessary, With the rear door still open, check all connections on the power supply for tightness. Close the rear door; the door and the assembly should both swing smoothly closed. Manually latch the wire wrap assembly. The rear access door should automatically latch into place when fully closed.

Report any damage to the shipper and to: CompuScan Incorporated, 900 Huyler Street, Teterboro, New Jersey 07608.

2-7. EQUIPMENT INSTALLATION PROCEDURES. - Follow the procedures outlined in the paragraph below to install the ALPHA. No special tools, materials, or equipment are required to install the unit. The printed circuit plug-in boards listed in table 7-2 and illustrated in figure A-39 are installed in place in the equipment when shipped. Make certain that all printed circuit plug-in boards are fully inserted and in their proper receptacles

a. Leveling the Equipment- - The ALPHA does not require any critical level parameters- However, after the equipment has been moved to its permanent location, the supporting surface

should be sufficiently level to stabilize the ALPHA.

b. Installation of Ancillary Parts. - Install the text hopper under the static strip as shown in figure A-35. The side tabs on the hopper hold it in place as it rests against the support.

c. Adjustment. - Set the POWER switch (figure 3-2) to OFF and unplug machine before making transformer and cable connections.

d. Transformer Connections. - Before connecting the cables, be sure the transformer primary is connected correctly. Access to the transformer is through the rear access door (figUPC A-35) and through main wire wrap assembly 1A3 located directly behind it. Transformer fuse F9 and the primary jumpers are located as shown in figure A-40. Ensure that the jumpers are installed and that fuse F9 is the correct value, as indicated below.

(1) 100 VAC Service Power. -

(a) Primary power is connected to 1A and 2A.

(b) 1A and 1B are jumper connected.

(c) 2A and 2B are jumper connected.

(d) Slo-blo fuse F9 is 10 amp.

(2) 110 or 115 VAC Service Power. -

(a) Primary power is connected to 1A and 3A.

(b) 1A and 1B are jumper connected.

(C) 3A and 3B are jumper connected.

(d) Slo-blo fuse F9 is 10 amp,

(3) 120 VAC Service Power. -

(a) Primary power is connected to 1A and 4A.

(b) 1A and 1B are jumper connected.

(C) 4A and 4B are jumper connected.

(d) Slo-blo fuse F9 is 10 amp.

(4) 200 VAC Service Power. -

(a) Primary power is connected to 1A and 1B,

(b) 2A and 1B are jumper connected.

(c) Slo-blo fuse F9 is 5 amp.

(5) 220 or 230 VAC Service Power. -

(a) Primary power is connected to 1A and 3B.

(b) 3A and 1B are jumper connected,

(c) Slo-blo fuse F9 is 5 amp.

(6) 240 VAC Service Power. -

(a) Primary power is connected to 1A and 4B.

(b) 4A and 1B are jumper connected.

(c) Slo-blo fuse F9 is 5 amp.

e. External Cable Connections. - Connect input power and output signal cables as shown on figure 2-1. After wiring connections are made, secure them to the ALPHA cabinet with the cable clamps provided (figure A-35).

f. Power Connections (figure A-31). -

WARNING

TURN OFF THE SWITCH THAT SUPPLIES THE FACILITY POWER TO THE ALPHA PRIOR TO HANDLING POWER LINES.

AC input power enters the cabinet through a power cable conduit elbow located on the Lower rear panel, right side. The conduit entrance is provided with compression fittings for heavy wall conduit. The external AC cables terminate at terminal board TB204 mounted behind the rear connector panel on the lower right side of the cabinet as viewed from the rear. The external power provided at the installation site must be 115/230 volts, single phase, with a separate safety earth ground return line. Proceed as follows to install the AC input power line.

CAUTION. Before connecting the input power cable to the ALPHA, make certain that the POWER switch (Figure A-40) on the ALPHA is set to the OFF position.

(1) Open the rear access door.

(2) Snake the power input cable through the conduit elbow.

(3) Connect the power lines to terminal board TB204 as shown on Figure A-31.

(4) Tighten the compression nut on the conduit elbow.

2-8. PACKING PROCEDURES. - The exact procedure for repacking the equipment depends upon the material available and the conditions under which the ALPHA is to be shipped or stored. For stock numbers of the materials required for preservation, packaging, and packing consult any one of the following manuals: TM-38-230; NAVEXOS P-938; AFM 71-1; or NAVMC 1144.

Preservation, packaging, and packing of the equipment for reshipment must be in accordance with the following portions of specification MIL-E-17555 as applicable.

a. Preservation and packaging for domestic shipment must be level A in accordance with paragraph 3.1.2 of MIL-E-17555.

b. Preservation and packaging for overseas shipment must be level C in accordance with paragraph 3.1.2. of MIL-E-17555.

c. Packing for domestic shipment must be level A in accordance with paragraph 3.2.2.1 of MIL-E-17555.

d. Marking for domestic and overseas shipment must be in accordance with MIL-STD-219 and paragraph 3.7 of MIL-E-17555.

2-9. STORAGE. - The ALPHA can be stored in a sheltered environment within the limitations specified in table 1-1 for periods of less than two weeks without any preservation, packaging, or packing. Limited storage for equipment to be removed from service for more than two weeks should be accomplished by using the same techniques as required for domestic shipment (refer to paragraph 2-8). If, however, the equipment is to be stored in a high humidity area, it is recommended that the equipment be packaged in accordance with the requirements for overseas shipment and that the humidity indicator be checked periodically to prevent moisture accumulations which could damage the brake-clutch assembly-

CHAPTER 3

OPERATING INSTRUCTIONS

3-1. GENERAL. - This chapter contains information and instructions for operating the ALPHA.

Note:- The operator's responsibilities are restricted to inserting scanable copy into the unit and use of the appropriate controls. All other maintenance procedures contained in this chapter are to be performed by maintenance personnel.

Perform the required procedures as outlined to assure proper operation of the equipment. Adherence to the procedures set forth in the following paragraphs will enable an operator (or maintenance personnel) with limited experience to successfully operate (and/or adjust) the equipment.

a. Operating Precautions (paragraph 3-2).

b. Identification, Description and Location of Power Up Procedure (paragraph 3-3).

c. Loading Header Sheet Sets (paragraph 3-5a).

d. Checking Margins (paragraph 3-5b).

e. Resetting Margins to Preprogrammed Values (paragraph 3-5c).

f. Setting Margins (paragraph 3-5d).

g. Loading Message Forms (paragraph 3-5e).

h. Scanning Message Forms (paragraph 3-5f).

i. Handling Unrecognized Characters (paragraph 3-5g).

j. Handling Crossouts (paragraph 3-5h).

k. Handling Error Stops (paragraph 3-5i).

l. Stopping Operation (paragraph 3-6).

m. Power Down Procedure (paragraph 3-7).

n. Deletion Symbol Editing (paragraph 3-8).

3-2. OPERATING PRECAUTIONS. - Before attempting to operate the ALPHA, carefully study the Location and function of all controls and indicators. The controls and indicators are described in paragraph 3-3. The potential danger areas are listed in paragraph 3-2c.

a. High Voltages. - This equipment employs voltages which are dangerous and may be fatal if contacted by operating personnel. Extreme caution should be exercised when working inside this equipment. While every practicable safety precaution has been incorporated in this equipment, the rules contained in the following paragraphs, b and c, must be strictly observed.

b. Keep Away From Live Circuits. - Operating and maintenance personnel must at all times observe all safety regulations. Exercise extreme caution when making adjustments inside the equipment with the power on. Under certain conditions, dangerous potentials may exist with the power controls in the off position due to charges retained by capacitors. To avoid casualties, the maintenance technician should always remove power and discharge circuits by means of a grounding stick prior to

touching them. Maintenance personnel should familiarize themselves with the techniques of resuscitation found in the Manual of First Aid Instructions.

c. Potential Danger Areas. - There are major potential danger areas within the ALPHA. These areas are:

(1) Power Supply Capacitor bank.

(2) Exposed AC Line terminals on the primary input.

(3) Top side of Upper Platen.

(4) Bottom side of Page Feeder Relay.

3-3. CONTROLS AND INDICATORS. - All operating controls and indicators are located on the Control Console. The functions of the operating controls and indicators are described in tables 3-1, 3-2, and 3-3 for the top of the Control Console, the Format Panel and the Control Panel, respectively. Figure 3-1 shows the controls and indicators on top of the Control Console, Figure 3-2 shows the Format and Control Panels.

3-4. POWER UP PROCEDURE. - Set the POWER switch to ON; four paper viewer lamps, Control Console Fan, Paper Handler Fan, Card Case Fan, and Power Supply Fan will come on. After a brief delay, main power supply will come on and LED display will indicate three NUL characters (figure 3-3).

3-5. OPERATION. - The following procedures are necessary for ALPHA operation:

a. Loading Header Sheet Sets. - This step is necessary only when the Output Code Conversions are to be changed or when the output data is not being code converted correctly.

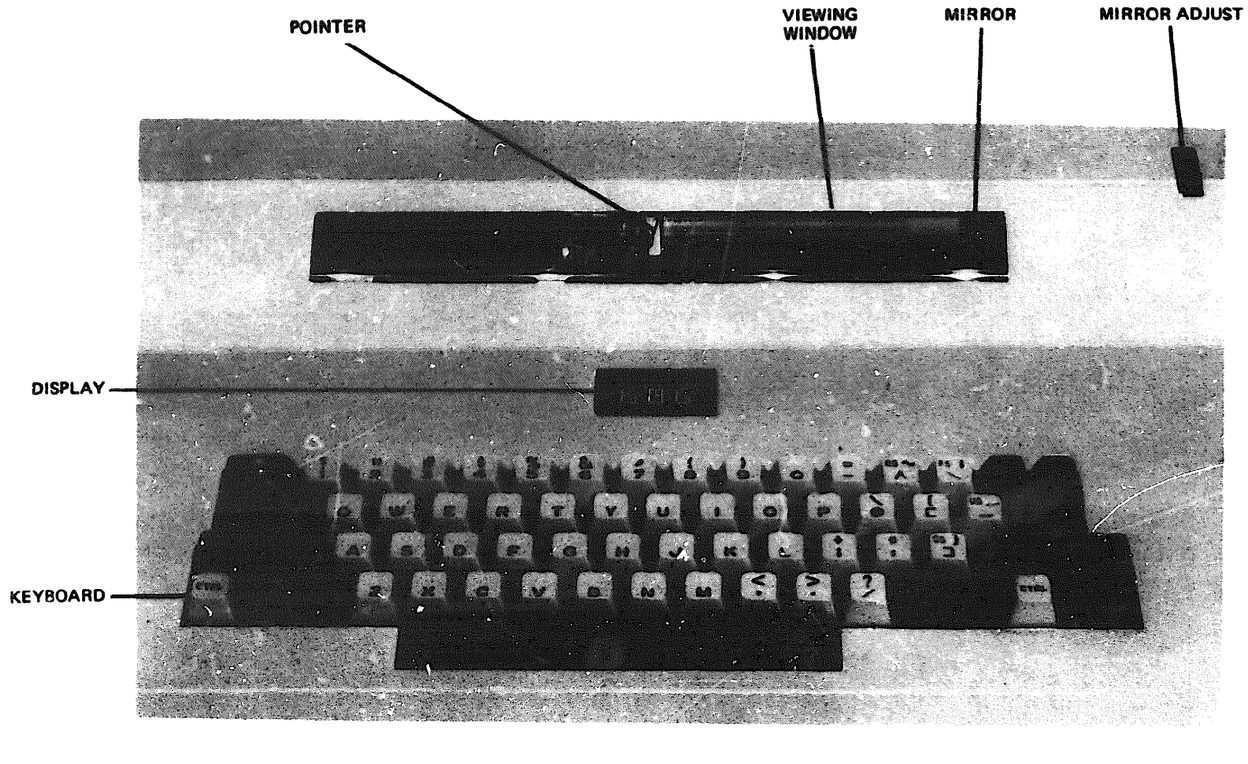
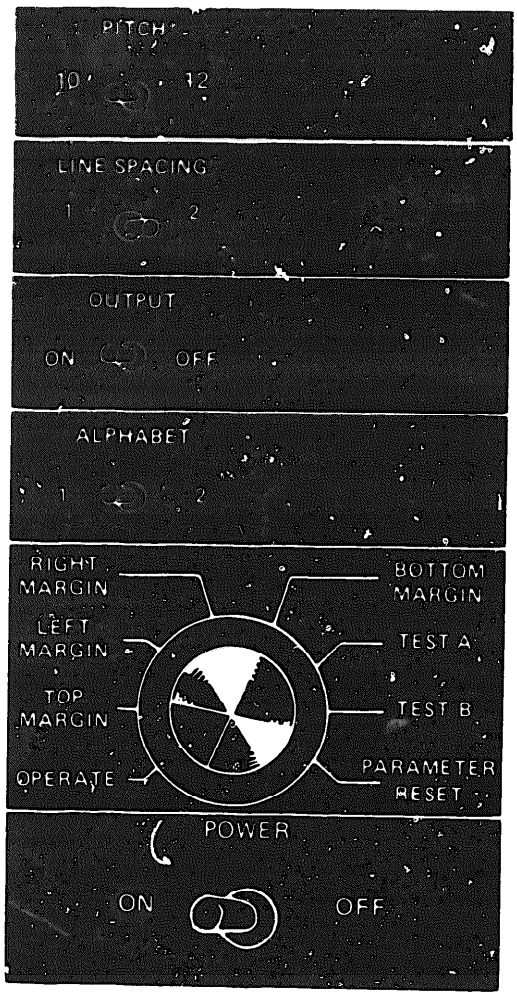
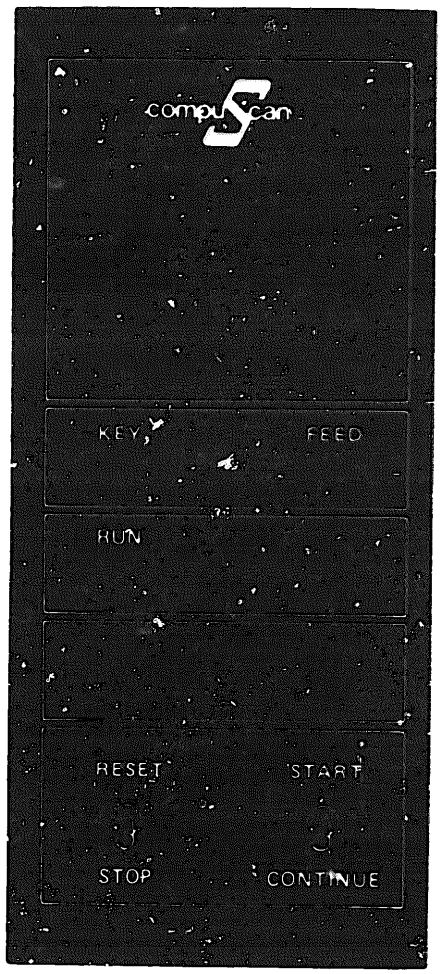


Figure 3-1. Control Console, Top View



FORMAT PANEL



CONTROL PANEL

Figure 3-2. - Operating Panels

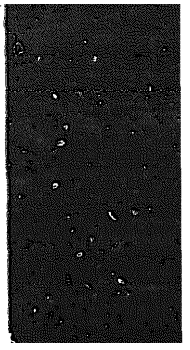
Refer to the Programming Manual for an explanation of how the user may program the ALPHA:

(1) To scan pages in accordance with desired rules.

(2) To output user defined codes for each character on the typing element.

(3) To output user defined codes for various functions, such as LF, CR, SI, SO.

For instance, the ALPHA may be programmed to read the DD173 Messageforms and output an 8-level, odd or even parity ACSII code for each character. For backup use, it may be programmed to output 5-level ITA-2 codes. The scanning rules and code conversion tables are defined on typed pages called Header Sheets.



The ALPHA Programming Manual explains the various programming options available to the user and how to change parameters or code conversion tables via Header Sheets- There will be two sets of Header Sheets supplied with every ALPHA:

(1) DD173/ASCII. - These Header Sheets program the ALPHA to read the DD173 (OCR) Message form and output an ASCII code for each character. These Header Sheets are designed for use of the ALPHA within the STREAMLINER program.

(2) DD173/ITA2. - These Header Sheets program ALPHA to read the DD173 (OCR) Message form and output ITA2 code for each character. These Header Sheets are designed for use of the ALPHA with an off-line device such as a paper tape punch. In addition, certain message format requirements, such as the EOM, are included.

b. Checking Margins. - When the Mode Selector Switch is set to one of the margin positions (top, left, right, or bottom) the value currently in use for that margin will be displayed on the three digit displays The numerals are the margin measurements in tenths of an inch from either the top or left edge of the paper. The absolute value displayed is divided by 10 to obtain the margin value in inches,

Example: The number 076 is displayed. Dividing by 10 gives 07.6. This margin is 07.6 inches from the edge of the paper.

CARE SHOULD BE TAKEN to insure that the Mode Selector Switch is NOT rotated through the PARAMETER RESET position when checking margins; this would cause the margin values to be reset to preprogrammed values.

c. Resetting Margins to Preprogrammed Values. - One set of scanning values is preprogrammed into the ALPHA. These values establish the correct parameters for processing the DD173 (OCR) Messageform.

To use the DDl73 values:

(1) Wher. the ALPHA is in the STOP OR RESET mode, rotate the Mode Selector Switch to the PARAMETER RESET position-

(2) Rotate the Mode Switch counterclockwise through each of the margin positions checking that the values shown on the LED display are the correct values as specified in table 1-1.

(3) Return the Mode Selector Switch to OPERATE. This procedure also causes values to be established for:

(a) Line spacing - 6 lines per inch,

(b) End of line criteria - 68 spaces from last scanned character in a line.

(c) Null End of Line criteria - 3" from left margin.

(d) End of Page criteria - 2 Null lines after last scanned Line,

These values may be changed through the use of @ Commands as described in the Programming Manual.

d. Setting Margins. - Margins may be set to values other than DD-173 through the keyboard. The procedure is:

(1) While the ALPHA is in the STOP or RESET mode, rotate the Mode Selector Switch clockwise to select the margin that is to be changed; the display will show the value currently in use.

(2) Use the "A" key to add to the value shown, or the "S" key to subtract from the value. Tapping the keys will cause the value to change by 1/10 inch. Holding the key down will cause the value to change rapidly, until the key is released.

(3) Repeat the process for any other margins that are to be changed.

(4) Rotate the Mode Selector Switch counterclockwise to the OPERATE position.

e. Loading Messageforms. - The ALPHA's Page Feeder may be loaded with stacks of up to 50 messages ranging in size from 11" X 11" down to 5" X 7"; the length in the direction of feed

must be at least 7". Sheets of copy longer than 11", up to 11" X 24", must be loaded one at a time with the Page Feeder removed.

Copy is placed into the Feeder face up, top line towards the machine, with page numbets increasing from top to bottom. Load copy into the Feeder no further than the edge of the tray inside of the assembly; no force is required, Copy inserted too far into the Feeder will cause a paper jam.

If the ALPHA is already operating and the FEED indicator is on, all that is required to load more copy of the same size is to place the copy neatly in the tray. When the copy is positioned correctly, the top page tends to float upwards lightly and feed in. If the FEED light is off, START must be toggled to feed the copy.

Perform the following procedure to load the Paper Feeder after installation or when the page size is to be changed (see Figure A-34):

(l) Loosen paper guide hand screws underneath the tray-

(2) Position paper in the center of the tray between the guides,

(3) Slide guides up to paper edges allowing l/16" clearance on either side. Guide position, within the entire horizontal space available, is not critical.

(4) Tighten paper guide hand screws.

f. Scanning Messageforms. - To initiate scanning, toggle the START switch. During normal scanning, the first three characters of a line are displayed in the LEDs after the line is read.

During normal operation, the ALPHA may stop and sound an alarm. This signifies that one of the following conditions has occurred:

(1) An unrecognized character has been scanned, in which case the Read Head will stop such that the red pointer in the viewing window points to the unrecognized character (see section 3-5, paragraph g, for corrective action).

(2) A crossout has been scanned, in which case the Read Head stops with the pointer indicating the crossed out character or the first character if more than one was crossed out (see section 3-5, paragraph h, for corrective action).

(3) An Error Stop has occurred in which case operation stops and a "BEL" Error Message is displayed on the LED display (see sesection 3-5, paragraph i, for Error Message Meanings and corrective action).

g. Handling Unrecognized Characters. - While scanning the messageforms, the ALPHA may encounter two different types of unrecognized characters; those which are unrecognizable by the machine or those for which it can make a best guess, but is not sure enough of the guess to output it without asking the operator to confirm the guess. In either case, the scanning operation halt with the Read Head positioned such that the red pointer in the viewing window points to the unrecognized character.

(1) Unrecognizable. - Where the character is unrecognizable, "US^{W} character (figure 3-3) will appear in the center of the display. The characters on either side of the unrecognized character in the text also appear on each side of the

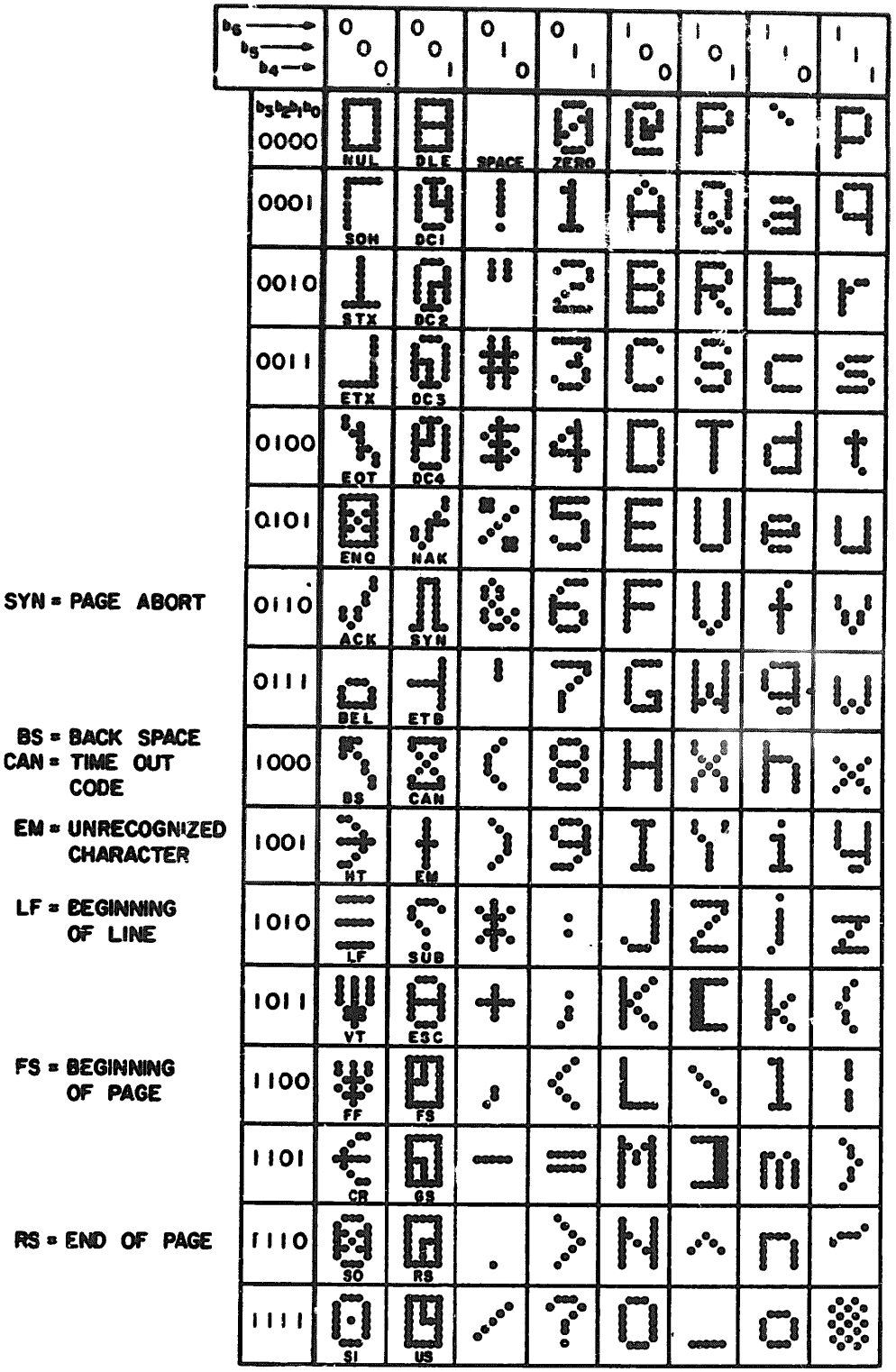


Figure 3-3. LED Character Patterns

"US" character. (The unrecognized character may be a single crossed out character.) In the event of an unrecognizable character, either:

(a) Press the correct character key(s) on the keyboard. The last character will appear on the display in the center position. Depress CR to resume operation.

(b) Depress CR only to delete the character and resume operation.

(2) Best Guess. - If the ALPHA encounters a slightly disfigured or poorly typed character, it will stop the scan operation, display its best possible identification, and ask the operator to confirm its best guess. The display will show the best guess character in the center position with the characters on each side of it. In the event of a disfigured or poorly typed character, perform one of the following steps:

(a) Best Guess Correct. - If the character under the pointer and the best guess shown on the display are the same, press the CR key on the keyboard to accept the character. The tone will stop and scanning will resume.

(b) Best Guess Incorrect. - If the character under the pointer and the best guess are not the same, press the correct character key(s) on the keyboard; the tone will stop and the correct character will appear at display center in place of best guess. Press the CR key on keyboard; scanning will resume,

(c) Best Guess Deletion. - If it is necessary to delete the best guess character without inserting a new character,

press the BACK SPACE key; tone will stop and back space symbol (BS in figure 3-3) will appear at display center. Press the CR key on keyboard; scanning will resume.

(d) Incorrect Entry. - If during the preceding steps an incorrect entry was made on the keyboard, perform the following procedure:

1. Press BACK SPACE key on keyboard; previous keyed character or, if none, back space symbol will appear at display center.

2. Enter correct character on keyboard; correct character will appear at display center.

3. Continue entries as required.

4. Press CR key on keyboard; reading will resume.

h. Handling Crossouts. - If more than one character is crossed out, (by placing a horizontal line midway through the characters with a carbon black felt tip pen) a horizontal crossout character (US in figure 3-3) will appeal- at display center. The characters before and after the crossout in the text also appear before and after the crossout character. The red pointer in the viewing window will indicate the first character of the crossout.

If the crossout is located at the left margin, a left margin character (LF in figure 3-3) will appear in the left LED) of the display. If the crossout extends to the end of the line, a NUL character will appear- in the right LED of the display. If an entire line is crossed out, the first character on display is left margin, the second is horizontal crossout, and the third is NUL.

In the event of a crossout proceed as follows:

(1) Crossout Deletion. - If you desire to delete the entire crossout, press the CR key on the keyboard. The tone will stop and scanning will resume.

(2) Character Crossout Correction. - Where it is desired to replace the crossout with different characters, enter the desired character or characters on keyboard; tone will stop and each character entered will appear at display center as key is pressed. Press CR key on keyboard; reading will resume.

(3) Line Correction. - If an entire line is corrected, perform the following procedure.

(a) Press NUL key on keyboard; Read Head will move to far left, tone will stop, and three NUL symbols will appear on display.

(b) Enter entire correct line on keyboard; each character entered will appear at display center as key is pressed.

(c) Press CR key on keyboard; reading will resume.

(4) Incorrect Entry. - If during the preceding steps an incorrect entry was made on the keyboard, perform the following procedure:

(a) Press BACK SPACE key on keyboard; previous keyed character or, if none, back space symbol will appear at display center.

(b) Enter correct character on keyboard; correct character will appear at display center.

(c) Continue entries as required.

(d) Press CR key on keyboard; reading will resume.

Asterisks, as well as crossouts, are used for in-text editing. See paragraph 3-8. One asterisk in text will delete the previous character including a space. Two asterisks will delete all characters back to, but not including, the previous space or margin. Three asterisks delete all characters back to left margin. In each case, reading continues without pause. All asterisks are deleted from the output. Asterisks may, however, appear on the display.

i. Handling Error Stops. - The ALPHA's program has provisions for detecting and displaying error conditions within several areas of its operation. These areas include paper movement, scanning, editing, output and the header sheet routine.

Displayed in the leftmost LED of the display will be a BEL symbol (see figure 3-3) which denotes that an error condition exists. Contained in the middle LED will be either a "P", "S", "E", "O", or "H" character defining the error. The third LED may display a number from 0 to 9 which identifies the particular error in that group. Refer to table 3-4 for a listing of most display error messages.

The characters displayed in the middle LED indicate failures of the following natures;

P Paper feed

S Hardware failure

E Edit error

O output error

H Header Sheet error

When an error occurs, ALPHA will stop scanning and an audible alarm will sound. To stop the alarm and clear the error condition, the RESET and START switches must be toggled respectively to reinitiate operation. Check the display error message against table 3-4 to find and remedythe error.

WARNING

DO NOT AT ANY TIME ATTEMPT TO REINITIATE OPERATION IF A BEL-P-3 OR BEL-P-4 ERROR CONDITION EXISTS WITHOUT FIRST CLEARING ANY PAPER JAMS.

(1) Toggle RESET.

(2) Loosen the two screws which secure the upper console located under the front corners of the machine directly below the Format and Control Panels (see figure A-34).

(3) Slowly raise the upper console until it reaches the stop.

(4) Remove any paper jammed in the Page Feeder or Paper Handler.

(5) Lower the upper console and secure the two screws.

(6) Reinitiate operation by toggling START.

3-6. STOPPING OPERATION. - Operations will stop if the STOP switch is toggled, or the RESET switch is toggled, or an automatic stop occurs when one minute passes during which no

Messageforms are available in the feed tray. The ALPHA is in Standby Mode when the FEED, RUN, and Read Head Lamps are off.

If ALPHA is placed in the Standby Mode with the STOP position of the RESET/STOP switch, the line being read will be finished and scanning will resume if either START or CONTINUE is toggled, The Read Head will be at the extreme left. It CONTINUE i s toggled after STOP, scanning resumes on the next line of the same page. If START is toggled, any Message forms under the Read Head Assembly will be ejected and scanning will begin on a new Message form. If the mode selector is moved from the OPERATE position, START must be toggled.

If the RESET position is toggled, scanning stops wherever the Read Head is at that moment. START must be toggled to resume operation. Any paper under the Read Head Assembly will be ejected and scanning will begin on a new Message form.

If all the Message forms in the paper tray have been scanned and no additional forms are inserted, the ALPHA will automatically go into the Standby Mode after one minute. The Read Head will be in the center position. When ALPHA automatically goes into the Standby Mode, START must be toggled to resume operation, Since the last Message form was ejected prior to going into the Standby Mode, scanning will start on a new Message form,

3-7. POWER DOWN PROCEDURE. - Set the POWER switch to OFF. All lights and fans will go off (the control console fan will continue to rotate for a short time).

3-8. DELETION SYMBOL EDITING. - Typographical errors that are detected during typing can be easily corrected by the use of a special deletion symbol which will not appear in the output data

The rules for deletion symbol editing are quite simple. The typist may delete a character, word, or line by typing one, two, or three deletion symbols respectively.

*	Deletes the previous character,
**	Deletes the previous word (back to the previous space or beginning of line, whichever came last).
***	Deletes the line (back to left margin).

a. Single Delete. - The single delete (*) eliminates the immediately preceding character. The deleted character may be anything including a space or character. Never put a space between the character to be deleted and the deletion symbol as that would delete the space and not the character.

INPUT: THIS IS AN EXAMPLE OF CHARACTR*ER EDITING.

OUTPUT: THIS IS AN EXAMPLE OF CHARACTER EDITING.

In the above example, the typist spotted the absence of the "E" in "CHARACTER", deleted the "R" by typing one deletion symbol (*) and typed "ER" to finish the word "CHARACTER".

b. Double Delete.. - The double delete (**) eliminates all. preceding characters up to, but not including, a space, Double deletion symbols following a space are improper procedure and are ignored.

INPUT: THIS IS A WORD COREC**CORRECTION.

OUTPUT: THIS IS A WORD CORRECTION.

Here the typist has forgotten the second "R" in the word "CORRECTION", deleted the incorrect word (COREC) with "**" and retyped the word correctly. Note that no space appears before the first deletion symbol or after the last deletion symbol.

c. Triple Delete. - The triple delete (***) eliminates all characters and spaces, including an indent, back to the left margin. The line may be retyped immediately following the triple deletion editing or begun again on the following line,

INPUT A: THIS WAS**IS A BOD**BADLY RYED***THIS WAS BAD.

INPUT B: THIS WAS**IS A BOD**BADLY RYED***
THIS WAS BAD.

OUTPUT A: THIS WAS BAD.

OUTPUT B: THIS WAS BAD.

The typist here had much difficulty getting started. making excessive errors, three deletion symbols (***) were typed which deleted everything up to the left margin and finally retyped the desired line. Notice that you may continue typing immediately after the first deletion symbol or drop down to the next line and continue typing there,

INPUT: CHARACTR*EX**CHARACTER AND WORD DELETES MAY
BE COMBINED.

OUTPUT: CHARACTER AND WORD DELETES MAY BE COMBINED.

In this example, the typist deleted the original word in addition to the single character deletion. Only the word "CHARACTER" would appear on the output. Any combination of one, two, or three deletion symbols may be used in a line.

TABLE 3-1

Control Console Controls and Indicators

(See Figure 3-1)

CONTROL OR INDICATORS	FUNCTION
Viewing Window	Used to view ALPHA reading operation and to check defective characters when an error is indicated.
Mirror Adjust	Adjust mirror in viewing window.
Red Pointer	Attached to the Read Head assembly. Points to a defective character or the beginning of a crossout.
3-LED Display	During normal operation, displays first three characters of each line after it is scanned. It also displays error indications and, when mode selector is in a MARGIN position, indicates margin values.
Keyboard	Provides communication between operator and ALPHA to set margins and correct errors.

TABLE 3-2

Format Panel Controls

(See Figure 3-2)

CONTROL	SWITCH POSITION	FUNCTION
POWER	ON	Applies service power to ALPHA circuits.
	OFF	Disconnects service power from ALPHA circuits.
PITCH	10	Sets ALPHA to read 10 characters per inch type (for use with OCR-B and OCR-A fonts).
	12	Sets ALPHA to read 12 characters per inch type (for use with OCR-B font only).
LINE SPACING	1	Sets ALPHA to read single spaced, 4, 5, or 6 lines per inch type.
	2	Sets ALPHA to read double spaced, 2, 2-1/2, or 3 lines per inch type.
OUTPUT	ON	Normal position for data output.
	OFF	Inhibits data output; must be held in this position to introduce Header Sheets.

TABLE 3-2

Format Panel Controls (continued)

CONTROL	SWITCH POSITION	FUNCTION
ALPHABET	1	Sets ALPHA to read primary font.
	2	Sets ALPHA to read a second font if installed. Normally disabled.
MODE SELECTOR	OPERATE	Sets ALPHA to read text for output or for programming output codes.
	TOP MARGIN	Places top margin value in LED display when ALPHA is in Standby Mode and enables keyboard A or S keys.
	LEFT MARGIN	Places left margin value in LED display when ALPHA is in Standby Mode and enables keyboard A or S keys.
	RIGHT MARGIN	Places right margin value in LED display when ALPHA is in Standby Mode and enables keyboard A or S keys.
	BOTTOM MARGIN	Places bottom margin value in LED display when ALPHA is in Standby Mode and enables keyboard A or S keys.
	Test A	Used for troubleshooting
	Test B	Used for troubleshooting.
	PARAMETER RESET	Selects default reading values when ALPHA is in Standby Mode.

TABLE 3-3

CONTROL PANEL CONTROLS AND INDICATORS

(See Figure 3-2)

CONTROL	SWITCH POSITION	FUNCTION
FEED LAMP		Indicates ALPHA page feeder is ready for more copy. Flashes as each sheet is ejected and next sheet is picked up.
RUN LAMP		Indicates ALPHA scanning function is operating.
KEY LAMP		Indicates ALPHA is waiting for a Keyboard input.
RESET/STOP SWITCH	RESET	Places ALPHA in Standby Mode. Used when scanning is to be resumed on new sheet.
	STOP	Places ALPHA in Standby Mode. Used when scanning is to be resumed on same sheet.
START/CON-TINUE SWITCH	START	Starts scanning on new sheet after RESET-STOP switch is toggled.
	CONTINUE	Starts scanning again on same sheet after STOP is toggled.

TABLE 3-4

LED Display Error Messages

DISPLAY INDICATION	ERROR
BEL-P-2	Double page feed.
BEL-P-3	Paper feed jam (no paper within 3 seconds).
BEL-P-4	Page eject failure.
BEL-S-1	Possible hardware failure; SR2 shifting too long, rescan sheet.
BEL-S-2	Possible hardware failure; Recognition never went ON/OFF, rescan sheet.
BEL-S-3	Possible hardware failure; Recognition never went OFF, rescan sheet.
BEL-E-1	Program malfunction; rescan sheet.
BEL-E-2	Program malfunction; rescan sheet.
BEL-E-3	Output buffer overflow (line greater than 250 characters).
BEL-E-4	Program malfunction; rescan sheet.
BEL-O-1	Output device not ready; clock/ control signal missing.

TABLE 3-4

LED Display Error Messages (continued)

DISPLAY INDICATION	ERROR
BEL-H-0	A number in an @ command or on a Header Sheet was larger than the allowed maximum for a number used in this context.
BEL-H-1	Illegal @ code on Header Sheet line.
BEL-H-2	Header Sheets out of sequence (i.e., an attempt was made to read a longer input string length code).
BEL-H-3	Illegal character to the right of the equal sign on a Header Sheet line.
BEL-H-4	Missing or incomplete specification of the output field (right of equal sign) on a Header Sheet.
BEL-H-5	Attempt to output from incorrectly defined code conversion table.
BEL-H-6	@ command error (such as no space following the command).
BEL-H-7	Code conversion table full.
BEL-H-8	Scanning parameter error (out of range).

CHAPTER 4

PRINCIPLES OF OPERATION

4-1. INTRODUCTION. - The ALPHA provides the means for scanning typewritten lines on a page, identifying each character, and assembling the resultant characters into a complete line representative of the typed line. This data may then be forwarded to the selected output device. The output code may be structured to conform to that of the selected output device.

The ALPHA consists of several blocks (Fig. 4-1). each of which is assigned a specific task. These "Macros" are circuits requiring only an instruction telling it when to start. It will then perform its task and provide a feedback signal indicating when it has reached completion. Supervising these Macros is an "Executive Macro" which provides a series of instructions which control all operations.

The scanning process requires that two electro-mechanical operations take place. The first is that the page be moved through the Page Feeder Assembly (vertical) to a position where the Read Head Assembly can be moved across the line (horizontal). The other operation is the movement of the Read Head across the page. The vertical movement of the page is controlled by the Vertical Servo Controller. The movement of the Read Head Assembly across the page is controlled by the Horizontal Servo Controller. Each Controller performs its task as directed by the Executive Macro.

Once the page has been positioned and the Read Head is being scanned across the line the data on that line must be detected, identified and assembled. These functions are performed by several more of the blocks.

The first task is to detect the character on the page. Since the page which is to be read contains black characters on a white background, the characters can be detected by evaluating the reflective patterns viewed by the Read Head Assembly as it moves across a line. The black characters will reflect very little of the light projected onto the page by the Read Head Lamp while the white areas around the character will cause high reflection of the light.

The Video Acquisition circuitry takes vertically aligned samples (slices) of the reflective pattern at regularly spaced intervals. These vertical slices of the character contain the data as to where the Read Head sees black and where it sees white. If, for example, the Video Acquisition circuit took 14 samples during the time the Read Head moved from the left edge to the right edge of a character, these vertical slices could later be reassembled into a matrix representative of the character over which the Read Head passed. The Video Acquisition circuitry, therefore, is responsible for processing the samples on a regular basis, converting the data into a digital form, and storing each completed sample such that it may be passed along to the next block.

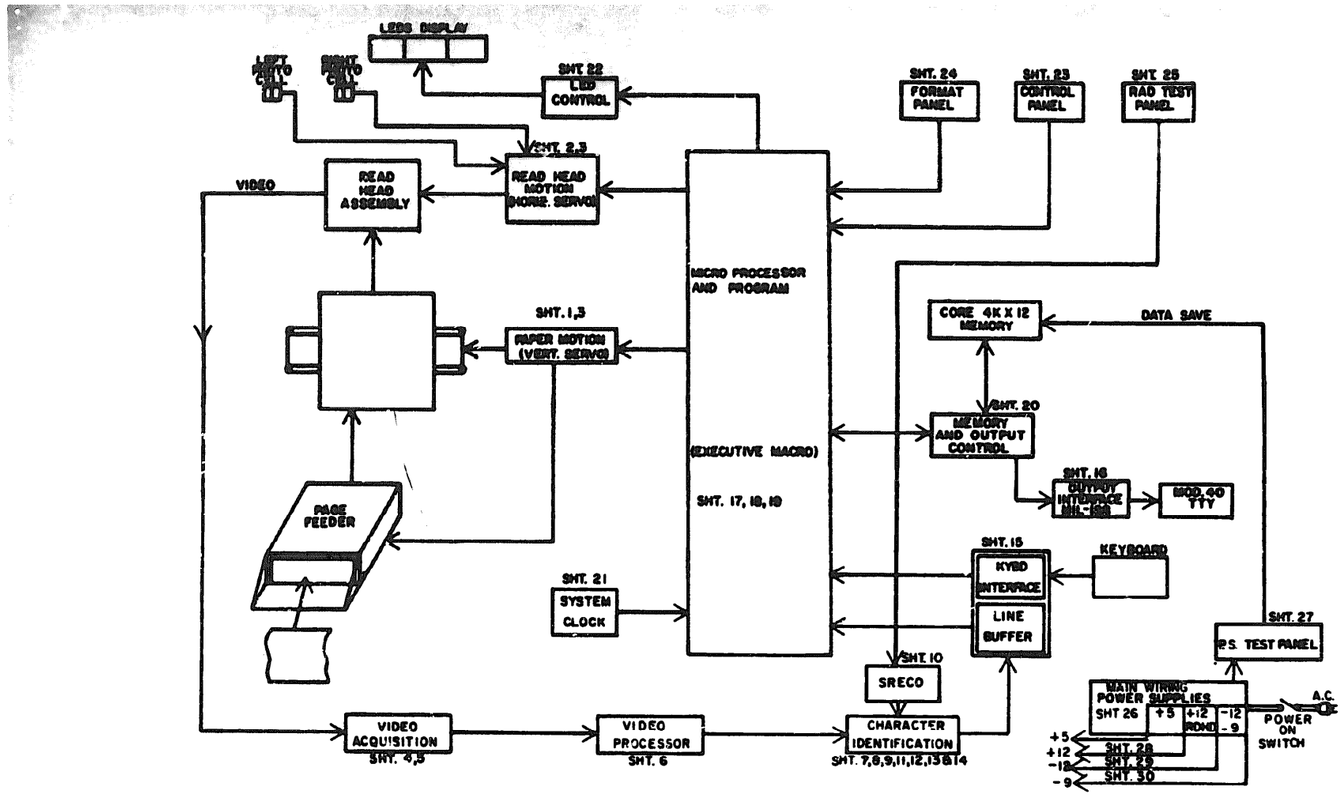


Figure 4-1. - System Functional Block Diagram

The Video Processor is the next block to handle the data. The Video Acquisition circuitry takes individual samples and passes them along to the Video Processor which assembles them into a matrix representative of the character scanned. In the previous example of the character which generated 14 samples during the time it took the Read Mead to travel. from its left edge to its right edge, the Video Acquisition circuitry passed these 14 samples along to the Video Processor which assembled them into a matrix. This matrix will show where black was detected on the page and where white was seen around and through the character.

In order to understand what is about to happen, assume that you are holding in your hand a single keypunch card with holes punched in it. On a table in front of you there is a pile of sixty-four keypunch cards, each different. One of the cards in the pile matches the card in your hand. You want to find that matching card. Assuming that the operation has to be done manually, you would have to take each of the cards in the pile, hold it against the card in your hand, align the bottom and left edges, and check to see if the holes match. booking from the front, you could see where the rear card was missing holes. Looking from the back, you could see where the front card was missing holes. When the mate was finally found, there would be no holes missing.

The Character Identification process is very similar to this, except that it is unlikely that a perfect match will occur.

instead, the closest match is accepted as the mate. Within the responsibility of the Video Processor is the function of aligning the Unknown Matrix. In the example, it was stated that the cards have to be aligned with respect to the left and bottom edges. The matrix must be moved around to allow proper comparison with the Reference Characters. The Reference Characters, the equivalent of the stack of cards, are aligned with their lowest point on an imaginary baseline and their leftmost point against a left axis. The Video Processor moves the Unknown Matrix into an identical alignment. Once this alignment has been made, the assembled and aligned matrix is passed along to the Character Identification circuitry.

The Character Identification circuitry now has to take the Unknown Matrix and determine which character it represents. If we go back to the keypunch example, we find that we have an Unknown equivalent to the card in our hand. There is a part of the Identification circuitry known as the Reference Alphabet. It is the equivalent of the stack of cards. It contains a whole series of Reference Characters, a matrix representative of what each perfect character should look like. The Character Identification circuitry compares the Unknown (single card) against each of the Reference Characters (the cards in the stack). Another portion of the circuitry, the Evaluation section, then checks for errors (looks through the holes), In the case of actual Character Identification, it is unlikely that a perfect match will occur. The Evaluation

circuitry, therefore, checks to see how many errors exist when each Reference Character is compared with the Unknown. The one which has the fewest errors (non-matching holes) is considered to be the match for the Unknown and is designated as the BEST ID. The ASCII code for this character is forwarded to the next section.

The next section is the Input to the I/O circuitry, This circuitry allows the multiplexing of data from either the Best ID Latches of the Character ID section or from the Keyboard during Key Optics Stops. It passes the selected data to the Line Buffer section.

The Line Buffer is a Shift Register 12 bits wide by 128 locations. It assembles and stores the individual characters that are being forwarded from the Character Identification circuitry or the Keyboard. The Line Buffer's 12 bits are divided as follows. Eight bits are used to store the ASCII code for the character (Line Buffer). The other four bits are used to store flags associated with that character (Flag Buffer). Two of the flags were established during the Video Processing operation. These are the WMF1 & VMF2 flags which indicate whether the character was touching the top or bottom of the Scan Window respectively. The other two flags were developed during the Character Identification process. One is the Touching Character Flag which indicates whether the character was too wide and was, therefore, probably two characters touching each other, It may also have been a horizontal

crossout. The second flag is the Unrecognized Flag which is generated whenever the error count for the identified character was higher than the Confidence Level stored in the CPM for that same character. This flag will set whenever a character is fuzzy, smudged, or disfigured,

The output from the Input to the I/O section feeds one place, THE EXECUTIVE MACRO COMPARE MULTIPLIER. As the data is transferred, the Flags associated with each character are checked. If a VMF1, VMF2, or Touching Character Flag is detected and Key Optics is on, a Crossout symbol will be displayed in LED 2 with the preceding character in LED 1 and the following character in LED 3. If an Unrecognized Flag is detected, the Best Guess character will be put in LED 2 with the preceding and following characters in LEDS 1 & 3 respectively. On any of these occasions the scan process will cease and the Read Head positions such that the attached pointer is aimed at the character on the page which corresponds to the data displayed in the center LED.

If there were no flags set, or once the Key Optics corrections have been made, the entire line is transferred to the Core Memory. Al& the previous sections are then freed to go about scanning and assembling the next line. Meanwhile, the line in the Core Memory has to be code converted via the header sheets, and then given to the output control circuitry.

In summation, each of the individual operations has been discussed, but it is important to realize that several simultaneous

operations are taking place. The Video Acquisition and Processor sections are involved in collecting and assembling samples of the one character over which the Reed Head is currently passing. The Character Identification circuitry is involved with identifying the previous character which the Video Processor forwarded. The Core Memory and Output Macro are outputting the previous line. When the character undergoing identification has been completed, it is placed in the Line Buffer. As soon as the character being scanned has been fully assembled, it is forwarded to the Character Identification circuitry. The Video Processor then starts collecting the next character and the Character Identification circuit starts on the character just forwarded to it. Eventually, the Output will have been completed and all the characters on the current line will have been identified and placed in the Line Buffer. this Line is then transferred to the Core Memory for outputting and the scanning of yet another line commences.

Program-wise, the ALPHA is considered to have three modules as shown on the ALPHA System Operating Programs Block Diagram figure 4-2. Each module directs and controls certain of the machine functions.

The Scan Module is charged with controlling the mechanical operations. It also finds the characters, takes the samples, identifies each character, and assembles the characters in the Line Buffer, The Line in the Line Buffer is a raw form containing all the questionable characters identified by the various Flags.

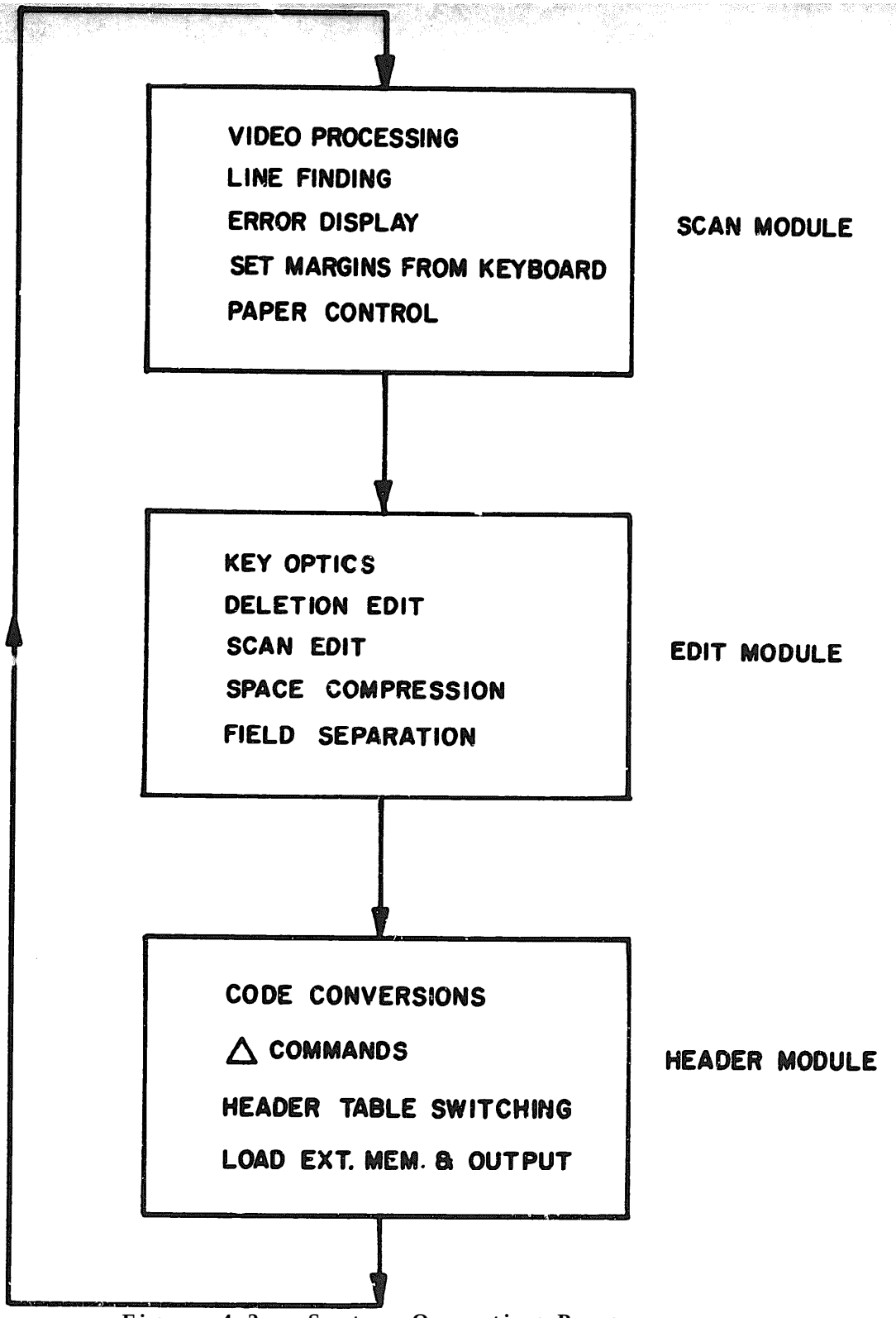


Figure 4-2. - System Operating Program

The Edit Module then receives this data once the entire line has been collected. The Edit Module controls all the correct ion features; Key Optics and Deletion Symbol Editing. The order listed is the order of priority for these operations. The resultant line has all the corrections made and is stored in the Input Buffer portion of the Core Memory. The line is preceded by the code for Beginning of Line and followed by the code for End of Line. These are required for code conversion purposes.

The Header Module controls code conversion operations, responses to @ commands, and Header Sheet loading operations. The line in the Input Buffer of Core Memory is transferred to the Output Buffer portion of Core Memory. During the transfer process the line is transformed from the ASCII code structure used within the machine to the required code structure for the selected Output Device (it may be that the output structure is also ASCII). The result is a Line stored in the Output Buffer portion of Core Memory in the new form. This line is ended with a terminator Call one character) to define its end. This line is now in the form in which it will be output.

The sections which follow describe the operations of the various circuits involved in the performance of the tasks outlined here.

4-2. SERVO CONTROLLER - OVERVIEW. The scanning process requires that the page be positioned for each line and that a Read Head Assembly be moved across the page for each line. These two movements are controlled by the Servo Controller circuits. Two nearly identical circuits are involved. The first is the Vertical Servo circuitry which controls the movement of the page thereby causing each line on the page to be positioned such that the Read Head Assembly can be swept across the line. The second circuit is the Horizontal Servo Controller which controls the horizontal movement of the Read Head Assembly back and forth across the page to scan each line. The two circuits work together to allow each line to be scanned in order starting with the top line on the page.

a. General Operation. - The Servo Controller consists of two nearly identical circuits, one for vertical movement of the paper and one for horizontal movement of the Read Head (R/H) assembly. Since the horizontal section is the more complicated of the two, this description will cover the horizontal circuitry operation first and then the differences wilt be pointed out. The Horizontal Servo Controller Block Diagram, Figure 4-3, illustrates the circuits described below.

The Tri-state Multiplexer selects from among the four sources of control data. These four sources are:

(1) STOP - simply holds the servo in a stop condition thereby causing zero motion of the servo.

(2) VELOCITY (right and left) - two sources, one causing movement at a constant speed to the right, the other to the left.

(3) POSITION - causes the R/H to move at a speed which is proportional to the distance which must be moved and in a direction required to get to the desired position, then to remain at that point,

The Multiplexer will select one of the four sources and output that data to the Digital to Analog Converter (D/A) which creates a signal proportional to the digital input. This signal is amplified by the 2-stage amplifier and fed to the Servo amp. The Servo is mechanically linked to a Tach and encoder which create signals to be fed back to indicate speed and distance of movements. (Refer to figure A-2 for subcircuit operation.)

b. Subcircuit Operation. - There are several subcircuits that may be described before the overall Servo Controller circuitry is covered. These subcircuits are shown on the Servo Controller Block Diagram,. figure 4-3. The subcircuits are:

(1) Tri-state Multiplexer

(2) D/A Converter

(3) 2-Stage Amplifier

(4) Servo Power Amplifier

(5) Encoder & Up/Down Pulse Generator

(6) Stop Control

(7) Velocity Mode Registers

(8) Position Mode Circuitry

(9) Instruction Register

(10) Paper in Position

(11) Bottom Margin Register

(12) Head in Motion

(13) LSTOP and RSTOP Photocell Circuits

The operation of the subcircuit is described in the following paragraphs:

(1) Tri-state Multiplexer (MUX). - The Tri-state Multiplexer, herein called MUX, is not a multiplexer as commonly known. Normally multiplexers are packages which select one of several input lines to be placed on the output line. The Tri-state MUX contains no actual IC packages, but rather is an arrangement of Tri-state outputs which effectively operates as a multiplexer.

The block diagram (figure 4-3) shows four sources of input to the MUX: the Stop control, Velocity mode left, Velocity mode right, and the data selector. Each of these input sources has Tri-state outputs. Tri-state outputs enable each source to either take or relinquish control of the data lines feeding into the D/A section. The data lines from all four sources are tied together. One of the four sources has control of the lines while the other three are effectively disconnected, To change from one source to another, the Tri-state outputs of the one in control are changed such that it relinquishes its control and the outputs of the one taking over control are enabled.

It is this method of always having one source connected to the data lines while the other three are disconnected that causes the circuit to be a multiplexer in nature.

(2) D/A Converter. - The D/A circuit takes digital data and converts it into an analog form required to drive the Servo. The Tri-state MUX transfers data from one of the four sources to the input lines of the D/A. The D/A puts out a voltage proportional to the digital number on its inputs. The greater the digital number the greater the voltage output.

Looking at the actual schematic, it can be seen that the output from the D/A is tied to a voltage divider circuit. This voltage divider is stretched between -12V and ground. It contains a potentiometer which may be adjusted to alter the voltage at the point where the D/A output is tied to the voltage divider. If the digital number on the inputs to the D/A is set to half the value it can reach (MSB high, all others low), the D/A will put out half its possible output voltage. The D/A puts out +1V and the voltage divider is adjusted to balance the junction back to OV. The Servo should be at rest when this condition exists.

When the Servo is to be driven such that the Read Head moves to the right, the digital number on the D/A input lines is changed to a value greater than half (MSB high plus some of the other lines high). The D/A then puts out a voltage greater than IV which, when summed with the voltage from the voltage divider, causes the junction to be positive. This voltage is amplified and fed to the Servo to cause it to rotate and move the R/H to the right. The bigger the number fed into the D/A the more positive the junction and the faster the Servo turns.

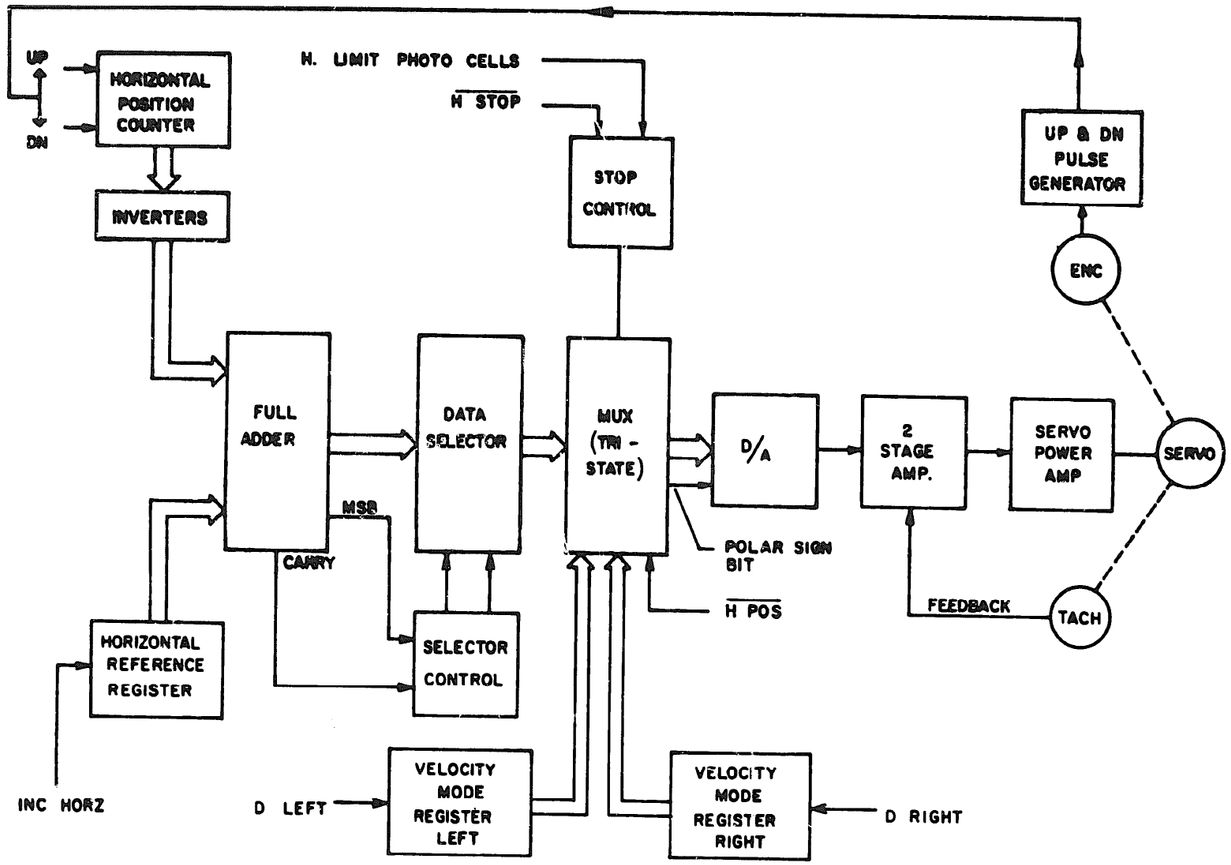


Figure 4-3. - Horizontal Servo Controller Block Diagram

When the Servo is to be driven such that the R/H moves to the left, the digital number on the D/A input lines is changed to a value less than half (MSB low plus some other bits high). The D/A then puts out a voltage between 0V and +1V which when summed with the voltage divider causes the junction to go negative This voltage is amplified and fed to the Servo which rotates and moves the R/H to the left. The smaller the number fed into the D/A, the more negative the junction goes and the faster the Servo turns.

The D/A can be seen to control the speed and direction of movement of the Servo. The movement may be defined by the following relationships.

STOP	MSB high, all other bits low
RIGHT	MSB high, some other bits also high. The greater the digital input to the D/A the faster the Servo turns.
LEFT	MSB low, some other bits high. The smaller the digital input to the D/A the faster the Servo turns.

(3) 2-Stage Amplifier and Tach. - The 2-Stage Amplifier consists of two operational amplifiers. The first stage amplifies the voltage that was created at the output of the D/A by approximately 5 times. This amplification takes place without inversion so the output goes positive for righthand motion of the R/H and negative for lefthand motion.

The second stage of the amplifier provides amplification, but it also provides a means of detecting whether or not the Servo is moving at the desired speed and in the proper direction. If not, the output is adjusted to correct the speed until it is correct.

Attached to the Servo is a Tach which generates a voltage proportional to the speed (higher speed equals greater voltage) and with a polarity indicating direction <negative for righthand and positive for lefthand motion). When the Servo is to be moved, a voltage is created at the output of the first stage indicating speed and direction. This is amplified by the second stage to provide a signal to the Servo. As the Servo responds, the Tach creates a voltage indicating that the Servo is moving, the direction and speed. This information is compared with the desired movement signal and the output adjusted to achieve proper speed and direction,

(4) Servo Amplifier. - The Servo Amplifier converts the op-amp output from the 2-stage amplifier to the high current drive required by the Servos. The amplifier is contained on a plug-in heat sink assembly. An octal plug on the base of the assembly mates with an octal socket allowing easy insertion and removal of the entire assembly. Four screws hold the assembly in place. The op-amp and transistors are individually mounted in sockets providing for easy replacement of these individual components.

The amplifier has the output from the 2-stage amplifier applied to the inputs of U1. The signal applied to U1-2 is inverted and appears on the output of the op-amp, U1-4. This signal will cause the transistors Q1 & Q2 to increase or decrease conduction depending on the signal amplitude and polarity. The output from Q2 will control whether the positive or negative portion of the subsequent circuitry has control of the output to the Servo. The Servo has one side grounded, and the amplifier provides a positive or negative voltage to the other side. The polarity and amplitude determines speed and direction of Servo rotation.

For a zero drive condition, the op-amp U1 must output a voltage sufficient to turn Q1 & Q2 on enough to keep the emitter of Q2 between +.6V & +1.2V. This range of voltages will keep Q5 from conducting, thus no positive voltage appears on the amp output, pin 4. The voltage at Q3 base will be between -1.8V & -1.2V. This will keep Q3, Q4, & Q6 from conducting, thus no negative voltage will appear at the output, pin 4.

If U1-4 starts going more positive, Q1 & Q2 increase conduction. The emitter of Q2 goes more positive, turning Q5 on proportional to the voltage increase at U1-4, The base of Q3 is also taken more positive which just keeps Q3, Q4, & Q6 off. The output of the amp is therefore a positive voltage.

If U1-4 had gone more negative, the emitter of Q2 would have gone more negative also, thereby holding Q5 off. The base of Q3 would have gone more negative causing Q3, Q4, &

Q6 to turn on proportional to the voltage decrease at U1-4. The output of the amp will go low causing the Servo to turn the opposite way.

(5) Encoder and Up Down Pulse Generator. - The Encoder and Up/Dn Pulse Generator work in conjunction to provide a series of pulses indicating direction and distance of travel. Mechanically linked to the horizontal and vertical drive mechanisms is an encoder which creates two square wave signals 90 degrees out of phase with each other. The direction of rotation determines which of the two phases leads the other. The phase that is leading determines whether UP or DOWN pulses are issued. These pulses are used by the Horizontal Position counter to keep track of Read Head movement and by the Vertical Position counter to keep track of page movement. The two Pulse Generator sections (vertical and horizontal) are identical.

The timing diagram (figure 4-4) shows the relationship of the two square wave signals from the encoder. The diagram shows that Up pulses are generated when phase 2 leads and Down pulses generated when phase 1 leads-

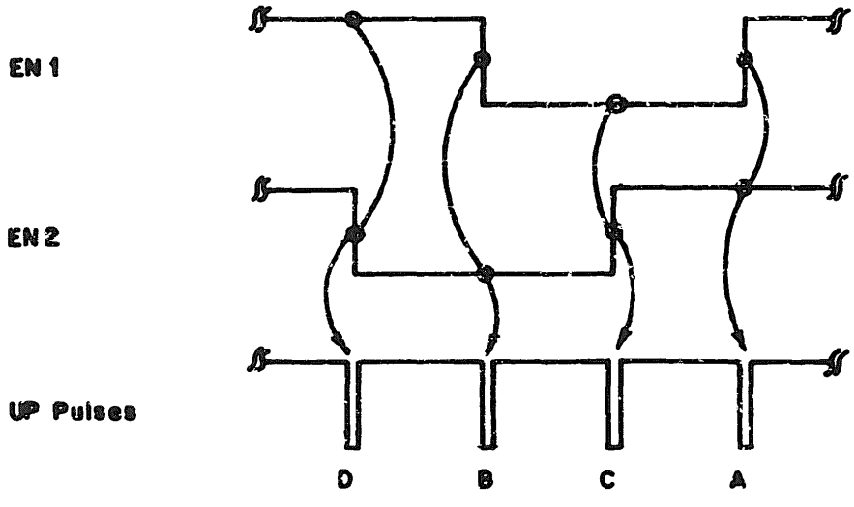
The Horizontal Encoder pulses (HEN1 & HEN2) are double buffered and inverted by ICs 2K & 4A. This provides both the true and inverted form of the signals. These four signals are fed to D-flops 1L & 3L which are positive edge triggered. Let's take the condition where EN2 is low and EN1 has a low going edge. This is condition B on the Up count section of the timing diagram. The Up decoder is 2L-8, 9, 10 marked B.

When HEN2 is low, HEN2(not) is high at 2L-10. HEN1 going causes HEN1(not) to go high at 1L-11 causing 1L-9 to go high and 1L-8 low, 3A-8 high, and 1F-6 Lou causing 1I-8 to go low This low feeds back to 1L and resets it. The output at 1L is a short pulse which passes to 2L-9. Since 2L-10 is high the pulse passes through to the output. In the horizontal section, this sets another set of flip-flops which ultimate creates the horizontal up signal. For horizontal down, vertical up, and vertical down the outputs from the NAND gates directly create the respective signals. The Next Up pulse will be created by a section of 3L setting and reset then IL again, etc.

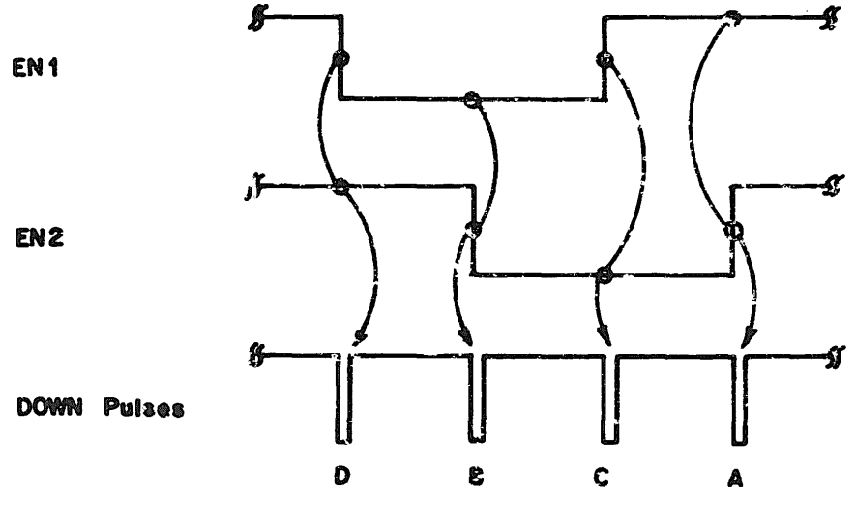
(6) Stop Control. - The Stop Control circuit take control of the input lines to the D/A whenever the R/H is to be at a stop. Whenever the Velocity Mode and Position circuits relinquish control of these input lines the Stop takes over and forces the Most Significant Bit high and the other 7 lines low. This is the defined state for stop or Servo movement.

There are four conditions which will cause the Stop Circuitry to take control of the D/A inputs. These four cond are ORed together at PC 13R. Any of the following will ca stop to take over:

(a) HSTOP(not) at 20S-1 is a signal generated by the horizontal instruction decoder. It goes low in response to an instruction issued by the Executive Macro requesting the Read Head be stopped.



	D	B	C	A
HOR.	4L-8	2L-8	2I-8	1K-8
VERT.	4L-3	2L-3	2I-3	1K-3



	D	B	C	A
HOR.	4L-11	2L-11	2I-11	1K-11
VERT.	4L-6	2L-6	2I-11	1K-6

Figure 4-4. - Pulse Generator Timing Diagrams

(b) A stop condition is detected by 20L-2 which will go low if the R/H is being driven to the right and the right stop photocell. is covered. This condition would indicate that an attempt is being made to drive the R/H too far right.

(c) A stop condition is detected by 22T-11 which will go low if the R/H is being driven to the Left and the Left stop photocell is covered. This condition would indicate that an attempt is being made to drive the R/H too far left.

(d) A stop condition is detected at 22S-12 if an attempt is being made to move the R/H via position mode and either of the two photocells is covered. This condition indicates that an attempt is being made to move the R/H to a position outside the limits of travel.

If one of these four conditions occurs, the output of 13R-8 will go high and 14R-10 will go low. This causes all the outputs of 27I and 26I to be enabled. The inputs 26I-5, 9, 12 are low because the circuit is not in a drive left condition. Inputs 27I-5, 9, 12, and 26I-2 are tied to ground. Input 27I-2 is high because 21L-2 is Low. The combined result is that the HDA1-7 lines are held low and HDA8 is held high, the defined state for stop.

(7) Velocity Mode Registers. - There are two Velocity Mode Registers, one to control the velocity during movement to the right and one for movement to the left. The speed at which the R/H will move during each mode is controlled by each of these registers:

Drive Right is controlled by register 31K plus parts of 27I and 26I. Prior to processing the page, a value is loaded into the Velocity Mode Register defining the speed at which the R/H will move whenever it moves to the right. When the R/H must move to the right, the Velocity Mode Register is enabled via a low on its chip select lines (pins 1 & 2). This low enable signal causes the register to take control of the MUX lines. This same signal also causes several other things to happen. It causes 20M-12 to go high, 28M-4 to go low, and the Tri-state outputs 26I-6, 8, 11, and 27I-3 to be enabled. It also causes 21L-3 to go high. The result is that the HDA1-3 lines are held low, the HDA4-7 lines are controlled by the register value, and the HDA8 line is held high indicating Drive Right.

Drive Left is controlled by register 31L plus parts of 27I and 26I. When the R/H is to be moved to the left, the chip select lines on 31L (pins 1 & 2) are taken low causing the register to take control of the HDA4-7 lines. This same signal causes 20M-12 to go high, 28M-4 to go low, 28M-6 to go low, and Tri-state outputs 26I-6, 8, 11, and 27I-3 to be enabled. The result is that the HDA1-3 lines are held high, the HDA4-7 lines are controlled by the register value, and the HDA8 line is held low indicating Drive Left.

(8) Position Mode Circuitry. - The Horizontal Position Mode circuitry consists of several registers, inverters, an adder, and data selectors. The circuit has two purposes:

(a) To control the movement of the Servo n order to position the R/H to a specific position on a line and hold it there such as during Key Optics stops.

(b) To detect that the R/H has reached a specific point on a line such as Left or Right Margins.

The different sections of the circuit may be identified as follows:

Horizontal Position Counter - 24L, 25L, 30M, 26L

Horizontal Reference Register - 32M, 32L

Inverters - 21M, 31M

Full Adder - 32I, 32K

Data Selector - 31I, 30I

Tri-state Outputs - 28I, 29I

The Horizontal Position Counter is responsible for keeping track of the actual position of the R/H as it moves back and forth across the line. As the R/H moves the Encoder and Up/Down Pulse generator circuit create Up pulses indicating movement to the right and Down pulses indicating movement to the left. The Horizontal Position Counter is therefore counted up by movement to the right and down during movement to the left= The resulting number in the counter may be considered to be a position number on the line. The zero mark may be the left edge of the page being scanned or may be the left stop photocell depending on the operation being performed. Negative positions are not possible.

The Horizontal Reference Register is loaded to a value indicating the position on the line which is being sought, This position may be sought after in order to position the R/H at that point or the Executive Macro may simply be checking to see when the R/H crosses that point by testing the LT/RT Margin.

The Adder and Inverters create a subtractor which subtracts the number in the Position Counter from the value in the Reference Register. The result is a number indicating the size of the difference between the two numbers and a sign indicating which number is the larger number. If the result is a positive number, then the Position Counter value is smaller than the Reference Register value and the R/H is to the left of the desired position. If the result is a negative number, then the Position Counter value is greater than the Reference Register value and the R/H is to the right of the desired position,

The output from the Adder is fed to the Data Selector. Bits 1-7 pass directly across to the selector, The 8th bit, the most significant bit, along with the carry output (32K-14) feed into several gates which form the control network for the Selector. The Data Selector (ICs 31I & 30I) is capable of passing the data without change, outputting all zeroes, or outputting all ones regardless of the inputs. The control inputs B & C determine which situation occurs as follows:

MSB	CARRY	B	C	OUTPUT
0	0	1	1	All lows
1	0	0	1	Bits 0-7 true value
0	1	0	1	Bit 8 equal to carry
1	1	1	0	All highs

The B & C control lines to the Data SeLector are a product of the Most Significant Bit of the Adder (32K-15) and the Carry Out Line (32K-14) which are the result of the two numbers being subtracted. This arrangement causes the Servo to be driven at maximum speed when the two numbers differ greatly and at a proportional speed when the numbers approach each other. The outputs are passed through Tri-state gates 28I and 29I, When the Position Mode is selected, the Tri state outputs take control of the MUX lines and control Servo speed and direction.

The Position Mode Circuitry has another purpose also. During the scanning process on a page the Executive Macro must determine when margins have been crossed by the R/H. The Drive Right mode has control of the Servo movement, but the Horizontal Position Mode section is keeping track of the R/H movement and position. The Carry output from the Adder (32K-14) is also known by the signal name LT/RT MARG. When this line changes from low to high, the Position and Reference Counters have just crossed coincidence with each other, meaning that the R/H has just arrived at the desired position. The Executive Macro then takes suitable action for the margin crossed,

(9) Instruction Decoder- - The Instruction Decoder consists of three sections, a series of buffers for the instruction register lines, three pulse decoders, and two latch circuits.

The buffer section consists of parts of ICs 18R, 18T, and 18S, These buffers and drivers provide buffering for the instruction register lines and drive the lines for the rest of the circuitry.

The pulse decoders are connected to the instruction register lines IR8, IR9, IR10), and IR11 plus the instruction Load Mechanism. The three resultant signals are LRS (load Tight speed), LLS (load left speed), and LVS (load vertical speed). These three signals load the values into the velocity mode registers.

The latch circuits are in two parts, 19s and 20s for horizontal instructions and 19T and 20T for vertical instructions. The load mechanism signal plus IR8 for horizontal or IR9 for vertical loads the IR12, 13, 14, 15 bits into the respective latch. These are decoded as the control signals for the various horizontal and vertical modes of operation.

(10) Paper in Position (figure A-1). - This circuit is used to detect when the paper is not in motion and is therefore assumed to be in position for the scanning of a line. The circuit consists of a one-shot (18L-12) which monitors the vertical up and down pulse lines. Since up pulses are issued whenever the paper is moving up, and down pulses during downward motion, if neither of the pulses is being issued it may be assumed that the paper is not in motion, therefore it is in position, When the Servo is moving the paper, one of these

two pulses will be occurring. As soon as the first occurs the one-shot is triggered causing the Q-not output (18L-12) to go low. The one-shot will start timing out, When the next pulse is detected the one-shot is retriggered and starts timing the full period again, The Q-not output remains low. When the up/down pulses finally stop occurring, the one-shot will have adequate time to time out and the Q-not output will return high indicating that the paper has stopped moving and is in position.

(11) Bottom Margin Reference Register. - The Bottom Marg Reference Register consists of two 74193 counters (16Z and 17Z). These registers will be incremented by the Executive Macro via the instruction "INC6". The value it will be incremented to will be the value of the bottom margin as set by the operator. The bottom margin register outputs are fed into the comparator 18Z and 19Z. The comparator compares the value in the bottom margin register with the value in the vertical position register- When these values are equal, the signal "CMP" will go high. "CMP" is fed to an Executive Macro test gate to alert the Executive Macro that the scanning of a page has reached the bottom margin and the page is finished. The Executive Macro will clear the bottom margin register via the instruction "RESET 5."

(12) Head in Motion, - The Head in Motion circuit is used to detect when the R/H is moving, The circuit consists of a one-shot (18L-13) which monitors the horizontal up/down

pulse lines, Either of these pulses will trigger the one-shot causing the output (18L-13) to go high indicating that the R/H is moving. Once the pulses stop, the one-shot will time out and 18L-13 will return tow indicating that the R/H has come to rest. The Head in Motion signal is monitored by the Executive Macro so that it knows when the R/H is moving or stopped.

(13) Lstop and Rstop Photocell Circuits. - The Lstop and Rstop Photocell Circuits are used in conjunction with the stop circuitry described earlier, Whenever the R/H reaches the end of travel a tab on the R/H assembly blocks the light being directed at a photocell. There is an infrared LED and photocell at each end of the scanning area; the one on the right known as the right stop photocell and the one on the Left as the Left stop photocell. When the light shining on the photocell is Mocked, the internal transistor turns off, thereby indicating that the end of travel has been reached.

The Rstop circuit consists of the LED photocell, two resistors, and an inverter 20L-1, 2. The light is connected between ground and the output line designated as RIR. The RIR output is a DC voltage from the 100 ohm resistor between R/F5 and 6. The photocell is tied between ground and the RPC Line, This line (right photocell) will be pulled high by the 10K resistor (R/F7-8) when the Light on the photocell is blocked and the transistor turns off. The circuit output, Rstop(not) at 20L-2, will go low, indicating that the R/H has reached the end of its allowable travel. When the R/H is not

at the right end of travel, the photocell will not be blocked, the RPC line will be low because the transistor is on, and the Rstop(not) output will be high,

The Lstop output works the same as Rstop, just the component numbers differ,

c- Servo Controller Program Operation. - The Servo Controller Circuitry consists of two sections as previously mentioned, the horizontal and vertical sections.

The horizontal portion controls the movement of the R/H assembly back and forth across each page to scan the characters on each line. Movement and positioning of the R/H is achieved through the use of the various modes of operation described earlier. Normal scanning uses the Velocity Mode (Drive Right and Left) to move the R/H at constant velocities. The Position Mode is used to move the R/H to a specific position on a line and hold the head at the point in order to place the pointer beneath a character during Key Optics stops. When no movement is required, the Stop circuit simply holds the R/H at whatever position it is at. All the movements are under the control of the Instruction Register which receives its directions from the Executive Macro.

The vertical portion controls the movement of the paper into the machine. It differs from the horizontal section in that it has only one velocity register, Since the page will only be moved into the machine, no register is required to control movement in the outward direction. The velocity made moves the

page forward at a constant speed such as when the page is being ejected, or first being brought in. The Position Mode controls the movement of the page required to position the first and each subsequent line beneath the R/H so it may be scanned. The Stop Mode holds the page where it is whenever the machine is in Standby,

The combined effect is that the first line is positioned beneath the R/H and the R/H is moved across the page from left to right. If there are no questionable characters in the line, the R/H is moved back to the Left and the page is moved up to the second line, The R/H then is moved across the line. If a questionable character causes a Key Optics stop, the R/H will be moved by the Position Mode circuit to point out the questionable character. When the operator has taken suitable action, the process of scanning resumes.

4-3. VIDEO ACQUISITION - OVERVIEW. - Video acquisition consists of those processes whereby the data contained on each typed line is scanned and collected in a raw form and made available to the next circuit,

The main process is known as SAMPLING wherein a Read Head Assembly containing a vertical column of 128 photodiodes is mechanically moved across a line from left to right. As the column is moved across the line,, the diodes are sequentially strobed at regular intervals to provide vertical samples of that portion of the page beneath the Read Head, The Read Head

Assembly contains a high intensity light source which is focused onto the area of the page beneath the diode column, When the column is over a blank white area of the page, all the diodes will have bright light reflected onto them by the page. However, when the column is over a character, some of the diodes will not receive strong reflected levels of light since the black portions of the character do not reflect the light.

Video acquisition takes many samples of each character. Each sample is in effect a vertical slice of the character which is beneath the Read Head. These slices of the character will eventually be reassembled into a matrix which can be compared with each of the characters in the Reference Alphabet. The reassembly is a function of the video processing circuitry and the comparison is a function of the character identification circuitry, The video acquisition circuitry is responsible only for taking the samples and forwarding them to the video processing section. (See Figure 4-5, Video Acquisition Block Diagram.)

a. General Operation. - The video acquisition circuitry consists of several sections. The first section is a Timing Generator which creates the master clock for this section, divides the clock by 8 for use on the Analog Card, and creates a tiring chain for use by the video addressing circuit,

The second section is the Analog to Digital Conversion circuitry which employs a column of photodiodes to detect the presence or absence of reflected light from the scanned pages-

FIGURE 4-5. VIDEO ACQUISITION BLOCK DIAGRAM

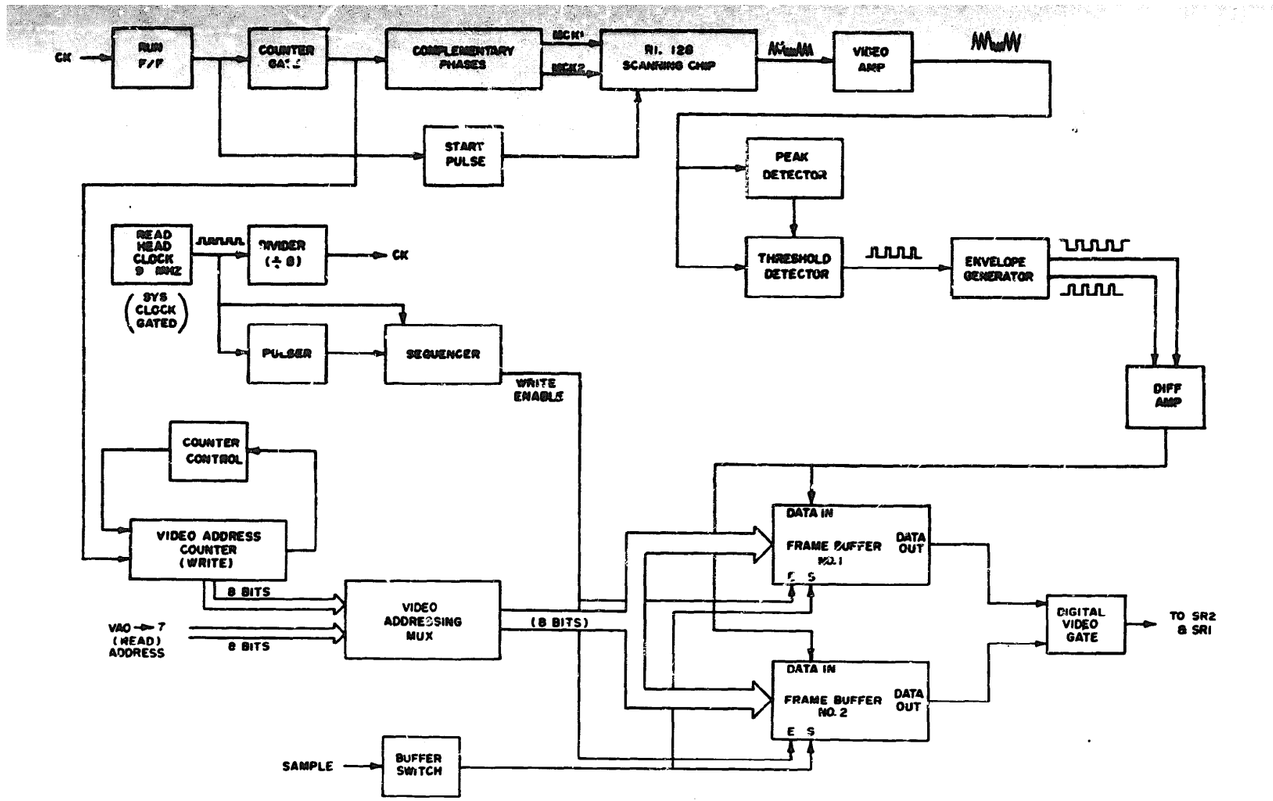


Figure 4-5. - Video Acquisition Block Diagram

That data is converted to a series of zeroes or ones (digital data) which can be handled by subsequent circuits.

The other sections work together to store the data being forwarded from the conversion circuitry. As the diode column is passed over the tine of characters on the page, each of the 128 diodes in the column is sequentially selected and the determination made as to whether that diode is above white or black. The status of each diode is stored in a 128 bit RAM (Frame Buffer) with the RAM address corresponding to the diode number. Tie video write addressing circuit coordinates this entire process by selecting diode number one and RAM address one, writing the diode status into the RAM, selecting diode two and RAM address two, writing, selecting three, etc. The video addressing circuit and the Frame Buffers do one other thing. There are two Frame Buffers each consisting of a 128 bit RAW. This allows the video write addressing circuit to be writing into one Frame Buffer while the prior sample is being read and transferred from the other buffer to subsequent circuits. When the prior sample has been transferred and the current sample has been fully collected, the function of the two Frame Buffers is exchanged.

b. Subcircuit Operation. - There are several subcircuits that may be described before the overall video acquisition process is covered. These subcircuits are:

(1) Timing Generator

(2) Analog to Digital Conversion Circuitry

(3) Video Write Addressing Circuitry

(4) Video Addressing Multiplexer

(5) Frame Buffers

(6) Paper Detect Circuitry

The operation of the subcircuits is described in the following paragraphs:

(1) Timing Generator (Fig, A-5). - The Timing Generator circuitry is located on the Read Head Digital Card (J40). It consists of the packages U1, U5, U4, and U6. (See timing diagram, Figure 4-6, for the following explanation.)

TP8 is a 9 MHz gated system clock which provides the master clock frequency for this circuitry. U6 is a four-stage binary counter, The 9 MHz clock is fed to the UP clock input and the output is taken from the Qc output. This divides the 9 MHz by 8 with the result being two signals CK and CK(not) running at 1.125 MHz. These two signals will be used by the video addressing circuitry.

The two halves of U4 plus U5 create a timing chain which issues two pulses, WRITE ENB and RESET V/H(not). The timing chain repeats itself every 8 chock pulses. The process is as follows. The numbers in parenthesis refer to numbers on the timing diagram.

The 9 MHz clock is fed to the clock input of J-K flip flop U4. However, the clear input on both halves of U4 is held low by the signal CK preventing U4 from setting except when CK is high. The signal CK will be high for 4 clock pulses and low for 4. As shown on the timing diagram, figure 4-6, CK will go high on the trailing edge of the fourth clock pulse. These same 4 clock pulses were fed to the toggle input

of U5-8 which is an 8-stage shift register. The data input has been held low by U4, pin 5, so that the data shifted into the first four stages has been zeroes. Since CK is high removing the clear clamp from U4, the next negative going edge of the clock (TP8) will set the first stage of U4 (1). The input to the shift register, U5-8, is therefore high and the next positive transition of the clock will transfer a one into the first stage of the shift register (2). The next negative going edge of the clock will reset the first stage of U4 (3) which will cause the second stage of U4 to set (4).

The next positive edge of the clock will cause two things to happen. Since the first stage of the shift register is set, the positive transition of the clock will cause the second stage of the shift register to be set (5). Also at this time, since the first stage of U4 is reset, the clock toggles a zero into the first stage of the shift register (6).

Each positive edge of the clock will cause the one bit which is set in the shift register to move one position to the right. Thus there is always one and only one bit set. This bit is shifted through the register until it shifts out the end as a new one is shifted into the first stage?. This Creates an 8 bit sequential timing chain of which only two bits are used; one for WRITE ENB and one for RESET V/H.

When the signal CK returns low, it resets the second stage of U4 and the circuit is back at the starting conditions (7).

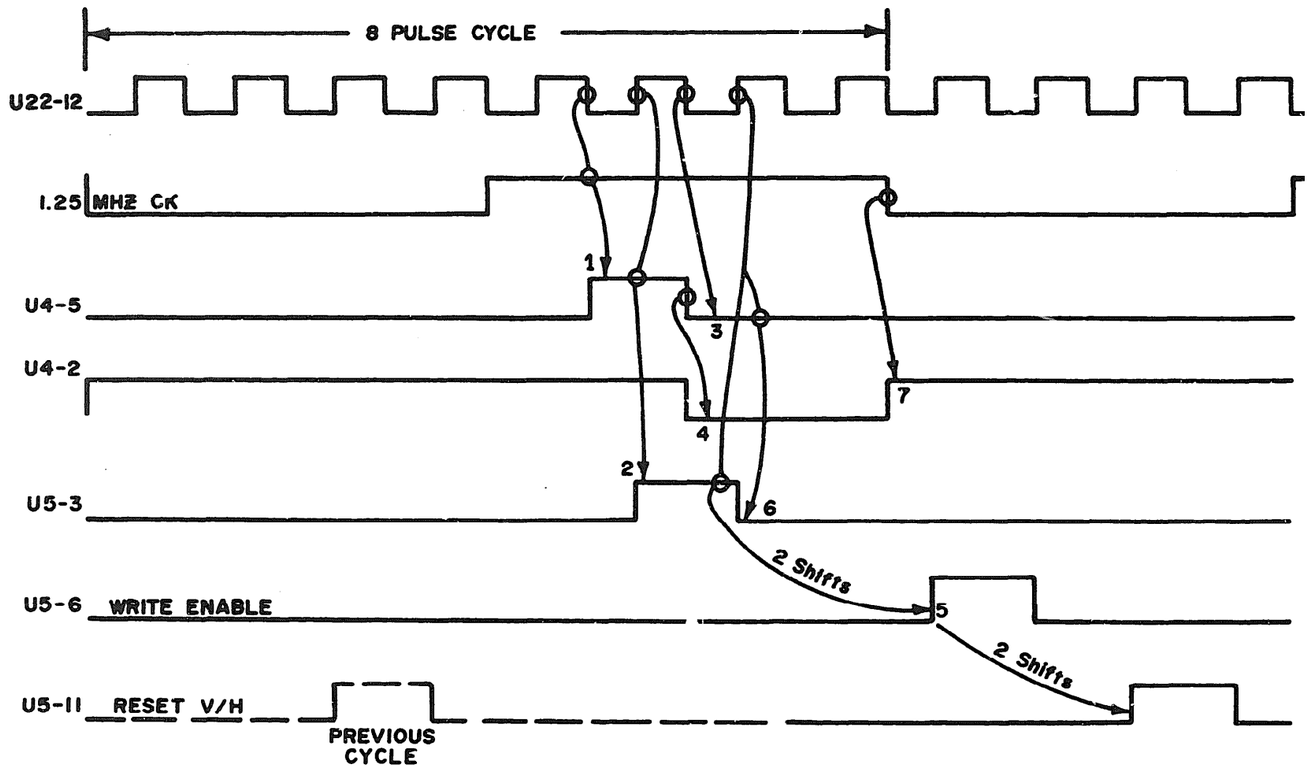


Figure 4-6. - Video Acquisition Timing Generator

(2) Analog to Digital Conversion Circuitry (Fig. A-4). - The Analog to Digital Conversion Circuitry amplifies the Read Head analog data, distinguishes between video levels generated by light and dark areas of the page, and converts this analog data into a digital form which may be handled by subsequent circuitry. The block diagram, figure 4-7, for the A/D Conversion Circuitry shows the major components of the circuit.

The Reticon Chip, U4, is en assembly of 128 photodiodes in a column, Each of the diodes may be sequentially interrogated to determine whether it is receiving high or low levels of reflected light from the page, The higher the level of reflected light, the higher the output voltage from the Reticon Chip. The output from the Reticon is amplified by U5. The resultant signal is a series of high and low pulses corresponding to the light levels on each of the diodes as they are strobed. This signal is passed to a Peak Detector circuit composed of a diode, capacitors and op-amp U7. When the output from U5 goes high, it charges the capacitor through the diode to a voltage close to the highest peak being output from U5. Since the input to the op-amp U7 is a high impedance, the capacitor will discharge very slowly. The output from U7 is a voltage equal to the voltage on the capacitor, Since the capacitor discharges very slowly, this voltage will be maintained close to the peak output voltage of U5.

The Peak Video signal from U7 is fed into a voltage divider circuit. A potentiometer in the divider allows a portion of the peak voltage to be selected and fed into one of the inputs

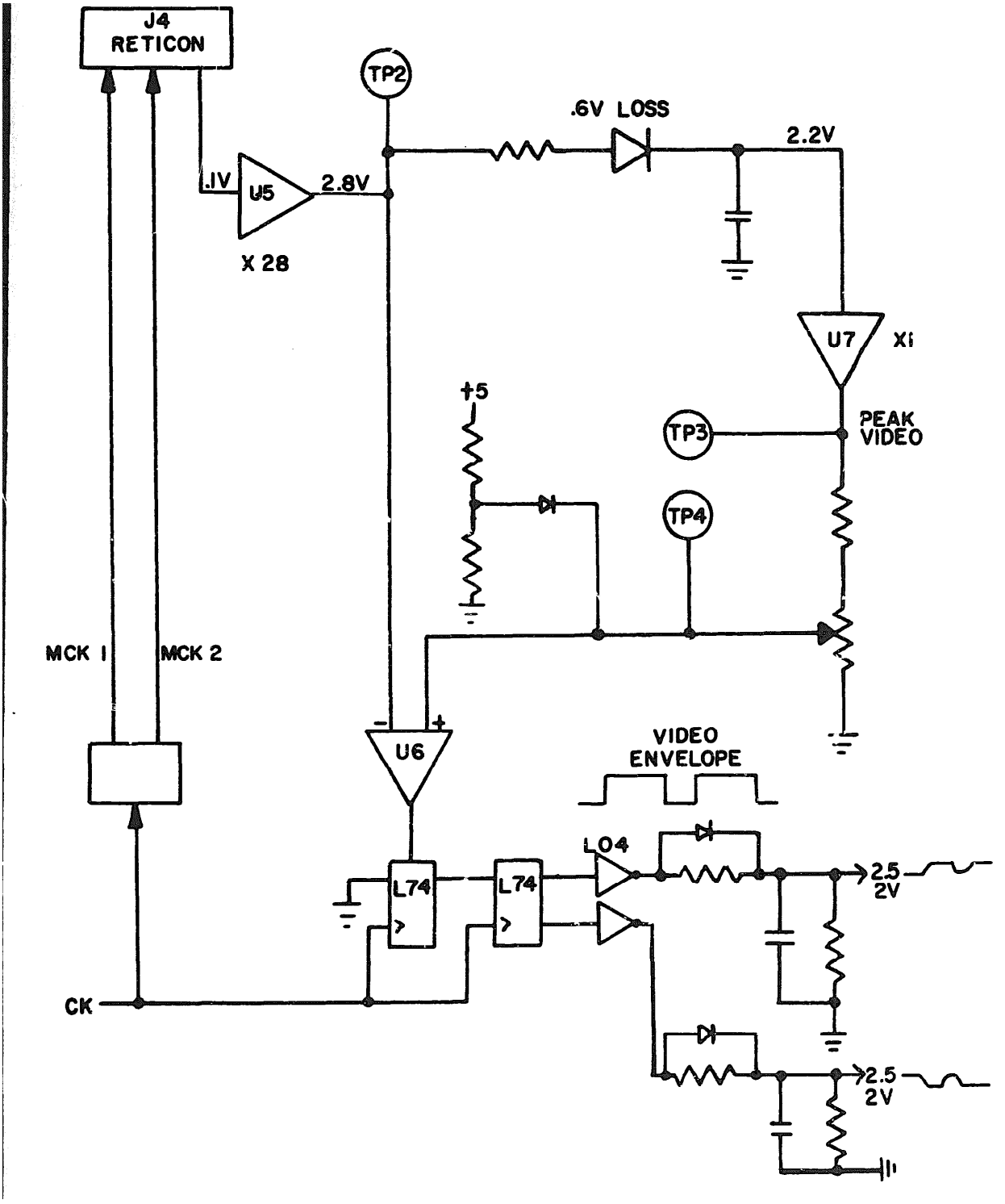


Figure 4-7. - Analog to Digital Conversion Circuitry Block Diagram.

on the voltage comparator U6. The other input to the comparator is the signal from the first amplifier, U5. Since U6 is a comparator, it has only two output states, high or low. The input to the comparator from the voltage divider is set to be approximately 2/3 of the peak voltage at TP2. The result is that the output from U6 will be low whenever the voltage at TP2 is higher than the voltage selected by the potentiometer. The output from U6 will be high when TP2 is lower than the potentiometer voltage.

U6 therefore determines which voltages at TP2 will be COW sidered to be high (high reflection from white area) and which voltages will be considered low (low reflection from dark areas). The reference voltage is selected by the potentiometer.

An important aspect of this circuit is that it accounts for differences in the levels of reflected light due to lamp aging or paper differences. If the level of reflected light decreases, the output from U5 will decrease. However, the Peak Video level detected will also decrease causing the picked off voltage at the potentiometer to lessen, When the signal at TP2 is compared with the new reference voltage, the same 2/3 ratio is maintained, thus no digitized video changes are caused.

(3) Video Write Addressing Circuitry (Fig. A-5). - The Video Write Addressing Circuitry counts from 0 to 127 such that the Frame Buffers U23 and U25 are addressed in sync with the photodiode scanning pattern. To achieve synchronization, a start pulse must be issued, Then a series of clock pulses is fed to the Reticon Chip on the Read Head Analog Board and to the Video Write Addressing Counter on the Digital Board. Each clock

pulse causes the next sequential diode in the Reticon to be selected and the data from that diode to be written into a corresponding address in one of the Frame Buffers as selected by the Video Write Addressing Counter.

Since the Video Write Addressing Circuitry operates in a free-running fashion, there is no starting point for the process. Therefore, for this discussion. a point shall be selected with defined conditions and the circuit operation explained until the circuit returns to the defined starting point. The diagram on figure 4-8 will aid in the understanding of the explanation. The letters in parenthesis in the explanation refer to the identifying letters on the timing diagram.

The point that shall be selected is where the addressing counter (U12 and U13) has a va1ue of 127. At this time, FF1 (U11) is clamped reset, FF2 (U3-5) is set, and FF3 (U3-3) is reset. With FF2 set, the clock CK is passed through (U2-8) to create the signal Scan Counter Clock (A) and (B). The next positive edge of CK sets the addressing counter to a value of 128 (c). When the 128 bit goes high, the reset clamp is removed from FF1. The combination of 128 set plus the next negative edge of the clock CK causes FF1 to set (D). When FF1 sets, FF2 is forced reset (E) and the address counter is placed in the parallel load condition by pin 11 being taken low. The inputs to the counter are all high except the least significant bit, therefore, the counter is loaded with a value of 254 (F). When FF2 was forced reset, its output forced the

Scan Counter Clock high and inhibited further clock pulses from being generated (G). The next negative transition of the clock CK causes FF1 to reset (H) thereby removing the clear from FF2 and the load from the counter. The next positive transition of the clock CK sets FF2 (I) which in turn causes FF3 to set, generating RStart (J). Since FF2 is set, the clock again creates the Scan Counter Clock (U2-8) (K), the first negative edge of which sets the count to 255 (L), The next negative edge after that sets the count to 0 (zero). With the counter set to zero, the negative transition of the clock CK will cause FF3 to reset (M) thus ending the RStart signal. When Scan Counter Clock next goes low it will cause the two phases of the clock to the Reticon Chip (MCK1 and MCK2) to switch (N).

Thus the address counter is counted from 0 to 127 and then reset while a simultaneous clock is fed to the Reticon Chip a long with the synchronizing start pulse.

(4) Video Addressing Multiplexer (Fig. A-5). - The Video Addressing Multiplexers, U14, U16, U15, U17, control the address lines to the two Frame Buffers, U23 and U25. Each Frame Buffer has a multiplexer feeding its address lines. Each multiplexer is able to select either the address created by the Video Write Addressing Counter, U13 and U12, or the Read Address created by a counter in the Video Processing Circuitry. The Video Write Address Counter supplies the address during the write process when the data from the Analog to Digital Conversion Circuitry is being written into a Frame Buffer. When the

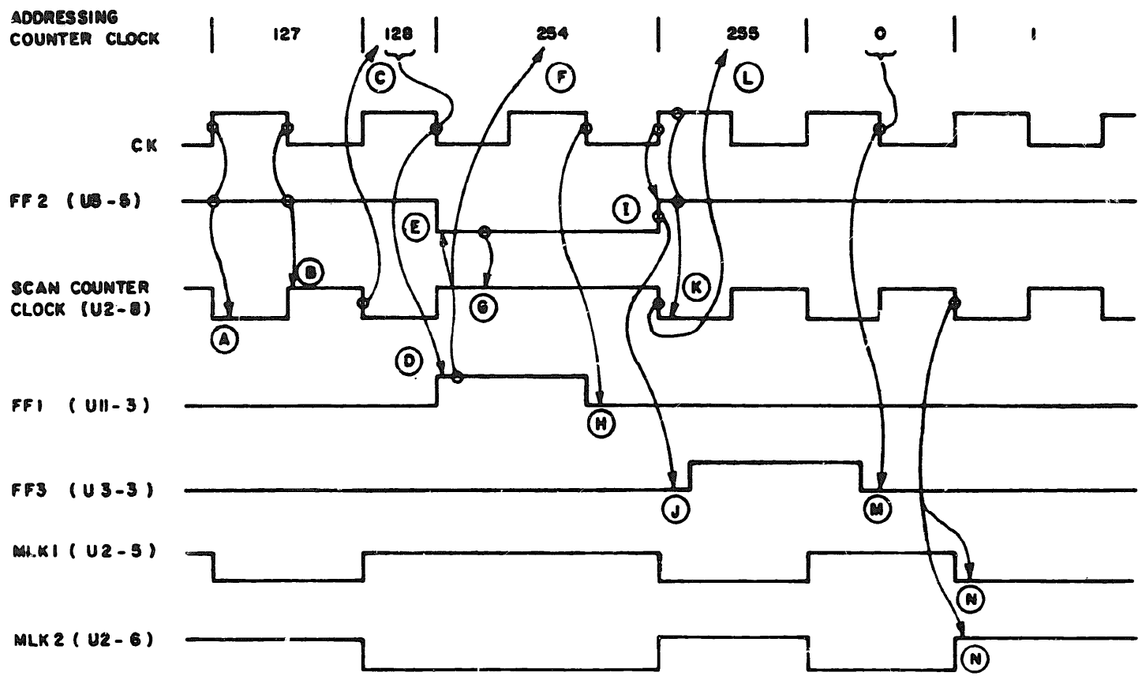


Figure 4-8. - Video Addressing Timing Diagram

data has been collected, it must be transferred to the Video Processing section. During the transfer process, the Video Processor provides the Read Address via the multiplexer to control the locations from which the data will be read.

The multiplexers thus select the appropriate address source for each Frame Buffer depending on whether the intention is to write into or read from the particular Frame Buffer.

(5) Frame Buffers (Fig. A-5). - There are two Frame Buffers, U23 and U25, which are used to collect the individual samples from the Reticon Chip. The digital data from the Analog to Digital Conversion Circuitry is applied to the Data In (DI) input on both Frame Buffers. However, only one of the two will receive a Write Enable (WE) signal, The RAN Switch (U7, pins 2 and 3) controls which of the two buffers will receive the Write Enable signal. Each time the timing generator issues a Write Enable signal, the selected Frame Buffer will have the data written into it at the address determined by the Video Write Addressing Counter and Multiplexer. The next address and next diode in the Reticon will then be selected and the resultant data written into the buffer.

At the same time that the Buffer Switch selects one Frame Buffer as the buffer into which data will be written, the alternate buffer has been designated as the buffer from which data will be transferred to the Video Processing section. This is achieved by enabling one of two nand gates which feed into a Nor function (U24, pins 1 and 2). The data from the selected

buffer is then passed to the Video Processor as the signal RH Video(not).

(6) **Paper Detect Circuitry (figure A-5).** - The Tentative Paper Present/Paper Present circuitry operates as follows:

(a) Hit Start, program issues DLEFT which clock U7-6 low forcing TPP high. This enables 2F and 2E-3, which generate PAPER PRESENT after 2F counts up, about 2 msec.

(b) Read Head reaches left stop, LSTOP generates TPPR which resets U7, causing TPP low.

(c) The Read Head drives right, to the center of the carriage and enters Position Mode. When paper comes under the head, or if it was already there, U20 will count 16 lite bits and fire the one-shot U19. This disables U2-11 generating TPP. After about 2 msec PAPER PRESENT is generated. Also, 2E-6 is reset.

(d) The Read Head drives left to the left stop. During this time U7-6 keeps TPP and PAPER PRESENT high.

(e) At the left stop, LSTOP generates TPPR which resets U7, causing TPP low and PAPER PRESENT low.

(f) As the Read Head drives right, at the edge of the paper U20 and U19 will generate TPP and PAPER PRESENT high.

(g) At the right margin the head will immediately drive left. U7-6 will force TPP and PAPER PRESENT high while driving left.

(h) About .2" off the left side of the paper the Read Head will drive right. 2E-6 will go low generating TPPR, resetting U7-6 low, causing TPP and PAPER PRESENT to go low until the Read head moves over the paper.

(i) At the edge of the paper U20 and U19 generate TPP and PAPER PRESENT high, 2E-6 resets.

(j) Steps g-i repeat for the rest of the sheet.

NOTE: The delay between the time that TPP is active to when PAPER PRESENT is active is about 2 ms or about .030" of Read Head travel.

When TPP is lost, U19 takes about 1.5 msec to time out after the edge of paper.

c. Circuit Operation (Figs. A-4 and A-5). - The Video Acquisition Circuitry is continually taking and storing samples when the Read Head is driving left. The dual phase clock (U2, pins 5 and 6) constantly selects the sequential diodes of the Reticon Chip. The output from the diodes is amplified and digitized by the Analog to Digital Conversion Circuitry.

In order to determine when the Read Head is over paper, a circuit counts the number of diodes that see white during each 128 diode sample. When the total reaches 16 or more within a sample, the signal Tentative Paper Present is generated. This circuit consists of a four bit counter (U20) and the one-shot (U19). The counter is cleared each time the clear signal is generated at U11-3. This happens at the beginning of each 128 diode sample. The counter then starts

counting the number of bits seeing white before the next load pulse occurs. If 16 or more occur, the carry output from U20 (pin 12) causes U19 to fire, creating Tentative Paper Present (TPP). The counter will then be cleared and will count the number of white diodes in the next sample, The timing of the one-shot-is such that it will not time out before the next sample is completed. If the next sample does have 16 white bits, the one-shot will be retriggered causing Tentative Paper Present to continue. If the second sample did not have 16 or more bits, the one-shot will not be retriggered and will time out ending the signal Tentative Paper Present. After about 13 such frames U7-5 is used to force TPP high while driving left.

It has already been shown that the Video Addressing Circuitry is constantly strobing the diodes and that the resultant data is transformed from analog to digital form. This data is stored alternately into Frame Buffers 1 and 2. Let's set up the conditions for the start of this explanation. The Buffer Switch (U7-2, 3) will be selecting one of the two Frame Buffers as the buffer into which the current sample of 128 diode bits is being stored. This is achieved by allowing that buffer to receive the signal WRITE ENB via the NAND gate, U26. Both Frame Buffers will be receiving the address being generated by the Video Write Addressing Circuit due to the signal TEST being low, forcing the select input high on the four multiplexers U14, U15, U16, U17. The Pulser (U8, both

halves) is clamped clear by the Low on the clear inputs (pins 10 and 13). This low is created by the circuit consisting of three parts of U10 and the inverter U22. The one-shot (U19) is reset at this point. U10-3 is high due to the signal TEST being low. U10-8 is low due to two high inputs, therefore U22-8 is low.

When all the diodes have been strobed and the data written into the selected Frame Buffer, the Video Write Addressing circuit goes through the process of resetting the counter and issuing the RStart pulse. When FF3 creates RStart, it also creates RStart(not) which is the input to 10-9. When RStart(not) goes low, U22-8 goes high removing the clear from U8. The next signal, Reset V/H(not) will set the first stage which in turn toggles the Buffer Switch (2). The end of RStart(not) resets the Pulser by clamping it cleared. Each time the 128 diodes are strobed, the alternate Frame Buffer is selected.

The collecting of samples takes place at a higher rate than the subsequent circuits can handle them, therefore portions of the samples stored in the Frame Buffers are never used and are simply replaced in the buffers by later samples, The Horizontal Servo Control Circuitry determines when the latest sample in the Frame Buffers will be transferred to the Video Processing circuitry. Every second count UP pulse from the Horizontal Encoder causes the signal Sample(not) to be created. This signal provides the input to U10-1 as well as to the one-shot (U19).

When Sample(not) goes low, the one-shot fires. U10-10 goes low taking U10-5 high. U10-1 is low, U10-2 high, thus U10-4 is high. U22-8 goes high removing the clamp from the Pulser allowing it to toggle the Buffer Switch at the next Reset V/H(not). The firing of the one-shot also causes TEST to go high on U26, pins 2 and 13. The two Frame Buffers then receive their addresses from two different sources. The one selected as the buffer into which data is being written continues to receive the address being generated by the Video Write Addressing Circuitry. The other buffer, from which the sample is to be read by Video Processing, receives the Read Address being generated by the Scan Window Addressing section of the Video Processing circuitry (VA0-7). When the Sample (not) signal ends, the Pulser is again cleared. The one-shot remains fired for a period (about 13 frames) long enough to allow the Video Processor to read the data from the selected Frame Buffer. The signal RStart(not) is blocked by TEST(not) from swapping the function of the two buffers as long as the one-shot is fired,

The data from the buffer being read is output to the Video Processor as the signal RHVIDEO(not) which may be checked at TP10. Once the one-shot times out, the process returns to storing the data in the Frame Buffers alternately.

4-4. VIDEO PROCESSOR - OVERVIEW. - As the Read Head Analog and Digital boards are taking samples of the data present on the page being scanned, the Video Processor functions to collect and assemble these samples, now called Frames, into an unknown

matrix. This unknown matrix will ultimately be compared with a whole series of reference matrices to determine which reference matrix most closely resembles the unknown matrix. The best match will determine the code assigned to the unknown.

The collecting of samples by the Read Head Analog and Digital boards results in samples consisting of 128 bits corresponding to the diode column height. This column height overscans the actual character by a great deal. Since most characters within the standard alphabet will have a height which does not exceed 24 bits, the machine is really concerned only with those bits covering the character, However, skew and fluctuations in the baseline due to the typewriter will cause different sets of 24 to come into play from character to character. The Video Processor therefore selects a window of 40 bits at which to look. This allows for vertical drift or misplacement of characters. The Digital Board stores all 128 bits of the sample, however, the Video Processor requests transfer of only 40 of those bits, The Video Processor keeps track of where within the 128 bits the character lies and requests that only the 40 bits which contain the character be transferred. This process results in a windowed portion of the total sample being analyzed rather than the whole 128 bits, This portion is then referred to as a frame,,

In order to perform the comparison, the matrix must first be assembled, This is achieved by collecting the frames in a shift register known as SR2. The Character Detection Circuitry controls the loading of SR2 by allowing the loading to start

when the leading edge of the character is detected and stopping the process when the trailing edge of the character is found. At that point, all the frames of the character (unknown) have been assembled into a completed matrix.

This matrix then has to be moved about within the shift register in order to position the matrix. This is called justification. Justification is a process whereby the matrix is made to sit with its lowest point upon a bottom reference line (Bottom Just) and with its leftmost edge against a left reference line (Left Just), Since all the characters within the reference alphabet are aligned against these same bottom and left reference lines, the unknown must be arranged in the same form to allow proper comparison.

The unknown matrix must also be analyzed to determine its height, whether it is broken such as an equal sign, and whether the character is too near the top or bottom of the scan window.

Once the unknown matrix has been positioned and analyzed, the Video Processor performs it last function on this "unknown" by forwarding it to the Character Identification Circuitry which compares the unknown matrix against all. the reference matrices,

The Video Processor is then free to repeat the same process up the next unknown matrix while the Character Identification Circuitry is identifying the unknown matrix just transferred to it,

The Video Processor responsibilities may be summarized as:

Addressing the Window of the Read RAM (Frame Buffers),

Character Start and End detection.

Assembling frames of data into a matrix,

Analyzing the resultant matrix.

Justifying (positioning) the matrix for comparison,

Loading the matrix into the URAM.

a. General Operation (figure A-6). - The Video Processor has six modes of operation which are:

(1) SCAN/SAMPLE

(2) LJUST

(3) POSITION MODE

(4) BOTTOM JUSTIFICATION

(5) JUSTIFICATION

(6) DIAGNOSTIC

Each of the first five modes is executed sequentially during the video processing operation on one character. The diagnostic mode is a special means of operation which is employed only when the diagnostic board is in the machine in place of the normal Executive Macro Memory Board.

(l) Scan Sample (Character Assembly). - This mode checks for the beginning of a character via the Character Detection Circuitry. When Character Start is detected, the data being received from the Frame Buffers on the Digital Board is assembled into a matrix in SR2 in preparation for later analysis and identification, At the same time, a horizontally compressed matrix is assembled in SRI. This process continues until the Character Detection Circuitry detects

Character End. Since the Character End criteria is normally two blank frames (unless the character is very wide or narrow), the number of stages in SR2 which will have been loaded may be defined by the formula:

TCW = ACW + 2 (Maximum of 24)

Where:

TCW = Tentative Character Width

ACW = Actual Character Width = Frames containing data

2 = The number of blank frames loaded after the character

When the matrix is complete, control is passed to the next mode.

(2) LJUST. - This mode Left Justifies the character. This is the process of positioning the character such that the first sample taken (the left edge of the character) is located at the output of Stage 1 of SR2. Since SR2 contains 24 stages, up to 24 samples may be taken of a character. Since only a few characters are 24 samples wide, most times there will be stages of SR2 which were not loaded during the Scan Mode. To move the character to the output end of SR2 requires that the matrix be shifted by a number of stages defined by the formula:

SS = 24 - TCW

Where:

SS = Number of stage shifts (stages remaining of the 24)

24 = Total number of available stages

TCW = Number of previously loaded stages.

To analyze the matrix, the matrix must be moved within SR2 such that the first frame which was shifted into SR2 is located within stage 1.

When the first frame was shifted in SR2, it was in the 24th stage. When the second frame was shifted in, frame 1 was moved over into stage 23. This process continues until character end is detected. If, for example, a character having 14 actual frames containing data was scanned, the first frame would end up in stage 9 (14 actual plus 2 blanks). The last frame of data scanned would be in stage 22, and stages 24 and 23 would contain blanks. To move the first frame over to the first stage of SR2 requires that the data in stage 9 be shifted some additional number of stages. This number is defined by the formula:

$$SS = 24 - TCW$$

In our example, TCW is 16 (14 actual + 2). Therefore, SS is 8. Consequently, 8 more bursts of 80 clock pulses must be issued to move the data in stage 9 over to stage 1. All the other stages move over to fill in behind. As the shifts are made, the input to the 24th stage is zeroes, so stages 24 through 14 are filled with zeroes.

Once the required number of stage shifts is made under control of the Executive Macro, control is passed to the Position Mode Circuitry.

(3) Position Mode. - This mode analyzes the matrix to determine:

(a) The height of the character

(b) Whether the character is broken (such as =)

(c) Whether the character is touching top or bottom of the scan window

(d) If the character is too tall

(e) Bottom Space

These matrix parameters are determined by placing SR1 and SR2 into the recirculate condition and issuing 80 SCCLK pulses. This causes the data in both shift registers to rotate within the registers one time and return to the same position. During the time the data is rotating in the shift registers, the horizontally compressed matrix in SR1 is analyzed. The position of the top and bottom of the matrix is noted and used to determine the matrix height (top minus bottom), If there is a break in the compressed matrix, the character is considered to be a broken character, such as equal sign. I the matrix extends to the top or bottom of the window, a misaligned flag is set indicating that the matrix is striking the Scan Window top or bottom. If the character is too tall (greater than 36), then the "Too Tall" flag is set. The Bottom Space is found by determining the distance between the bottom of the window and the bottom of the matrix. This value is loaded into the Scan Clock Counter and used during the next mode to Bottom Justify the matrix prior to transferring the matrix to the Character identification Circuitry.

(4) Bottom Justification. - This mode moves the data stored in SR7 and SR2 by less than a full stage, in fact, it will be only a small number of bits. Instead of the Scan

Counter issuing a burst of 80 pulses, the complement of the Bottom Space value figured out during the Position Mode will be loaded into the Scan Counter. The counter will then issue a burst of pulses equal in number to the Bottom Space value. This will move the matrix down until it is bottom justified within SR2. With the matrix moved in this manner, it will sit upon a bottom reference line when loaded into the URAM; the position required for character identification.

(5) Justification. - This mode transfers the justified matrix to the URAM in the Character Identification section where the matrix is stored during the identification process. This transfer frees SR1 and SR2 so they may be used to assemble the next matrix which will be scanned while the matrix just transferred to the URAM is identified.

(6) Diagnostic. - The sixth mode is not routinely used, but is employed only during certain diagnostic routines when the diagnostic card is inserted in the machine.

b. Subcircuit Operation, - There are several subcircuits that may be described before the overall Video Processing operation is covered. These subcircuits are:

(1) Window Addressing

(2) Matrix Assembler (SR2)

(3) SR1

(4) Character Detection

(5) Scan Clock Timing (SCCLK)

(6) Matrix Analysis

(7) Instruction Decoder

The operation of the subcircuits is described in the following paragraphs:

(1) Window Addressing (Fig. A-6). - This section contains the following parts:

(a) Bottom value latches 8M and 6M

(b) Bottom value counter 9M and 7M

(c) Top window value latches 3M and 5M

(d) Bottom = Top value comparators 2M and 4M

(e) Stop window latch 5N

The control circuitry on the Read Head Digital Board is constantly sampling the data being received from the Read Head and storing it into one of two RAMs. While a sample is being written into one RAM, the Video Processor reads the previous sample data stored in the alternate RAM. The Window Addressing circuitry addresses the RAM from which the data is being read.,

The sample written into the RAM consisted of 128 bits corresponding to the 128 diodes in the Read Head. Since the viewing area viewed by the 128 diodes extends considerably above and below the actual character, the Video Processor is only interested in 40 of the 128 bits of data stored in the RAM, a number sufficiently large to sample the character with only a slight top and bottom overscan. These 40 may be any of the 128 bits and may change from time to time depending on which diodes are over the character. The Executive Macro controls the overall process of deciding which 40 diodes to select. To enable the selection of the 40 bits, the Executive Macro establishes the boundaries of the area to be read from the RAM. A Bottom Value is established in the Bottom Value

Latches which determines the starting address from which data will be read from the RAM A Top Window Limit is set in the Top Value Latches wwhich determines where reading will cease. These two values are established 40 addresses apart.

To start the read process, the Bottom Value is transferred from the latches to the Bottom Value Counter. This addresses the point in the RAM from which the first data bit will be read. When the first bit has been transferred into SR1 and SR2, the Bottom Value Counter is incremented to the next address, etc., thereby selecting each of the 40 sequential addresses from the RAM. When the Bottom Value Counter has been incremented 40 times, it will contain a value equal to the Top Window Limit which will be detected by the comparator. This will set a latch creating the signal SWNDO(not) indicating that all 40 bits have been transferred,

When the next sample is available and the 40 bits are to be transferred, the bottom value is again transferred from the latches to the counter and the process repeated.

(2) Matrix Assembler, SR2 (Fig. A-6). - The Matrix Assembler (SR2) consists of 24 shift register stages with each stage containing 80 bits, The package designations are 27N, 28N, 29N, 30N, 31N, and 32N. The Matrix Assembler is usually referred to as SR2.

As the frames are transferred from the Read RAM on the Read Head Digital Board, they are assembled in SR2 until all the frames for a single unknown have been assembled into a

matrix which can be forwarded to the Character Identification Circuitry.

Since the stages are 80 bits long, each stage can store a 40 bit frame. (In fact, there are 40 blanks in each stage.) a common clock causes all bits of all stages to shift to the right at the same time. This clock is issued in bursts of 80 to shift the frames by one complete stage in SR2 as the new sample is entered. The Scan Window Addressing section selects the 40 bits of data that are entered from the Read RAM. When the Stop Window Latch sets creating SWNDO(not), further input to stage 1 of SR2 is blocked. The effect is to shift in the 40 bits of data from the Read RAM followed by 40 blank bits each time a sample is loaded into SR2,

Once the matrix has been assembled, analyzed, and justified by the Video Processor, the matrix is available for transfer to the Character Identification Circuitry.

(3) SR1 (Fig. A-6). - The Video Processor must analyze the unknown matrix which has been loaded into SR2. To facilitate this process, another shift register (SR1) is loaded with the same data passing into SR2. This loading process takes place differently however. SR1 has only one stage of 80 bits. The output from SR1 can be externally fed back to the input where it is ORed with the new data being loaded. The result is that each new frame is superimposed on the preceding frames thereby creating a single, horizontally compressed frame.

This single frame provides information about the matrix in SR2. By analyzing the single frame in SR1, the lowest and

highest points (bottom and top) of the matrix (character) can be determined. Subtracting the bottom value from the top value yields the height of the matrix, If the frame is divided into two segments, the matrix represents a broken character such as i, equal sign, colon, or semi-colon. The Video Processor controls this analysis, but it is the data in SR1 that provides the characteristics of the unknown matrix.

(4) Character Detection (Fig. A-6). - As the Read Head scans across the page taking samples, the 128 diode column may be Located over a character or above the space between characters. If the diodes are over a character, some of the diodes will see black and some white. If the column is located between characters, all the diodes will see white.

The Character Detection circuitry is responsible for detecting when the Read Head comes onto a character and when it runs off a character. To do this, it checks each frame as it is shifted into the first stage of SR2. Ii the data being shifted into SR2 indicates that none of the diodes has seen black, then the Read Head is not over a character. If the data shifting into SR2 indicates that some number of the diodes have seen black, then the Read Head is over a character.

For discussion, assume that the scanning process has just started on a line. At this time the signals FB1, FB2, FC, and POPF are all Low. As each frame is shifted into SR2, the same data is placed on the input to the FBI latch. When a frame is finally shifted into SR2 that contains data (black), the FB1

latch will be set indicating that the circuit has found a bit in the current frame. When the next frame starts to shift into SR2, FB1 is transferred to FB2 and FB1 is reset. FB1 then checks the new frame to see if it has any data in it. So FB1 indicates if the current frame has data in it and FB2 indicates if the preceding frame had data in it. When both FB1 and FB2 are set, the indication is that two consecutive frames have had data bits in them.

The FC latch checks each frame of data being shifted into the first and second stage of SR2. The FC stands for Found bit Correlated which means that two consecutive frames have had data located on the same horizontal plane. This may be better understood by considering it to mean that the same diode in the Read Head Assembly has seen black during two consecutive samples. When this flag is set, the data scanned from the sheet must have some width to it and not simply be a reflective irregularity in the page.

The POPF latch is set whenever the number of data bits in the current unknown exceeds 16. The counter which sets the POPF. latch is cleared each time the signal ENCODER SAMPLE is generated at the beginning of the Video Processing cycle. When a frame containing data is shifted into SR2, the Executive Macro detects FB1 and issues TCSF (Tentative Character Start Flag) which prevents the counter from being cleared. The counter will contain the number of bits contained in that same frame which set FBI. As the next frame is shifted into SR2

the number of data bits in that frame will be added to the number in the previous frame, When the total number of bits exceeds 16, the counter will overflow setting POPF, If FBI is reset before POPF is set. the Executive Macro will remove TCSF and the counter will be cleared at the next ENCODER SAMPLE SIGNAL.

(5) Scan Clock Timing (Fig. A-6). - The Scan Clock Timing section is responsible for issuing the clock pulses to shift registers SR1 and SR2. These pulses may be issued either in bursts of 80 or in a burst of pulses equal in number to the Bottom Space value determined by analyzing the compressed matrix in SR1. The circuitry works the same in both modes except that the source of the data loaded into the counter is changed to determine which number of pulses are to be issued.

(a) During one mode of operation, the circuit issues the burst of 80 pulses as follows. The load input on the counter (11P and 11R) is taken low causing the data on the parallel input lines to be loaded into the counter. This data is the complement of the number 80 as controlled by the transfer gates. At the end of this transfer process, 10S-5 is set high creating the signal SCCF which allows the clock to proceed through into the counter and also to create the signal SCCLK(not) The signal SCCF is checked by the Executive Macro to detect when this circuit is running. The clock runs until 80 clock pulses have been issued at which time the counter is at a full state. The all ones detector, 12P, then blocks the clock at

12P-4 and allows control flop 10S-5 to reset. SCCF is lowered to signal that the counter has finished counting.

(b) During the other mode of operation, the circuit issues a number of pulses equal to the Bottom Space value. This value is placed upon the inputs to the transfer gates which provide the input to the counter. The control flop 11S-9 is set such that pin 9 is high. when the load line on the counter is taken low, the complement of the number on the inputs to the transfer gates is loaded into the counter. The process from this point on is identical to the above mode, the difference being that some number of pulses is output other than 80.

(6) Matrix Analysis (Fig. A-6). - The Matrix Analysis section checks the characteristics of the compressed matrix in SRI during what is called "Position Mode." The following are checked for or determined:

(a) Bottom Space Value

(b) Character Height

(c) Bottom Space Zero

(d) Top Space Zero

(e) Character Too Tall Flag

(f) Bit Height Too Low

(g) Broken Character

This analysis is achieved by issuing 80 SCCLK(not) pulses causing the data in SRI to recirculate one full revolution and back to its original position. This does not change the data, but allows the detection of certain characteristics of the "unknown".

Initially the Position Counter (9P and 9R) is reset to zero. The SCCLK(not) pulses are counted by the counter to establish when during the 80 pulses the events occur. The data shifting out of SRI will normally be zeroes to start. When the bottom of the compressed character starts shifting out, the data will become ones. This transition point from zeroes to ones is detected and 2R-5 goes high creating LBLF (Load Bottom Latch Flag). The value of the Position Counter at this transition point is locked into the Bottom Latches (8P and 8R). This process has stored the number of pulses which were issued to shift SRI far enough to bring the bottom of the compressed character out of SR1. This value is known as Bottom Space.

The counter will continue to count the SCCLK(not) pulses. When the top of the compressed character is reached, the data at the output of SR1 will change from ones to zeroes. This transition is detected causing 3R-9 to go high creating LTLF (Load Top Latch Flag). This signal latches the value of the Position Counter into the Top Latches (8N and 9N). This process notes the number of pulses which had to be issued to bring the top edge of the compressed character out of SR1.

This information provides the means for determining several things. First, the Bottom Space value which is stored in the Bottom Latches indicates how far the character is sitting above the bottom of the scan window. In order to Bottom Justify the character, it will have to be moved down by this distance during SJUST Mode.

The character height can also be determined at this point. Since the location of the top and bottom of the compressed character is known, the subtraction of the bottom position from the top position will yield the height of the compressed character. This subtraction is performed by the adders 7N and 6N. The inputs to the adder are the true value of the Top Latch and the complement (inversion) of the Bottom Latch. The Carry input of the first stage is tied high (7N-13) thereby adding 1 to the sum. The result is the difference between the Top Latch and Bottom Latch values which is the height of the character. The output from the adder is the HT1 through HT128 lines.

If when the Position Mode starts and the first SCCLK(not) clock pulse occurs, the first bit which comes out of SRI is a one, then the indication is that the character is touching the bottom of the Scan Window. This condition causes 2N-9 to go high creating BSZF (Bottom Space Zero Flag). 2N-8 also went low causing the signal VMF2 (Vertically Misaligned Flag 2). VMF2 is detected by the Executive Macro so that it may adjust the Scan Window position if necessary. A similar condition occurs if a one is shifted out of SRI at the very top of the window. This sets 3R-5 creating TSZF (Top Space Zero Flag) which in turn creates VMF1. VMF1 and VMF2 will be loaded into the Flag Buffer at the end of Character Identification.

There is a maximum height which valid characters will not exceed. The program loads this maximum height (36) into a six bit latch, 10T. The output from the Latch is compared with the

output from the adder which is the height which has been determined from the compressed character. As long as the height never becomes greater than the allowable maximum, no problem exists. If the determined height does exceed the maximum, the signal CTTF (Character Too Tall Flag) will be created which in turn creates both VMF1 and VMF2. This condition indicates to the Executive Macro that the character is too tall. This would be the situation created by a vertical crossout. These VMF flags will be stored with the character to indicate that there is something wrong with it and suitable action such as a Key Optics Stop must be taken.

Occasionally, there will be bits of dirt beneath a character which will be stored in SRI as an additional segment of ones. This segment will shift out of SRI prior to the valid character segment and will cause both the zero/one and one/zero detectors to set. Since a top and bottom value would be latched into the latches, a resultant character height would be calculated by the adder. Since bits of dirt would have very low height, any dirt can be ignored by bypassing any segments which do not have a height which is greater than three and looking further in SR1 for the valid character data.

There is a comparator, 7P and 6P, attached to the output of the adder. The other side of the comparator is tied with the two least significant bits high and all the other inputs low. This places a value of three on the inputs. The output is taken from the A less than B output and creates the signal

BHTL (Bit Height Too Low). This signal indicates that the data segment which set the zero/one and one/zero detectors was three bits or less high. This signal, when active, indicates that the height was too low to have been caused by a valid character, therefore, it must be dirt. The signal BHTL causes 1P-2 to go low creating BBS(not), (Bottom Bit Small). This signal resets the zero/one and one/zero latches allowing new values to be stored when the valid segment comes out of SR1.

After the top of a character has been found and the one/zero latch is set, another segment may occasionally be found sitting above the character. This segment may represent one of two things. First, it may be another bit of dirt, only this time it is above the character, The other possibility is that the character is broken such as a.. equal sign, colon, semi-colon, or lower case i. When a broken character is encountered, a new top value must be latched into the Top Latch in place of the value stored when the top of the first segment was reached.

The determination as to whether the new segment represents dirt or part of a broken character is made through the following process. The input at 7U-2 is the ANDed result of the one/zero latch and the output of SR1. When a second segment is encountered 7U-5 will set as the first bit shifts out of SR1. The second bit will cause 3U-5 to set. This enables 1P-5 at the next transition of the 9 MHz clock. The other side of the latch 1P-6 is the signal TBS(not) (Top Bit Small) which is ORed at 4P-13 with the signal that originally caused the top value to

be set into the Top Latch. This makes LTLF go low. When the data coming out of SR1 changes to zeroes again, 7U and 1P reset taking TBS(not) high and LTLF high which latches a new top value into the Top Latch. If the segment had been caused by dirt, the latch 1P would not have been set and a new value would not be loaded.

The program is also able to establish a maximum distance above a character beyond which no further checking will be made for additional segments. The complement of this distance (10) is loaded into the vertical space latch 1U. At the beginning of each Position Mode, this value is transferred into counter 2U. Once the one/zero latch, 3R, is set, the Position Mode Clock is allowed into the counter. If the counter reaches full, the carry out line causes 3U-8 to go low creating STBF(not) (Space Too Big Flag) which in turn Locks up the Position Mode Clock at 13R-5 preventing any further analysis of the compressed character. Any segment which is far enough above the first segment to allow the counter to overflow is assumed to not be part of the valid character and is ignored by the discontinuation of character analysis,

Since the compressed character has to fall within the first 40 clock pulses, the scan window height, and it takes a total of 80 pulses to shift the data in SRI one full revolution, the Scan Clock will finish counting after the analysis is completed.

One additional circuit was included in this area which now has no functional purpose. This is the Broken Flag Latch, 2R-9,

Table 4-1

Operational Modes

MODE	SIGNAL STARTS	SIGNAL ENDS	No. of SCCLKs
SCANNING	CEF x SAMPLE	ESCN x PROGRAM	TCW x 80
LEFT JUST	LJUST	SCCF x PROGRAM	(24-TCW) x 80
POSITION	STPMS	ESCN	80
BOTTOM JUST	SJUST	ESCN	BOTTOM SPACE
JUST	ESCN x JUST	UHCOMP	HEIGHT +1

which sets when the compressed character in SRI represents a Broken Character as previously described. This latch is not checked by the operating program,, however, it is checked by the diagnostics. If it is faulty. it should be fixed to allow proper operation of the diagnostics in order to find a real problem.

(7) Instruction Decoder (Fig. A-6). - The Instruction Decoder, IOU, is loaded by the Executive Macro via the IR10-15 lines. The output from the latch determines which of the Video Processing modes is in operation. The RECRF output also controls when the data on SR2 will be recirculated within the individual stages.

c. Video Processor Operational Modes (Refer to Table 4-1). -

(1) Scanning Mode (Fig. A-6). - The Scanning Bode assembles the frames into a matrix, addresses the scan window of the Frame Buffers, and detects the character.

Video Processing is started when the Executive Macro detects that the Read Head has crossed Left Margin and causes CEF(not) (Character End Flag) at 12U-10 to go high indicating that the character end has not been reached. Actually, a character has just been started.

CEF(not) is gated with ENCODER SAMPLE resulting in a high at the J input to 10s. The clock input to 10s then causes 10S-3 to set. The Q output generates the signals SAMPLE and SAMPLE(not) which are used by the Character Detection Circuitry and elsewhere. At the same time, the Q(not) output at 10Q-2

passes to the OR function at 13S-13 and through an inverter to become the signal LD WNDO(not). This signal loads the Scan Clock Counter to the complement of 80, which is the same as 80 less than full. LD WNDO(not) also loads the Bottom Window Counters 9M and 7M.

When ENCODER SAMPLE returns low, 10S-3 resets ending SAMPLE, SAMPLE(not), and LD WNDO(not). The setting and resetting of 10s caused its Q(not) output (pin 2) to go Low, then high, thereby setting 11S-5 high which in turn enables the J input (pin 8) on the other half of 10s. The clock at 10S-9 then sets 10S-5 high creating SCCF. SAMPLE also caused 5R-5 to be set high storing the fact that a sample is being collected. When SCCF went high at 12R-2, the clock was allowed to pass into the Scan Clock Counter and also to create the signal SCCLK(not). The clock continues for 80 pulses until the counter has counted to full at which time this condition is detected at 12P-8 which goes low. This blocks further clocks from being passed through 12R-6. The next clock at 10S-9 toggles 10S-5 low thereby locking the clock up until the next ENCODER SAMPLE signal starts the process again. The signal ESCN allowed 5R-3 to go high indicating that the sample had been fully collected. The Executive Macro counts these EMSPLF signals to determine the width of each character.

When the Character Detection circuitry determines that the character end has been reached, the CEF(not) line is lowered and control passed to the LJUST mode.

(2) LJUST Mode (Fig. A-6). - The Left Justification Mode (LJUST) starts once the Scanning Mode has completed its job of assembling an unknown matrix which represents the character on the page. Once the Executive Macro has determined that the end of the unknown matrix has been reached, it does three things:

(a) Lowers the Character End Flag (CEF not)

(b) Issues LJUST(not)

(c) Causes bursts of 80 shift clocks (SCCLK not) until the matrix is Left Justified (SSHTS).

The Character End Flag is lowered by changing the instruction loaded in the Instruction Register (10U). This prevents the Scan Mode from operating further and keeps 10S-3 in the low state. The instruction that was loaded into the Instruction Register also caused the signal LJUST(not) to be issued. LJUST(not) will remain low for the duration of the LJUST Mode. This signal and its inverted form pass to the Start Position Mode Flag latch 9U. Wher LJUST goes high, 9U-2 will go low on the next clock pulse. This output, STPMF(not) will remain low until the signal LJUST(not) returns high and allows the clock to reset 9U signifying the end of the LJUST Mode.

While the Executive Macro holds the circuitry in the LJUST Mode, it causes bursts of 80 SCCLK pulses to be issued. Back during the Scan Mode the Executive Macro counted the number of times that the Scan Clock Counter issued bursts of 80 SCCLKs. That number was subtracted from 24, and additional bursts of 80 are issued. The result is that the total bursts issued during

the two modes is 24. The Executive Macro creates the signal SSHTS(not) which triggers the Scan Clock Counter and causes one burst of 80 to be issued. The Executive Macro then tests the signal SCCF to determine when the burst is complete. It then sends another SSHTS(not) pulse and tests SCCF waiting for the end of the resultant burst. This process is repeated until the Executive Macro has caused the required total number of bursts to be issued.

At this point the LJUST Mode is complete and the Instruction Register is loaded with a new instruction which takes LJUST(not) high.

(3) Position Mode (Fig. A-6). - Back at the beginning of the LJUST Mode, the signal LJUST allowed the Start Position Mode Flag latch (9U-2) to set. This stored the fact that the LJUST Mode was being run. At the end of LJUST Mode, LJUST is again lowered and 9U resets. That process of setting and resetting 9U causes the signal STPMF(not) to go low and then return high. The rising edge signifies the end of LJUST and tells the Position Mode to start. STPMF provides the toggle input to the first half of the D-flop 4R. This flop sets on the rising edge of STPMF(not) thereby enabling the second half of 4R. This creates the signal STPMS which does several things:

(a) Force sets the Position Mode Flag Latch 5P.

(b) Resets the first half of 4R.

(c) Acts as a general clear throughout the Matrix Analysis circuitry prior to analyzing the current matrix.

(d) Triggers the Scan Clock Counter circuitry to issue one burst of 80 SCCLK pulses.

The next positive transition of the clock would reset the second half of 4R thereby removing the clear from the Matrix Analysis circuitry. The 80 SCCLK pulses are issued and the unknown matrix is analyzed to determine its characteristics. When the last of the 80 pulses is issued, the signal ESCN clears the Position Mode Flag latch 5P and takes the circuitry into the next mode.

(4) Bottom JUST (Fig. A-6). - When the end of Position Rode is reached, the signal PMF returns low thereby setting the Bottom Just latch 9U. The resulting output is called SJUST(not). The setting of 9U-5 enables 8U which sets on the next clock pulse. Its output, pin 6, feeds back to 9U causing it to be reset. The pulse signal SJUST(not) which resulted:

(a) Toggles the control flop 11s which selects which input is provided to the Scan clock Counter. It is set to transfer the Bottom Space value calculated during Position Mode into the counter. Consequently, the counter will issue a burst of pulses equal in number to the Bottom Space instead of the usual burst of 80.

(b) Triggers the Scan Clock Counter to issue the number of pulses selected by its input,

The pulses issued by the Scan Clock Counter cause the matrix in SR2 to be moved such that it is bottom justified.

(5) JUST Mode (Fig. A-6). - Since the matrix in SR2 has been bottom and left justified during the previous modes, the bottom plane of the matrix is sitting at the outputs of the 24 stages of SR2. This bottom plane may, therefore, be parallel transferred to the Unknown RAM where the matrix will be stored while it is being identified. The contents of SR2 may then be shifted one bit making the second plane available at the outputs of SR2. This process of transferring and shifting is repeated until the entire matrix has been transferred to the Unknown RAM. One additional plane, a blank frame, is then transferred to the Unknown RAM.

During the last mode, Bottom Just, flop 8U-5 was set high. This output is tied across to the J input on 23N. However, for 23N to set, all three J inputs must be high. The signal JUST had previously held 23N and 22N in the clear condition. The clear was also removed when JUST went high. Since 22N is reset, its Q(not) output is high which feeds back a high into a second J input on 23N. The only J input preventing 23N from setting is pin 4, a signal called ESCN. That signal will go high at the end of Bottom Just Mode thereby allowing Just Mode to start as 23N sets.

The two flip-flops 23N and 22N are combined to form a Johnson counter which has the following sequence of states:

23N	22N	STATE
RESET	RESET	0
SET	RESET	1
SET	SET	2
RESET	SET	3
RESET	RESET	0

These states are decoded to create two signals, WRIT ENABLE(not) and 1 SRSHT(not), The first signal, WRIT ENABLE(not), is created during states 1 and 2 of the counter and causes the data on the outputs of SR2 to be parallel loaded into the URAM. The other signal, 1 SRSHT(not), causes the data in SR2 to be shifted one position so that the next plane of the matrix is at the outputs of SR2. This process is repeated until the entire matrix has been transferred.

At the end of the transfer process, the signal UHCOMP causes 8U to reset. UHCOMP is a flag which goes high when the transfer process has occurred a number of times equal to the height plus one of the "unknown". This stops the counter 23N and 22N by clamping them in the clear condition.

Once the Just Mode has been completed, the circuitry of this section may again be returned to the Scan Mode where it will be used to assemble the next matrix while the one which was just transferred into the URAM is identified.

d. Summary of Operation of Scan Clock (SCCLK). -

(1) Scanning Mode. - SCCLK will clock in bursts of 80 pulses loading SR2 and SRI. Clock is initiated by the signal "ENCODER SAMPLE."

(2) Left Justification. - After the program raises the flag "LJUST", it will issue the signal '"SSHTS" which will cause the "unknown" in SR2 to move one stage, i.e. the Scan Clock will pulse 80 times for each "SSHTS" issued by the program,

(3) Position Mode. - When Left Justification is finished, the program will lower "LJUST" and raise "RECIRC", and Position Mode is entered, The Scan Clock will clock 80 times. The clock is initiated by "STPMS".

(4) Bottom Justification. - When Position Mode is finished the hardware will automatically enter Bottom Justification ("SJUST"). The signal "SJUST" will initiate the counting of the Scan Clock. In this mode the Scan Clock will pulse an amount equal to the bottom space as determined during Position Mode,

(5) Unknown RAM Load. - In this mode, the Unknown RAM gets loaded and the Scan Clock must shift SR2 an amount equal to the Unknown height plus 1. This will load the "unknown" character into the RAM with a blank plane on top.

4-5. CHARACTER IDENTIFICATION - OVERVIEW. - The Character Identification circuitry takes the matrix which was assembled and positioned by the Video Processing circuitry and compares it with a whole series of matrices known as the Reference Alphabet, At the completion of this comparison process, one

of the Reference Alphabet characters will be chosen as the character which most closely resembles the unknown matrix. The ASCII (U.S.A. Standard Code for Information Interchange) code for that character will be placed into the line buffer section and the Character Identification circuitry freed to await the next unknown matrix from the Video Processor section.

a. General Operation (Fig. 4-9). - The Character Identification process starts each time the Video Processing circuitry signals that it has completed the process of assembling and Positioning the unknown matrix and has placed the resultant matrix into the Unknown RAM. With the unknown matrix stored in the Unknown RAM, the Video Processing section can go about assembling and positioning 'the next matrix as it is scanned on the page. The Character Identification circuitry can also take the time required to identify the matrix since it does not have the Video Processor tied up.

The Character Identification process involves comparing the unknown matrix with a whole series of matrices known as the Reference Alphabet. The Unknown RAM (URAM) contains the unknown matrix which was passed along by the Video Processing section. The Reference Alphabet is contained in a series of PROMs or ROMs. A third piece of data is stored in PROMs known as the Character Parameter Memory (CPM). This data identified certain parameters about each of the Reference Characters as each character is compared with the Unknown matrix. The result is that the Unknown matrix is identified as being that character which most closely resembles it in the Reference Alphabet=

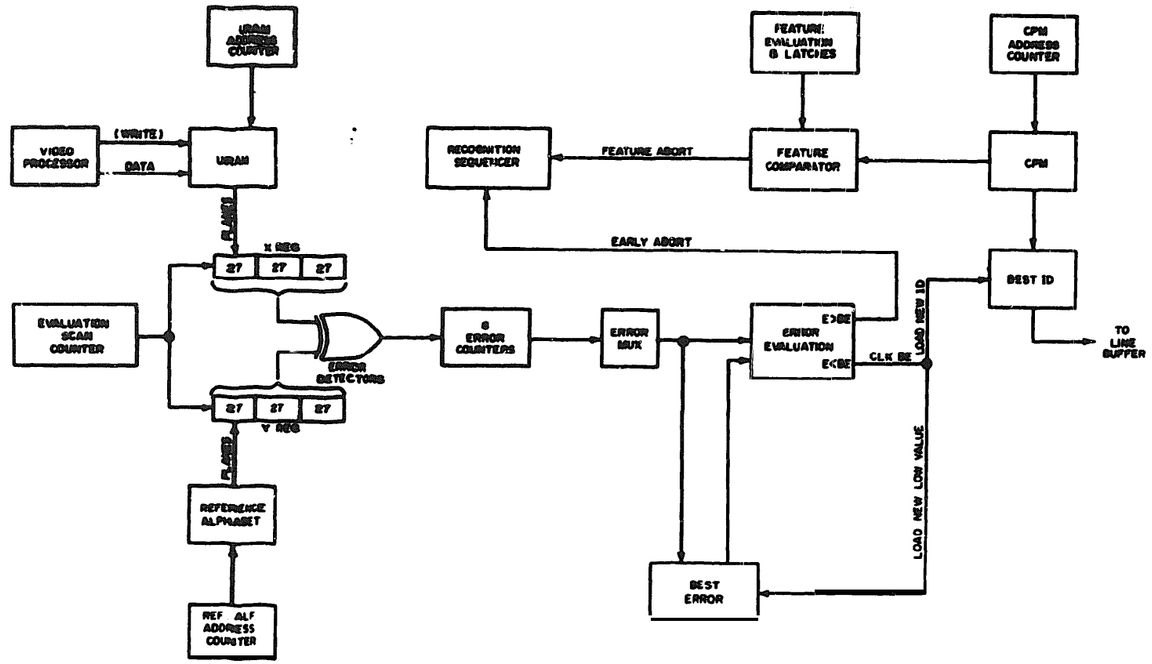


Figure 4-9. - Character Identification Block Diagram

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Actually, the comparison process uses an error detection process. As the Unknown is compared against the Reference, each point in the two matrices is compared. If the two points do not match, both white or black, an error count is generated. If the error count that results from the comparison of one Reference Character with the Unknown matrix exceeds the lowest previous error count for an earlier Reference Character comparison, then the Reference Character currently being compared looks less like the Unknown matrix than that earlier Reference Character did. Therefore, the current Reference Character is eliminated from consideration as the one that matches the Unknown, Another Reference Character is then compared to see if it can come closer to the Unknown than the previous lowest error count. The Reference Character which recorded the lowest error count of all the Reference Characters is identified as being the match for the Unknown matrix. The ASCII code for that Reference Character is placed in the Line Buffer. The ASCII code is one of the character parameters contained in the CPMs.

The comparison process is done by loading successive planes of the Unknown and of the Reference Characters into the X-Y Shift Registers and shifting the bits through the register while points are compared. A series of error detecting Rates compares the points looking for mismatches. Each time bits do not correspond, an error count is added to a set of registers known as the Error Counters. As each Reference

Character is compared, the Evaluation circuitry checks the number stored in the Error Counters. If the number exceeds the previous Best Error, that Reference Character is eliminated from considerat ion.

This whole process is controlled by circuitry known as the Recognition Sequencer. This circuit is started each time a new Unknown matrix is placed in the URAM and stops when the whole Reference Alphabet has been compared. The output from the Character Identification circuitry is the ASCII code for the Reference Character which most closely resembled the Unknown matrix.

b. Subcircuit Operation. - There are several subcircuits that may be described before the overall Character Identification process is covered. These subcircuits are:

(1) Unknown RAM (URAM)

(2) Reference Alphabet

(3) Character Parameter Memory (CPM) and Address Counter

(4) X-Y Shift Registers

(5) Error Counters, Latches, and Multiplexer

(6) Evaluation Circuitry

(7) Recognition Sequencer

(8) Recognition Scan Counter

(9) Unknown and Reference Height Counters

(10) Random Reference Character Select and Simulated Recognition Controller

(1) Unknown RAM (URAM) (Fig. A-7). - The Unknown RAM (known as the URAM in most notation) is an arrangement of 12 RAM chips resulting in a matrix of 32 addresses by 24 data bits wide. Each of the individual RAMs is 4 bits wide and has 16 addressable planes. By arranging six RAMs side by side with common address lines, the width may be expanded to 24 bits (4 bits by 6 chips), (Figure 4-10, URAM Chip Assignments diagram,) Two of these 24 bit arrangements are stacked one above the other to create the 24 wide by 32 high matrix. The Unknown matrix which was assembled by the Video Processor is transferred into the URAM as the last step of the Video Processing procedure.

The URAM is addressed by the Unknown RAM Counter consisting of two binary counters 23R and 23P. This counter' is strictly an UP counter. Prior to the start of the Load or Read process from the URAM, this counter is cleared by the signal CLURA which is fed to the Clear input of the counters. This will cause all the URAM outputs to be low. URAM1 to URAM4 address all the WAMs, therefore selecting the zero address of all the RAMs. The URAM5 output has an inverter tied to it SO that both the non-inverted and inverted forms are available, The non-inverted form is tied to the six RAMs which compose the lower section of the URAM, specifically 25R, 26P, 24P, 31R, 32P, and 30P. The inverted form is tied to the upper section 26R, 24R, 25P, 32R, 30R, 31P. These signals

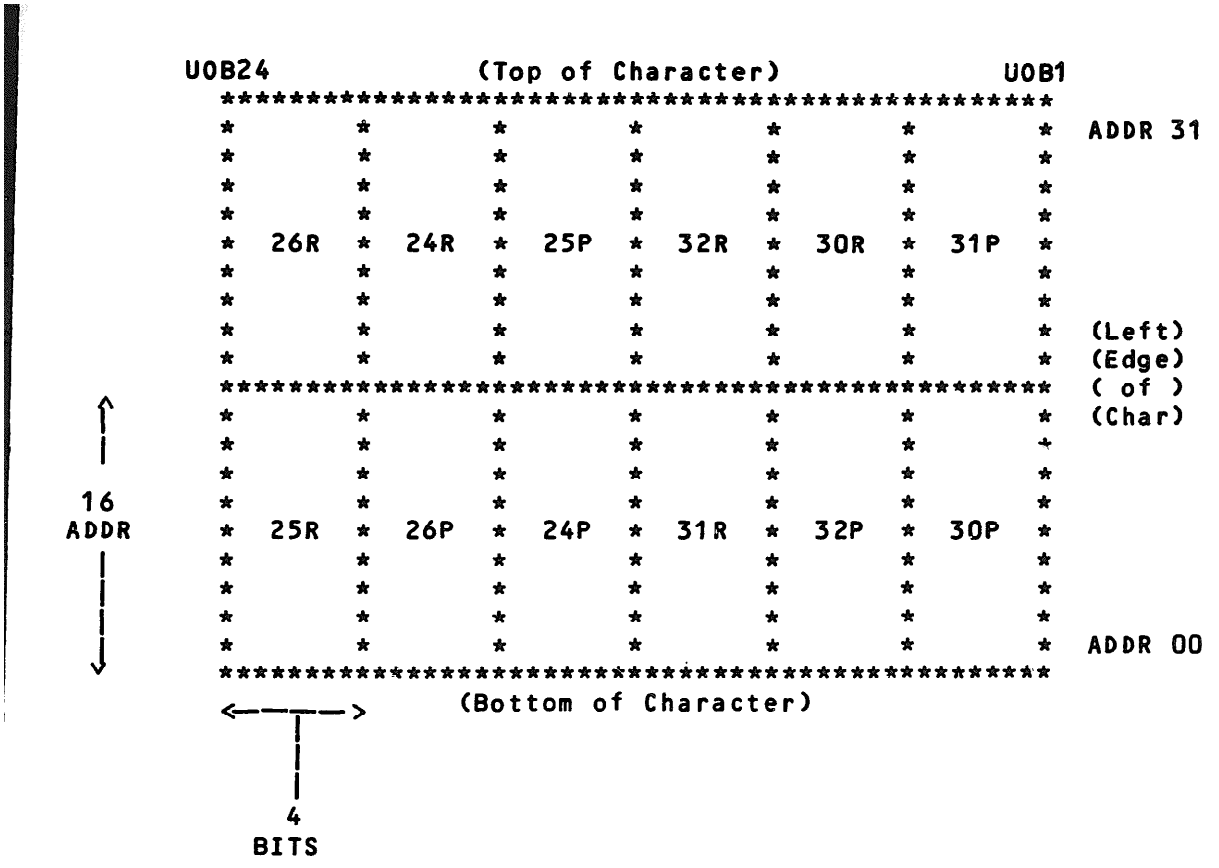


Figure 4-10. Unknown RAM Chip Assignments

control the Chip Select of the RAMs. Tied together in this form, the fifth bit of the RAM Counter selects the upper section or lower section of the URAM. Initially, with all bits low, the lower section is enabled and the zero bit of that section enabled,

Each time a Write or Read function has been performed, the RAM Counter is incremented by the signal INCUR CTR. The address will be incremented from zero to 15, The next increment pulse will set the first four bits of the counter back to zero, but will set URAM5 hi The lower section of the URAM will be disabled and the upper section enabled. The counter will select address 16 which is the lowest address of the upper section. From there on addresses 16 to 31 will be chosen in the upper section of the URAM.

The Write process is controlled by the Video Processing section as it transfers the assembled matrix from SR2 into the URAM. The first thing done is to clear the URAM Counter so that the first address is selected. The first horizontab plane of the matrix, the bottom, is at the outputs of SR2 since the character was bottom justified during Video Processing, The Video Processor issues a WRITE ENABLE(not) which writes the first plane of data into the first address of the URAM. The Video Processor then issues INCUR CTR(not) to increment the URAM Counter to the second address. At the same time it shifts the data in SR2 by one bit so the second plane of the Unknown matrix is on the UB1-UB24 lines, Another

WRITE ENABLE(not) is issued and the second plane is loaded. The counter is then incremented, SR2 shifted, a write issued, etc. until the matrix has been loaded. The number of cycles necessary to complete this depends on the character height. One additional blank plane is loaded just above the character by loading the blank which follows the character in SR2. This blank serves a purpose which will be described later. It should be noted that URAM is never cleared, new data simply overwrites the previous data (Figure 4-11).

Once the matrix has been written into the URAM, it may be used during the Character Identification process. The matrix may be read out by sequentially selecting addresses starting from zero and incrementing to the blank location just above the matrix. Remember that the read process does not in any way change the contents of the URAM so the URAM may be read many times.

To read out, the URAM Counter is cleared via CLURA thereby placing the contents of the first address, zero, on the output lines UOB1-UOB24. This data is loaded into the first stage of the X-Shift Register. The URAM Counter is incremented to the second address placing the second plane data on the UOB lines where it may be transferred into the X-Shift Register, etc. The incrementing and transferring is controlled by the Recognition circuitry. The Character Identification process requires that all the planes of the matrix be read out many times in order to compare the matrix against each of the reference

The contents of the URAM (Figure 4-11) reflect having loaded an upper case "A", then overwriting a lower case "a". Note the blank plane above the "a" that separates it from the remains of the "A".

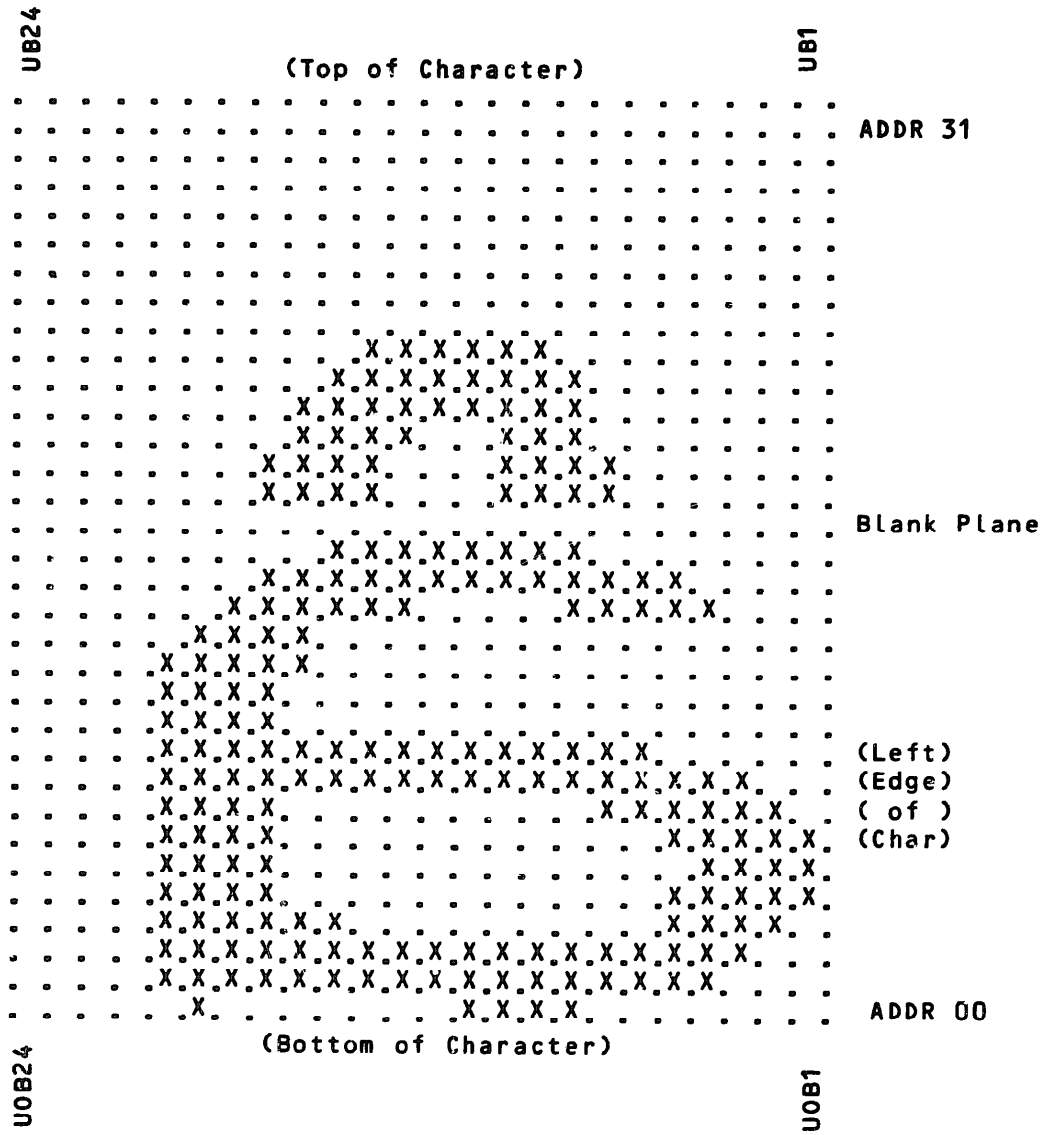


Figure 4-11. Contents of Unknown RAM (URAM)

characters. Comparison with just one reference character requires clearing the URAM Counter, then addressing and transferring each of the planes sequentially,

(2) Reference Alphabet and Address Counter (Figs. A-8, A-9, A-11, and Fig. 4-12). - The comparison process described earlier requires a set of Reference Characters against which each unknown character will be checked. These Reference Characters are contained within the Reference Alphabet, Each typestyle (OCR-A, OCR-B, etc.) requires a different Reference Alphabet. This is due to the differences in the formation of the characters in the different typestyles. If the proper Reference Alphabet is not used, the scanned characters will be improperly identified. An ALPHA may contain two Reference Alphabets at the same time, however, only one may be in use at any time. The desired Reference Alphabet is selected by the Alphabet switch on the Format Panel.

The Reference Alphabet is controlled by the Reference Alphabet Address Counter which sequentially selects the data in the Reference Alphabet PROMs for a particular Reference Character. The Reference Alphabet Address Counter consists of the counters 12A, 14A, and 11A. Prior to each Recognition cycle for a particular Unknown character, the counter is loaded such that stages 12A, 11A, 14A are set to start at the bottom horizontal plane for a Reference Character chosen at random. During the Recognition cycle, the counters are counted down.

The decoder 19A is tied to the output lines of the Address Counter third stage. The outputs from 19A will be used to select banks of PROMs in the Reference Alphabet. The outputs from 12A and 14A will be used to select addresses within the banks.

The Reference Alphabet consists of 10 banks of 3 PROMs. Each PROM is 8 wide by 256 addresses. Each bank is, therefore, 24 bits wide by 256 addresses. Multiplied by IO banks, the total ends up as 2560 addresses containing 24 bit words. The unknown character can be up to 24 bits wide which corresponds to the maximum width of the characters stored in the Reference Alphabet. The height of the unknown and reference Characters depends upon the particular character. A lower case a is a low character while an upper case A is a high character. The amount of space a character takes in the Reference Alphabet depends upon the character height. The characters are stored in the Reference Alphabet PROMs one immediately behind the other with only one blank location separating each character from the previous character.

(3) Character Parameter Memory (CPM) and Address Counter (Fig. A-7). - The Character Parameter Memory (CPM) contains additional information concerning each of the Reference Alphabet characters. The CPM consists of two PROMs each 8 bits wide by 256 addresses. They are tied with their address lines in parallel thereby creating 256 addresses each containing a 16 bit wide word. If the ALPHA contains two Reference Alphabets, it will also contain two sets of CPMs each consisting

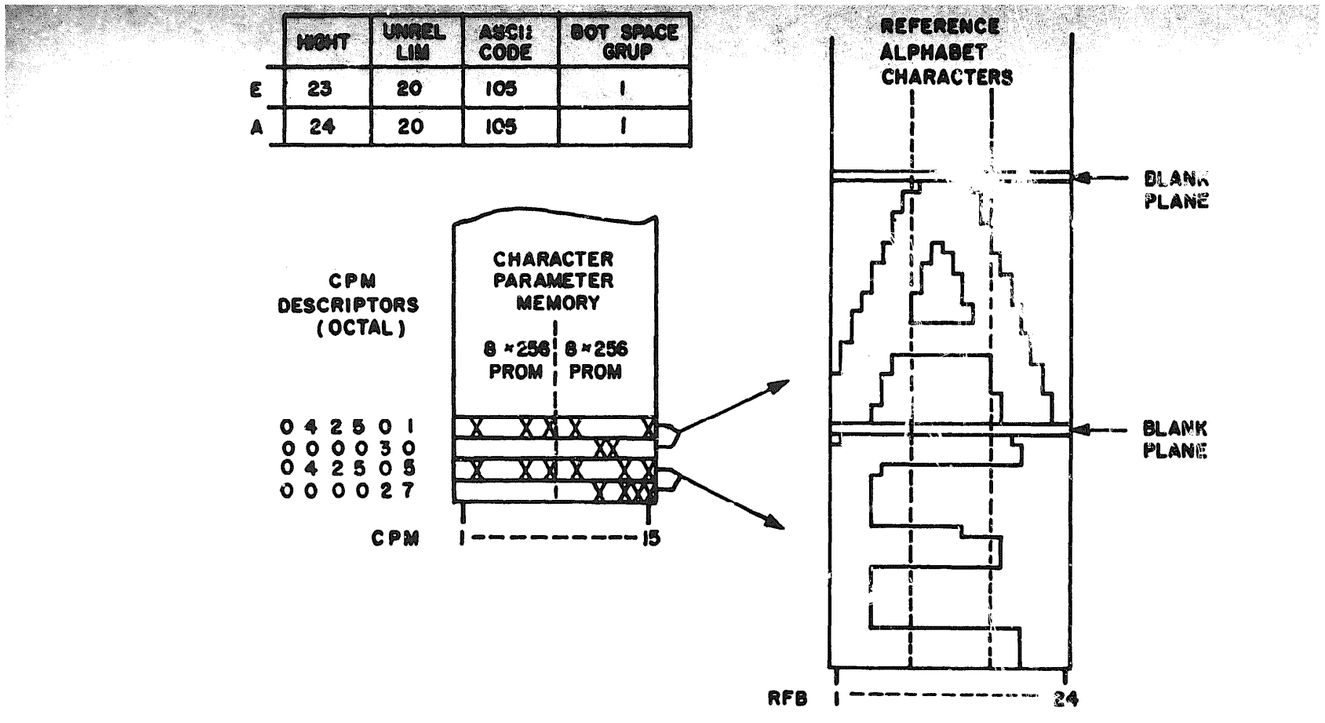


Figure 4-12. - Character Parameter and Reference Alphabet Organization for "E" and "A"

at two PROMs. The PROMs contain data for a specific Reference Alphabet. The proper CPM PROMs must be installed to match the Reference Alphabet contained in the machine.

Each Reference Character in the Reference Alphabet has two addresses in the CPMs which describe it. These descriptors cover areas such as the Reference Character height, maximum error allowed, and what the ASCII code for that character is. The organization of the CPM words is shown on the CPM Organization diagram, figure 4-13.

Addresses 000 and 001 contain information for "E". Addresses 002 and 003 contain information for "A". Addresses 004, 005, 006, and 007 are related to the two special test characters in Reference Alphabet positions 3 and 4. Addresses 008 and 009 define the Space character in Reference position 5. The remainder of the CPM addresses define the Reference Characters with two addresses per Reference Character.

PROMs 3S and 5S combine to form the CPM which is selected when the Alphabet Switch on the Format Panel is in the Font 1 position. PROMs 7S and 9S combine to form the CPM selected when the Alphabet Switch is in the Font 2 position.

The addressing of the CPM is done by the Character Parameter Counter composed of counters 2T and 2S. The counter is cleared by the signal JUST(not) prior to the commencement of the Character Identification process, and will be loaded at the beginning of each Character Recognition cycle with the address of the first descriptor for some Reference Character chosen at random.

CPM BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CPM DESCRIPTOR WORD NUMBER 1	NOT USED											16	8	4	2	1
												HEIGHT OF REFERENCE CHARACTER				
CPM BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CPM DESCRIPTOR WORD NUMBER 2	2 BOTTOM SPACE GROUPS	1	NOT USED		MAXIMUM ALLOWABLE ERROR				NOT USED	ASCII CODE OF REFERENCE CHARACTER						

Figure 4-13. - CPM Organization

(4) X-Y Shift Registers (Fig. A-12). - There are two Shift Registers which are used during the comparison process between planes of the Reference Character and the Unknown character in the URAM. Each of the shift registers is composed of three sections containing 27 stages apiece, For example, the first section of the "X" Register consists of I.C.s 27U, 28U, 29U, 27V, and half of 28V. The first three chips are each S-bit shift registers with parallel load ability. The chips 27V and 28V provide three additional bits. The total for the first section is, therefore, 27 bits. The other two sections of the "X" register and the three sections of the "Y" register are similarly constructed.

In the second and third sections of both registers, the parallel load inputs to the shift register chips are tied to ground. This provides a means of clearing these sections by activating the load input to these chips via the signal CLR XYSR(not) which causes these chips to be loaded with all zeroes, in effect, cleared. The same signal directly clears the D-flops which compose the three additional bits of each section.

The inputs to the first section of the X and Y shift registers provide the means for loading data into the registers. he inputs of the X register are tied to the outputs from the URAM. It should be noted that on&y the first 24 bits of the shift registers can be parallel loaded, This number, 24, is significant because it corresponds to the width of both the URAM and the Reference Alphabet. The Y register receives its input

from the Reference Alphabet.

To compare a Reference Character with the Unknown character, the 00 address of the URAM is selected by its address counter placing the bottom plane of the Unknown character-on the input lines of the X register. The bottom plane of the desired Reference Character is also selected by the Reference Alphabet Address Counter thereby placing that data on the Y register inputs. The Recognition Sequencer than strobes the data into the first section of both registers via the signal LD XY SR(not) (Load XY Shift Register). The Recognition Sequencer then issues a burse of 27 pulses, SHIFT XY SR(not), which causes the data to be shifted from the first section into corresponding positions within the second section. During this shifting process, error detection gates compare various combinations of X and Y outputs looking for faulty comparison. Each time a faulty comparison does occur, an error pulse is generated which is fed to the Error Counters keeping track of the error totals for the comparison with the currently selected Reference Character,

When the date from the first section has been shifted to the second section, new data must be loaded into the first section, The Recognition Sequencer increments the URAM Address counter to select the second plane of the Unknown, the first plane up from the bottom. The Reference Alphabet Address Counter is also incremented to select the next plane of the Reference Character. This new data is thus placed on the inputs to the first section of the X and Y Shift Registers=

The LD XY SR(not) signal is again issued loading the new data into the first sections.

The comparison process continues by again issuing 27 SHIFT XY SR(not) pulses which move the data from section 2 to section 3 and the data from section 1 to 2. During this movement, comparison of the various outputs is made causing more error counts, The number of errors generated depends on how well the Unknown and Reference Characters compare. The next plane will then be selected, loaded, shifted, another plane selected, etc. This will continue until the top of the taller character is reached or until a high error count indicates that the current Reference Character so poorly resembles the unknown as to make further comparison unnecessary.

If one of the characters is shorter than the other, either Reference or unknown, it will be necessary to compare the taller character with a blank. Remember that the process is one of determining which Reference Character generates the fewest errors when compared with the unknown, When one character is shorter than the other, all bits in the taller character which are above the highest point in the short character will create errors, If the comparison stopped at the top of the shorter character, the extra portion of the taller one would not be loaded and shifted through the X or Y Shift Register to create errors. A false identification might result.

It was pointed out that the characters of the Reference Alphabet were separated by one blank space, Additionally, the

URAM had a blank space at the top of the unknown character, When the top plane of the shorter character has been loaded into its respective shift register, the next time that same shift register is loaded, that blank space will be loaded. This blank will be compared with the remainder of the taller character with the result that every bit in the tall character will create an error pulse.

Once the comparison of one Reference Character versus the Unknown has been completed and its error count determined, the next Reference Character is selected at random and the URAM Address Counter is cleared. This places the bottom plane of the Unknown and the new Reference Character on the inputs to the X and Y Shift Registers,

(5) Error Counters, Latches, and Multiplexer (Figs. A-12, A-13, and A-14). - The Error Counters are used to keep track of the number of errors encountered during the comparison of one Reference Character with the Unknown, Each time the X-Y Shift Registers are loaded, they then shift 27 times. During this time, errors (mis-matches) are detected. Each error causes the Error Counters to be incremented. At the end of the shifting operation for that one plane, there is an accumulated error count in each of the Error Counters. Prior to the Sequencer loading and shifting the next plane, these values are transferred to a set of latches. The next plane is then loaded and shifting started. Additional error counts will be generated and added to the Error Counters. While these

errors are being generated and counted, the error counts which existed at the end of the prior shifting sequence can be evaluated since they are locked in the Error Latches.

The outputs from the Error Latches are tied to the Error Counter MUX. This multiplexer allows the Evaluation Circuitry to select each of the Error Latch outputs in order to compare it with the previous best error.

Each of the Error Counters contains six stages. They are tied such that the count will start from zero and proceed to 48. At 48, the counter will be forced to a count of 62. The counter will then be locked up such that it can only count 62, 63, 62, 63, etc.

(6) Evaluation Circuitry (Fig. A-14). - The Evaluation Circuitry has several functions:

(a) Flag characters for which an identification has been made with less than complete confidence.

(b) Detect vertical drift of the lines within the window and electronically adjust to account for the drift.

(c) Check the errors for the current comparison against the previous Best Error Count.

(d) Initiate an Abort where the current comparison causes an error count in excess of the previous Best Error.

(e) Store the ASCII code for the character with the Best Error Rate. Update the code as lower error rates are encountered.

The Evaluation Circuitry is in operation during the same time that the Recognition Sequencer is running. The Recognition Sequencer is selecting, loading, and shifting the planes of the Unknown and various Reference Characters through the X-Y Shift Registers. During this time the Error Counters are being incremented as different points of the Unknown and Reference Characters do not properly match. The Evaluation Circuitry evaluates the resultant error data to see if the Reference Character currently being compared with the Unknown is a better or poorer match than a previously selected best match. If the result of the comparison is a poorer match (higher error count), the character is discarded from consideration and another Reference Character checked. If the error rate indicates that the current Reference Character looks more Like the Unknown than any previous Reference Character did (lowest error count), then the ASCII code for the current Reference Character is latched into the Best ID latches and the new low error count is recorded. This new low value will be checked against the results obtained as the remainder of the Reference Characters are compared to see if any other character can get even closer to a perfect match. If a better error count occurs, a new ASCII code and error value will be stored. The ASCII code that is stored in the Best ID latches when all Reference Characters have been checked is the code for the Reference Character which most closely resembled the Unknown.

Prior to the start of Recognition and the Evaluation of the resultant error data, the first stage of the Evaluation Sequencer, 2Z, is clamped clear by the low signal RECOG. This signal, RECOG, is ANDed with two additional levels at 10Y creating the signal PRESET 48(not) at 10Y-6. This low signal feeds to the Best Error latches 8Z and 8X where it sets the BE5 and 4 bits high and BE3-0 low, a value of 48 decimal. This value will be used as the starting limit.

The Evaluation process operates as follows. First, the signal RECOG goes high at the input to the Evaluation Sequencer, 22-2. This is the indication that the Recognition Sequencer has started loading and shifting the Unknown and Reference Character planes thereby creating error data. The evaluation process must start to evaluate that error data. The signal X/Y SHIFTING(not) will go high signifying that a plane has been loaded and is being shifted through the X-Y Shift Registers. This allows 22-8 to go high on the next ECLK pulse which is free-running at 5 MHz. The signal LOAD LATCHES(not) is generated at 1Y-3 and fed to the latches of the Error Counter section. This primes the latches for loading as soon as LOAD LATCHES(not) returns low. The sequencer will remain in this condition until the X-Y Shift Register finishes shifting the current plane. When shifting is completed, X/Y SHIFTING(not) will go high at 3Z-4 allowing ECLK to set 3Z-8 high. LOAD LATCHES(not) returns high loading the Error Counter values into the Error Latches. At the same time, the signal ENABLE ECTR(not) at 1Y-6 goes low. This is fed to the MUX Strobes Counter, 11Z, where it

removes the Clear. The clock input then causes the counter to count from 0 to 7 sequentially selecting the data from the Error Latches so that it can be evaluated. When the count of 7 is reached, the ECT1, 2, 4 outputs are all high at 2Z. The Sequencer will be clocked by ECLK resetting the first stage, 2Z. The Clear is placed back on the MUX Strobe Counter as ENABLE COUNTER(not) returns high and the next signal, END OF CYCLE(not), is generated at 1Y-11. Since 2Z is reset, the next ECLK will reset 3Z thereby ending END OF CYCLE(not) and creating E C Y CLE(not).

Assuming there was no early abort cycle, this sequence will be repeated over and over until the last plane of the tallest character is reached. This last plane will be indicated by the signal LAST PLANE at 7Z-12. It comes from the Recognition circuitry. It is now time to evaluate the results. When LOAD LATCHES(not) is generated, 7Z is set causing ABORT CYCLE at 7Z-9. When the last plane has completed shifting, X/Y SHIFTING(not) allows 3Z to set making LOAD LATCHES(not) return high thereby latching the final error values for the comparison of the Reference Character into the Error Latches. ENABLE ECTR(not) then removes the Clear from the MUX Strobe Counter which counts to 7 in order to sequentially select each of the Error Counter values through the Error Counter Multiplexers.

As the data from each Error Counter is selected by the Multiplexer, it is checked against the previous best error to see if it is lower than the lowest error found se far (BE).

This is accomplished by the BE Comparator 9X and 9Y. One side of the comparator has as inputs the value stored in the BE BITS latches. This is the data on the lines marked BEO-BES, The other side of the comparator is tied to the Error Counter Multiplexer (E0-E5), The data on these lines is the value of one of the Error Counters. The output from the comparator is taken from the E greater than BE line. If the Error Counter value is greater than the value already in the BE BITS latches, this line will go high making 2Y-5 low and preventing this new value from being entered into the BE Bits latches, If the Error Counter value was less than or equal to the value in the BE BITS latch, the E greater than BE line will remain low keeping 2Y-5 high. Since 1V-1, 2, 5 are high, the next ECLK will cause the new, low error count to be loaded into the BE BITS Latches, The next Error Counter input will then be selected and checked to see if it is higher or lower than the previous lowest value. If higher, the previous Low value will be retained. If lower, the new value will be latched into the BE BITS latches. After all eight have been selected and checked, the value in the BE BITS latch will be either 48 (all Error Counters exceeded 48 so no new value was established) or a new value less than 48 (equal to the lowest value of the eight Error Counters).

The Sequencer will be advanced to the next step where END OF CYCLE(not) is generated. The signal RESET ERROR ETRS(not), which clears the error Counters in preparation for the next Reference Character, is also generated.

Each Reference Character will be compared with the Unknown. The Evaluation Sequencer will wait until the bottom plane of the Reference Character has been loaded and is being shifted through the X-Y Shift Registers. X-Y Shifting will then allow 2Z to set. When shifting is completed, X/Y SHIFTING(not) will allow 3Z to set. LOAD LATCHES(not) will return high locking the error counts into the Error Latches of the Error Counters section. ENABLE ECTR(not) will allow the Error Counters to be polled sequentially,

Since the Character Identification process is based upon finding the Reference Character which generates the fewest errors when compared with the Unknown, it does not make sense to continue comparison of a Reference Character once the error count exceeds a previous low value. Further comparison of that character can only increase the error count. For this reason, a circuit has been incorporated which performs an "Abort" when the current error count exceeds the previous best error. The Abort routine tells the Recognition Sequencer to discontinue comparison of the current Reference Character and jump ahead to the next one. This circuit consists of two sections of D-flop 1X and several gates.

The Abort circuit is in operation each time the Sequencer issues ENABLE ECTR(not), Initially, both stages are reset. This is an assumption that all Error Counters will exceed the previous low. The first stage has as its D input the signal E LESS THAN BE. As the data from each Error

Counter is selected, this line will indicate whether that Error Counter value is or is not less than the previous best error value. If any one of the Error Counters has a value less than the previous low value, the first stage will set, 1X-5 high. When the Sequencer advances to the next state and issues END OF CYCLE(not), the second stage will not set, thus, no Abort will take place. If all the Error Counters had values in excess of the previous best, the E LESS THAN BE signal would not go high. Consequently, the first stage would not set. Then, when END OF CYCLE(not) is issued the second stage will set thereby issuing Abort and further comparison of the current Reference Character will cease. In other words, all eight Error Counters must have a value accumulated in them greater than the best error for an Abort routine to occur.

If the comparison process for a Reference Character goes to completion without an Abort occurring, then at least one of the Error Counters must have a value less than the previous low. This Reference Character must, therefore, resemble the Unknown better than any prior Reference Character did. The signal LAST PLANE then allows 7Z to set creating ABORT CYCLE(not). When the error totals are evaluated after the last plane, this new bow value will be loaded into the BE BITS to replace the number in there. The BE Comparator output E GREATER THAN BE will stay low when a new low error count is selected. The output from 2Y-6 will go low clocking the new value into the

BE BITS latches. The same signal will also strobe the BEST ID BITS latches which loads the character code. The Recognition Sequencer will then select another Reference Character and process it for evaluation. After all Reference Characters have been compared, the character code which is in the BEST ID latches defines the character which generated the fewest errors during comparison with the Unknown.

When the Video, Processor has assembled the next Unknown and placed it in the URAM, the entire evaluation process will be repeated. This means it ill be compared with each Reference Character

E a c h reference Character has a Confidence Level associated with it. This value is stored in the CPM. This number is the maximum allowable error. If the comparison process goes to completion for a particular Reference Character, then it has been shown that the code for that character will be Latched into the BEST ID Latches. At the same time, the error count is placed into the BE BITS latches. This error count is compared with the Unrecognized Limit value from the CPM by comparator 7X. If the Best Error is greater than the limit, the output from the comparator takes 7Z-2 high which allows 7Z to set. This creates a signal called UNREC FLAG which is stored with the character in the Flag and Line Buffer. It indicates that there is some question as to the accuracy of the identification, If, on the other hand, the Best Error had been Iess than the limit, the UNREC FLAG signal would not have been generated meaning that the identification has

been made with confidence. The UNREC FLAG when high will be used later to initiate a Key Optics stop,

Earliier, mention was made of the Character Width Register (5V), into which the Executive Macro places the width value for the Unknown. The Unknown should never have a width of 32 or greater. If a value is detected which is greater than 31, a Touching Character situation is said to occur. If two characters did touch, the width would be measured from the start of the first to the end of the second. When the width is placed in the Character Width Register for a width greater than 31, the Qe output (5V-12) will be high. This will generate the signal TOUCHING CHARACTER which will be stored with the character in the Flag and Line Buffer. This flag will be detected later to initiate a Key Optics stop or a Scan Edit Deletion.

The Evaluation Circuitry performs one last function. It monitors the position of the character within the Windowed Data that has been transferred from the Video Acquisition Frame Buffers to the Video Processor. The Video Processor determined the distance from the bottom of the window to the bottom of the character. This is the value stored in the Bottom Latches of the Video Processing section. When a character is identified, its Bottom Space value is checked against a value stored in the CPM which defines how big the Bottom Space should be for that character. Each character belongs to one of four groups. Each group has a different value assigned. These

groups account for the natural Bottom Space differences between characters such as an A and a hyphen. The bottom edge of the hyphen can be seen to be higher than the bottom edge of the A. This must be taken into consideration before the electronics attempts to adjust the window to track a vertically drifting Line, The four groups are:

CROUP:	0	1	2	3
VALUE:	4	8	12	20

These values are wired into locations 4Z and 5Z, The value is selected by the multiplexers 4Y and 5Y which are controlled by the CPM bits 0 and 1 where the Bottom Space group is defined, The multiplexer outputs are fed to comparator 4W which checks it against the Unknown Bottom Space Bits value. Two signals may result. NBS GREATER THAN BOT indicates that the Nominal Bottom Space is Larger than the actual Bottom Space, therefore, the window must be moved clown to provide more space beneath the character. If the signal NBS LESS THAN BOT had been generated, the indication is that the actual Bottom Space is larger than desired and the window must be moved up to provide less space beneath the character.

There is also the possibility that the Nominal and Actual Bottom Space will not be different. It should be noted that the comparator 4W monitors the 4, 8, 16, and 32 lines,. That means that it is not detecting the value of the 1 and 2 bits in the Bottom Space Register. If, for example, a Nominal Bottom Space of 4 is selected, the Actual Bottom Space could

have a value of 4, 5, 6, or 7 and the comparator would consider them equal. This allows a Bottom Space tolerance of 4.

When a character is clocked into the Best ID latches by the signal CLK BE(not), the output from the comparator will set either STEP DN (10X-5) or STEP UP (10X-9) if the windo needs adjustment. If neither is set, no adjustment of the window is necessary., The Executive Macro will detect the setting of either STEP UP or STEEP DN via its test gates and adjust the window by 1 bit for the next character.

(7) Recognition Sequencer (Fig. A-11). - The Recognition Sequencer controls the order in which operations are performed during the Recognition portion of Character Identification. The Sequencer is composed mainly of ICs 23s and 24s. They are arranged so as to create a sequential series of pulses each of which performs a certain operation at its designated time. The State Counter, 23S, starts from a count of zero and counts up, The Decodes, 24S, outputs one unique signal for each possible value of the State Counter,

One complete sequence is performed each time the State Counter goes from zero to full (15 decimal) and overflows back to zero. This sequence is performed once for each Reference Character. For one Unknown to be identified,, all Reference Characters must be compared with that one Unkno Therefore, since the Reference Alphabet contains 64 characters, the sequence will have to be repeated 64 times to identify that one Unknown.

During one sequence, it is required that certain of the steps be repeated several times. States 5 through IQ must be repeated for each plane that is loaded into the X-Y Shift Registers. Provisions are made for causing the Sequencer to skip back from State 10 to State 5 the required number of times before the Sequencer is allowed to finish the entire sequence for one Reference Character, The order in which the operations take place and the purpose of each step is explained in the Character Identification - Circuit Operation section. The Recognition Sequencer Flow Chart also shows the order of events and the operations Performed at each step of the sequence,.

(8) Recognition Scan Counter (Fig. A-11). - The Recognition Scan Counter is a counter which issues a burst of 27 pulses each time it is triggered by the signal LOAD XYSR(not). This burse of pulses is the number required to shift the data in the X-Y Shift Register from one Section into the identical position in the next section. The Scan Counter consists of the counter 17V and 17W and the associated gates.

Initially, the two control Flops (17W-9 and 17U-5) are reset. When the Recognition Sequencer requires that the 27 pulses be issued, it creates the signal LOAD XYSR(not). The rising edge of this sets 17W-9 high. The next 9 MHz clock then sets the second flop, 17U-5, high. The combination of high inputs to 16W allows the 9 MHz clock to pass through the gate. This clock goes two places. First, it passes through 24U to create the signal SHIFT XYSR(not) which is the clock

that shifts the X-Y Shift Register. The clock also passes to the counter 17V. This counter has the LOAD XYSR(not) signal tied to its load input. When the LOAD XYSR(not) signal was issued, the counter was preset to a value of 4. The counter has one additional stage, 17W. This is cleared.

The result is a five stage counter containing the number 4. A five stage counter can count to 31 when it is full, The counter, therefore, has been loaded to a value of 27 less than full. It will take 27 clock pulses to count the counter up to full. The clock from 16W proceeds to count the counter up, at the same time issuing pulses to the X-Y Shift Register. When 27 pulses have been issued, the counter reaches full. The full state is detected by the AND gate 18V whose output then blocks further pulses from being issued, This same signal also causes 17U to reset further blocking the clock at 16W until the Recognition Sequencer again requests the burst.

When 17U was initially set, its output created a signal called XY SHIFTING (true & not). These signals are used to show that the data in the X-Y Shift Registers is being shifted. When the 27 pulses have been issued and the data in the X-Y Shift Registers is at rest, the reset condition of 17U indicates that the resultant error counts are available for evaluation,

(9) Unknown and Reference Height Counters (Fig. A-11). The Unknown and Reference Height Counters are Loaded with the number of planes contained by the Reference and Unknown

Characters, then, as the planes are loaded in and shifted through the X-Y Shift Registers, the counters keep track of how many planes of each character still have to be compared.

Since it is likely that the Reference and Unknown Characters will be of different heights, one counter will reach the top of its respective character before the other- The port ion of the taller character still has to be loaded into and shifted through the X or Y Shift Register. This must be done in order to generate errors indicating that this extra portion does not match the lower character. The Height Counter for the shorter character will allow the blank space above the shorter character to be selected and loaded into the X or Y Shift Register along with the extra planes of the taller character. The comparison of a blank plane against the extra planes of the taller character will generate error counts. The process will end when all the planes of both the Reference and Unknown have been completed.

Both counters are constructed and operate similarly. They are loaded with the complement of height and counted UP each time a load and shift of the X-Y Shift Registers takes place. The same signal that loads the counters clears two status latches. One indicates that the counter has reached its LIMIT which is the full condition. The second indicates that the counter has been issued one additional clock pulse and reached COMPLETION. This additional pulses allows the Address Counters for the Reference Alphabet and the URAM to select the

blank plane above the current character, The counter will then hang up the increment signal to the respective Address Counter so that as any additional planes of the other character are loaded and shifted, they are compared with the blank.

When both RH COMP and UH COMP are reached, then all planes plus the blank one of both Reference and Unknown Characters have been compared and the Recognition Sequencer is signalled to finish one Character Recognition cycle.

(10) Random Reference Character Select and Simulated Recognition Controller (Fig. A-10). - The purpose of this circuitry is to feed the Reference Alphabet Character to the Character Identification circuitry in a random order. This circuitry also is used to generate "fake" or simulated recognition cycles in between normal recognition cycles.

During normal recognition, this circuitry will select the address of the bottom plane of some Reference Character at random and load it into the Reference Alphabet Addresser. This circuitry will then set a flag in a RAM corresponding to that Reference Character. When the character recognition cycle is over, this circuitry will select another start address at random. If the new Reference Character has already been used, the next sequential start address stored in the PROM will be used,

This same process is repeated in between recognition cycles using the simulated recognition circuits, During simulated recognition, the Unknown Character will be the "or

tied" result of the last plane of the last unknown with a "simulated" character stored in the PROMs.

Major Blocks - The function of these circuits are accomplished using the following circuit blocks:

(a) Random Number Generator

(b) Random Number Latches

(c) Reference Start Address Counter

(d) Reference Character Start Address PROMs

(e) Recognition RAM Multiplexer

(f) Clear RAM Addresser

(g) Recognition RAM

(h) Simulated Recognition RAM Multiplexer

(i) Simulated Recognition RAM

(j) RAM Output Check

(k) Randomness Checker

(l) Simulated Character PROM

(m) Simulated Character Addresser

(n) Simulated Character Height Counter

Random Number Generator - The Random Number Generator consists of ICs U40, U41, U42. The toggle input to these flip flops are the outputs from the Error Generator circuitry. As errors are generated, these flops will toggle. Since no one can predict the amount of errors that will be generated during any comparison, the number which will be latched into the Random Number Latches will be random.

Random Number Latches - These latches consist of two 74193's, U16 and U17. When the Recognition Sequence passes through state eight (S8) a random number will be latched into these ICs.

Reference Start Address Counter - This counter consists of ICs U27 and U28. They will be loaded with the signal "INCCPMCTR 1" which occurs during state 4 of the Recognition Sequence. If the Reference Character addressed has been used before, the RAM Output Check circuitry will produce the signal "INCRNDA" which will increment the counter to address the next Reference Character Start Address.

The six outputs from the Reference Start Address Counter are used to address 64 places within the Reference Character Start Address PROMs. They also go to the Recognition RAM Multiplexer as well as the Simulated Recognition RAM Multiplexer.

Reference Character Start Address PROMs - These PROMs, U38 and U39, are 1702's, the same type used for the CPM's, Executive MacroMemory, and Simulated Character PROMs. The outputs are programmed so that the first 64 locations will correspond to the address within the Reference Alphabet of the bottom plane for each of the 64 Reference Characters. Addresses above these 64 locations are not used. Thus, for any number from 0 to 63 given to the PROMs, the Start Address for some Reference Character will be generated.

Recognition RAM Multiplexer - The Recognition RAM Multiplexers consist of IC's U36 and U37. During normal recognition

the address from the Reference Start Address Counter will be gated through to the Recognition RAM. When normal recognition is not happening the Clear RAM Addresser will be gated in order to clear the flags from the RAM.

Clear RAM Addresser - These counters U34 and U35 are constantly counting up with the 5MHz clock. The outputs of these counters go to the Recognition RAM Multiplexer and the Simulated Recognition RAM Multiplexer, These lines will be gated to their respective RAM's when the flags are to be cleared, i.e. during normal recognition.

RAM Recognition - The Recognition RAM is a 256X1 memory of which only 64 locations are utilized. Once a character is allowed to be processed a "one" will be written into the corresponding location. Before a character is allowed to be processed, circuitry will check that there is a zero in the corresponding RAM Address.

Simulated Recognition RAM Multiplexer - This multiplexer, consisting of ICs U23 and U24, is used to gate either the Clear RAM Address or Reference Start Address to the Simulated Recognition RAM. During Simulated. Recognition the Reference Start Address will be gated through. The clear RAM Address will be gated when the Simulated RAM is cleared.

Simulated Recognition RAM - This RAM functions in the same manner as the Recognition RAM. It will be used to control Simulated Recognition Cycles using the Reference Alphabet. This RAM is located at U12and is a 256X1 memory of which only 64 addressed are utilized.

RAM Output Check - The purpose of these circuits is to control the selecting of Reference Alphabet Characters to be sent to the Character Identification circuitry. If the output of the RAM is a "one" the signal INCRNDA will be generated to access the next location in RAM as well as the next start address. If the output is a "zero" the signal "WE" will be generated to write a "one" into this location and the start address will be given to the Reference Alphabet Addresser. This "one" is used so that if when the next random character is selected it can be determined if this Reference Character has been selected before. If it has, the next available start address will be used,

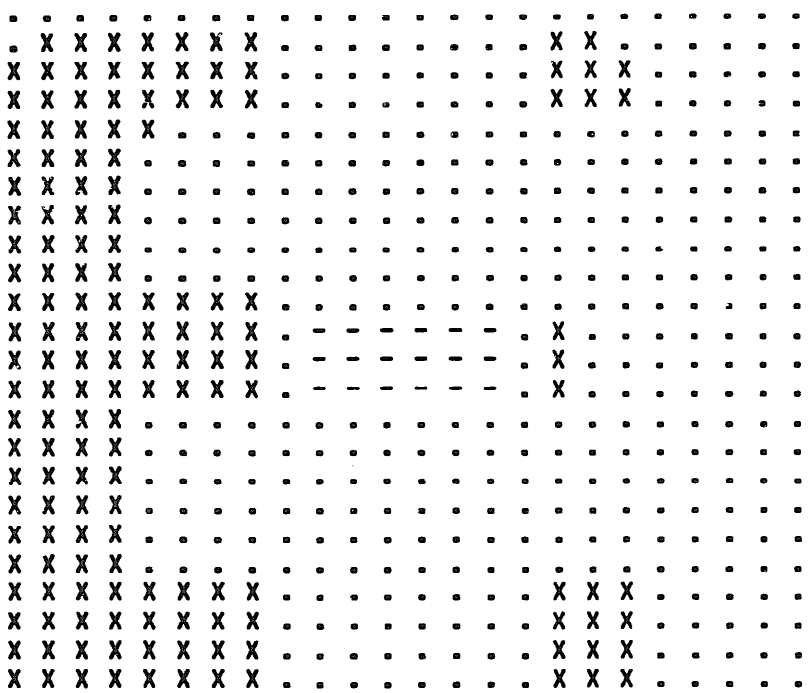
Randomness Checker - A simple circuit consisting of counters U7, U8, and U9, flops US and U10-5, and their related gates, detect the malfunction of one or more lines of the Random Number Generator. If one or more of the lines malfunction, it would be necessary to generate at least 32 INC RND A pulses during a Random Recognition Process (until END ALPHA). Therefore, every time INC RMD A is generated, it will cause U5-5 to set (as long as U6-6 is disabled); incrementing counter U7 and U8. The WE signal, which soon follows, will disable U3-11, causing U5-5 to jam reset; preparing it for another INC RND A,

If this sequence of events were to happen 31 more times, U6-6 would be enabled, Locking up counter U7 and U8 (disabling U5-2) and cause U5-9 to reset with any even character comparison cycle (U31-1). At the end of the Recognition Process,

RROV would momentarily enable U1-11 which, on its trailing edge, increment U9.

If these above conditions exist for 15 more consecutive times (or a total of 16 Recognition Periods) then U9-12 will go high, setting U10-5 and generate F3. The F3 signal would enable U6-12 generating FAIL 2, which would inhibit the generation of END ALPHA (11)17X-6, thereby preventing 17U-2 from going high, in which case the Program would issue a BEL-S-3 (on LED Display) error condition. The RAD Panel Switch A tests this circuit. Counter (10)U22 and flop (1O)U33-6 test the machine's ability to abort a Character comparisen upon encountering a high amount of errors.

Simulated Character PROMs - These PROMs, 26S, 28S, 30S, are 1702's which are preprogrammed with a "fake" character. The character programmed looks like this.



This character will be compared with the last plane of the last unknown character that went through normal recognition, The planes of the simulated character are addressed via the Simulated Character Height Counter. These PROMs are enabled via the signal "SRECO" or from the Rad Test Panel.

Simulated Character Address Counter - This circuit, 19V, 20V, controls the addressing of the simulated character during Simulated Recognition. This counter is cleared when the Recognition Sequencer passes through state 0 and is incremented during state 6 via "DEC CTRS."

Simulated Character Height Counter - This counter (4Z and 5Z) is used during Simulated Recognition to keep track of the height of the Simulated Character. The signal "SUHT COMP(not)" will go low when the counter has reached 24, the address of the blank plane above the Simulated Character. This counter is incremented at state 6 via "DEC CTRS" and is cleared during state 0.

Simulated Character Population Counter - Before normal recognition begins on the first character on a line of text, the Simulated Character will be pushed through the X Shift Register and the "X1" output will be tested to see if the Simulated Character circuitry has a malfunction. This circuitry consists of counters 20R and 21S and its associated circuitry. The population is checked to see if it exceeds 192. If this occurs, the unit will enter a failure mode.

c. Circuit Operation. - The Character Identification process is controlled and directed by the Recognition Sequencer. Once the Video Processing section has assembled, analyzed, and loaded an Unknown Character into the URAM, the Recognition Sequencer is signalled to go ahead and identify it. The Sequencer will then cause to take place those operations which are necessary in order to compare that Unknown against each and every Reference Character. The end product from this procedure is an ASCII code for the character which most closely resembled the Unknown. This ASCII code is transferred to the Line Buffer circuitry.

The Recognition Sequencer Flow Chart (Figure 4-14) shows the order in which the steps are executed. The numbers in the blocks refer to the State Number assigned to the outputs of the Recognition Sequencer. Care should be taken not to confuse the State numbers within the package outline with the IC pin numbers outside the package outline on the schematic.

The Recognition Sequencer has two modes of operation. The first mode occurs when the comparison of a particular Reference Character goes to completion resulting in that Reference Character being identified as the character which, so far, most closely resembles the Unknown. Later Reference Characters may subsequently be identified as even better matches.

The second mode, "Abort", occurs when, in the midst of comparing a Reference Character against the Unknown, the error count exceeds the previous Best Error. This indicates

that the current Reference Character is a poorer match than some previous Reference Character was. Further comparison will only serve to increase the error count, so further consideration of the current Reference Character is useless. At that point, in an effort to save time, an "Abort" is executed causing the Recognition Sequencer to bypass the remainder of the planes in the Reference Character.

The following description will treat each mode separately with the understanding that the total recognition sequence is a combination of both modes dependent on the Unknown being identified and the relationship of each Reference Character to that Unknown.

The Recognition process is started by the signal JUST from the Video Processing circuitry. This signal passes through a gate, 15U, to form END JUST(not) which is fed to 17U-1 allowing the J/K flop to set. When 17U is set, the Recognition process is in operation. 17U will remain set until the entire Reference Alphabet has been compared with the current Unknown, then it will reset indicating that Recognition is complete.

When the Reco flop, 17U, was in the reset condition, the State Counter, 23S, was held clear. The Sequencer was thus held at State 0. With RECOG low, 21U-9 is set high. When the Reco flop, 17U, sets, the signal RECOG allows 22U-8 to set high. The 4.5 MHz clock is then allowed into the State Counter 23S. The Recognition Sequencer then will proceed through its steps.

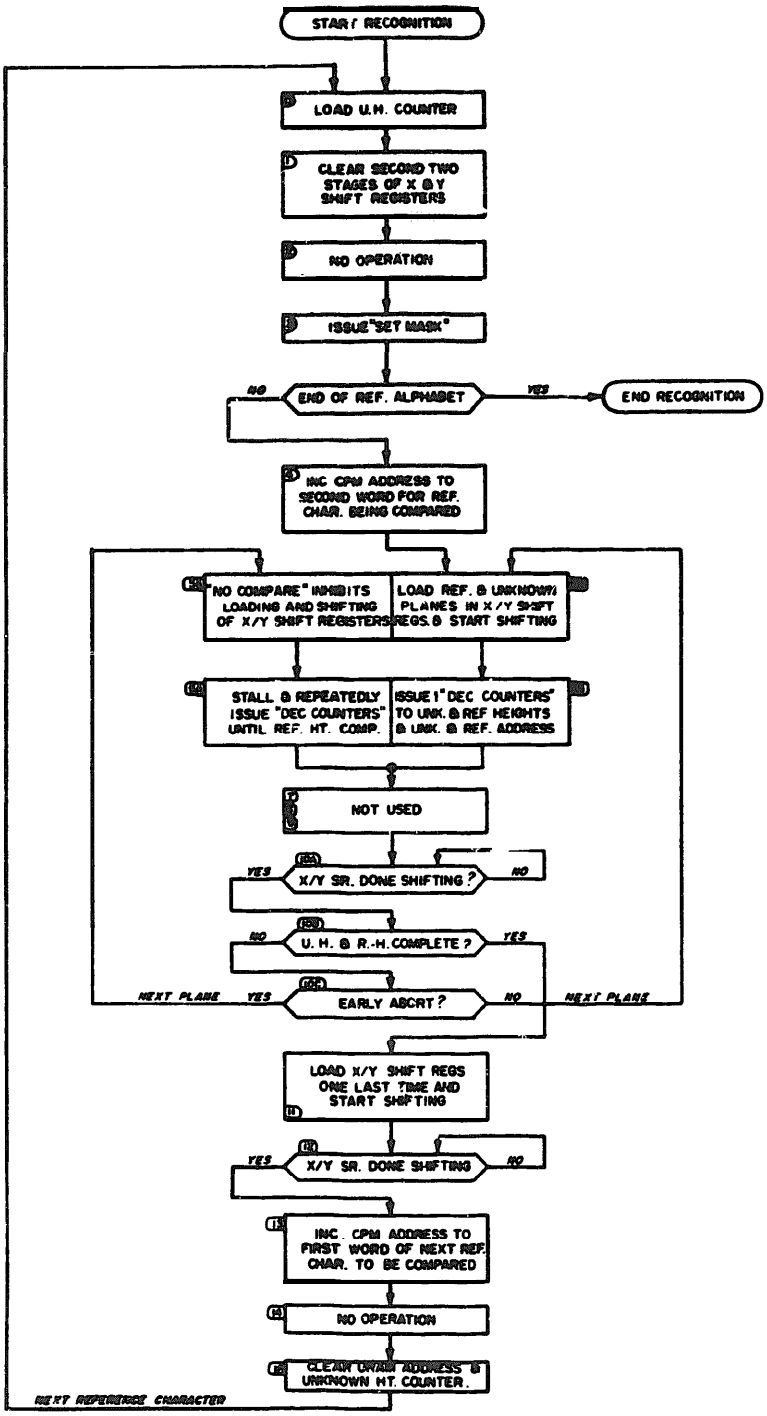


Figure 4-14. - Recognition Sequencer Flow Chart

full comparison is the first mode which will be described. It is the one which takes place when a Reference Character is fully compared with the Unknown.

State 0 causes the Unknown Height Counter to be loaded with the height of the Unknown Character from the Height Subtractor in the Video Processing section. State 1 then clears the second and third stages of the X and Y Shift Registers. The first section does not have to be cleared since it will be loaded with new data anyway. State 2 does nothing.

State 3 loads the Reference Height Counter with the height of the current Reference Character. This value is contained in the CPM at the address being selected by the CPM Address Counter. This is the first of the two words describing the Reference Characters.

State 4 then issues INC CPM CTR1 (not) which steps the CPM Address Counter ahead to the next CPM address. This CPM location contains the second word describing the current Reference Character. This information will be needed shortly.

State 5 issues the signal LOAD XY1(not) which becomes LOAD XYSR(not). This loads the X and Y Shift Registers with a plane of the Unknown and Reference Characters. If it is the first time that State 5 has been executed since State 0, then the bottom plane of the Unknown and Reference Character will be Loaded. Each subsequent time State 5 is executed without going through State 0, the next higher plane will be loaded. The trailing edge of LOAD XYSR(not) will cause the Scan Counter to start issuing the-burst of 27 pulses.

State 6 creates DEC CTRS(not) which causes the following changes. The Reference Alphabet Address Counter is decremented by DEC RCTR(not). The URAM Address Count-r is incremented by INCURCTR(not). The Reference Height Counter is decremented by DEC CTRS. The Unknown Height Counter is decremented by DEC UNCTR(not). These actions select the next planes of the Unknown and Reference Character and they subtract one from the counters which are keeping track of the number of planes contained in the Reference and Unknown Characters. The Recognition process cannot be completed until all the planes have been loaded and compared. The taller character, therefore, controls how many times the load and shift sequence must be repeated. States 7, 8, and 9 perform no operations.

State IO involves some decision making. It also is a stall state where the Sequencer awaits the completion of the shifting process. When the Sequencer reaches State 10, the "K" input to 22U is taken high which allows 22U to reset. This locks the clock up at 10V and prevents the Sequencer from going any further. The Sequencer will stay in this state until the X-Y Shift Registers have finished. This will be indicated by the signal XY SHIFTING(not) on 22U-4 which will go high allowing 22U to set and the clock to again reach the Sequencer. When State IO was generated, the toggle input to 14Y was taken low in preparation for setting it. When the stall has been completed, the Sequencer tries to clock ahead to State 11. However, the Load State flop, 14Y,

checks to see whether the comparison process is complete. so far, only one plane of both the Reference and Unknown Characters has been compared. Neither the RH COMP or UH COMP signal will be created, thus 14Y will set on the trailing edge of State 10. This forces the State Counter to load the number 5, thus returning to State 5. The State 5 signal, LOAD XY1 (not) will immediateby reset 14Y,

The Sequencer then repeats States 5 through 10, goes back and does 5 through 10 again, etc. This looping is repeated until both the RH COMP and UH COMP conditions occur, thereby preventing 14Y from setting at the end of State 10. This makes the Sequencer load and shift the required number of planes depending on the height of the taller character.

The Sequencer will then continue through the remaining steps. At State 11, the X and Y Shift Registers will be loaded one last time (with zeroes) and the burst of 27 issued again. This allows the last plane of the characters to be compared in the third stage of the X and Y Shift Registers. State 12 again stalls the Sequencer until that last burst of 27 pulses has caused the X-Y Shift Registers to fully shift.

State 15 clears the URAM Address Counter causing the bottom plane of the Unknown to be selected. It also clears the Unknown Height Counter,

The next clock pulse overflows the State Counter which then goes back to State 0. This is the end of one Sequencer cycle. The next Reference Character will now be compared with the same Unknown. Either of the two modes may occur

during this next pass. Each overflow and return to State 0 indicates one Reference Character has been considered and accepted or rejected-

Abort is the second possible mode for the Sequencer. It is encountered when it becomes obvious midway through the comparison process that the current Reference Character is a worse match than a previous match was. This is the case when the error count for the current Reference Character exceeds a previously established low. Further comparison of the current Reference Character can only serve to increase the total error count, so why continue? Provisions have been made to end comparison once an excessive error count is detected,

The comparison process starts out and proceeds the same as normal comparison did. The Sequencer steps down through State 10, loops back to 5, down through 10, loops back, etc. Each time the X-Y Shift Registers are done shifting, as signalled by XY SHIFTING, the Evaluation circuitry compares the current error total against the previously recorded low value, If the error count of the current comparison exceeds that number, the Evaluation circuitry sets the ABORT(not) flag. This creates the signal NO COMPARE. The next time the Sequencer loops back and passes through State 5, the HOLD flop will set, This forces the Sequencer to State 6 where the DEC CTRS(not) signal quickly increments the Reference

Address Counter past the remainder of the Reference Character. When RH COMP signals that the remainder of the character has been skipped, the HOLD flop releases the Sequencer to count through the remaining States and overflow. Thus, Abort takes place after the Sequencer has looped several times and made a partial comparisen of the Reference and Unknown Characters.

In order to identify one Unknown Character, the Sequencer will go through one cycle for each Reference Character, One cycle is completed each time the Sequencer overflows.

Every time the Sequencer went through State 3 a check was made to see if the entire Reference Alphabet had been completed yet. This will occur once all 64 characters in the Reference Alphabet have been compared with the Unknown. This condition is searched for by 17X-3 which will go high when the end of alphabet is detected. END ALPHA will allow 17U-3 to reset thereby ending the Recognition Process. The Character Identification process is also ended and the ASCII code in the BEST ID latches represents the character which best resembled the Unknown.

4-6. EXECUTIVE MACRO - OVERVIEW. The Executive Macro provides overall coordination of the processes required to fulfill the purposes of the ALPHA. Each machine function is performed by a macro which is completely dedicated to that function. The Executive Macro circuitry consists of several subcircuits which are described in the subcircuit portion of this section. These subcircuits are configured so as to permit the execution of an operating program. This is a logical series of instructions, tests, and decisions which provide control of the following:

The process of scanning.

Synchronizing justification and recognition.

Storing and editing scanned characters.

Code converting the data prior to output.

Synchronizing output devices,

Initiating, controlling, and detecting mechanical motion.

Internal communication with switches, LEDs, and keyboard,

Internal communications with the Core Memory.

Communication with any on-line interface.

Each of these instructions, tests, and decisions is described in detail in the following paragraphs:

a. General Operation. - The Executive Macro consists of several subcircuits which are structured to provide the ALPHA with overall direction of its functions. One vital portion is the Executive Macro Memory made up of 16-bit instructions in some multiple of 256 instructions. These instructions Provide direction to the Executive Macro Logic as to which

signals to issue, which tests to perform, and, depending on the result of the test,, which instruction to execute next. This logical sequence of instructions is the Operating Program for the ALPHA. It is stored in PROMs on a separate board and is not field alterable. Any changes to or updating of this Operating Program must be accomplished through replacement of the Executive Macro Memory card with another card containing PROMs with the desired program version.

The Operating Program has seven basic types of instructions. These seven types and the number of the paragraph containing a fuller description of each are as follows:

(1) LOAD/LDR Instructions

(2) PULSE Instructions

(3) ARITH (INC/INCR) Instructions

(4) JMP/JMPS Instructions

(5) TST Instructions

(6) CMP/CMPR Instructions

(7) XFR Instructions

The format of these groups is shown by the Instruction Word Summary illustration in Figure 4-45.

(1) LOAD/LDR Instructions. - The LOAD/LDR instructions are selected whenever the first three instruction word bits (IRO-2) are in a 011 state. The LOAD instruction (IR3 low) causes the 8 least significant bits (IR8 through IR15) of that same instruction to be loaded into the register designated by IR Bits 4-7. The LDR instruction (IR3 high) causes

TST	0	1	0		WHAT	TST TRUE ADR
XFR	1	1	0	0	RAM	TO WHERE (Bit 3 = Bit 13)
CMP	1	0	1	0	WHAT	TST TRUE ADR
INC	1	0	0	0	REG	OVERFLOW ADR
LOAD	0	1	1	0	REG	DATA
IMP	0	0	0	0	ADR OF	NEXT INST
IR BIT#	0	1	2	3	4 5 6 7	8 9 10 11 12 13 14 15 LSB
JMPS	0	0	0	1	RAM	NOT USED
LDR	0	1	1	1	RAM	DATA
INCR	1	0	0	1	RAM	OVERFLOW ADR
CMPR	1	0	1	1	RAM	DATA/NOT USED (Depends on Compare MUX)
XFR	1	1	0	1	RAM	FROM WHERE (Bit 3 = Bit 13)
				0	SET RST TOG STB	(May be Combined)
PULSE	0	0	1		4 5 6 7 8 9 10 11 12	
				1	PLB PLA	(May be Combined)

Figure 4-15. - Instruction Word Summary

the 8 least significant bits (IR8 through IR15) of that same instruction to be loaded into the RAM designated by IR bits 4-7.

Further detailed information concerning the operation and purpose of the individual instructions within this group is provided in Figures 4-16 through 4-21. (See end of chapter.)

(2) PULSE Instruction. - The PULSE instruction is selected whenever the first three instruction word bits (IRO-2) are in a 001 state. The PULSE instruction may issue 44 separate and distinct pulses. The instruction is divided into two major groups. Refer to the Pulse Instruction Word Format illustration for a graphic view of this instruction. The selection of one or the other major group is controlled by the status of IR3. When IR3 is in the 0 state, the major group selected contains four sub-groups known as SET, RESET, TOGGLE, and STROBE. When IR3 is in the 1 state, the major group selected contains two sub-groups known as PLA and PLB.

Each of the sub-groups is controlled by three of the IR bits. For example, when IR3 is at a zero, the SET sub-group is controlled by IR4, IR5, and IR6. There are eight possible combinations of these three bits. When all three are at 0, no pulse is issued from this sub-group. Each of the other combinations causes one of the pulses from this group to be issued. The same situation exists for the RESET, TOGGLE, and STROBE &b-groups. The construction of the instruction word allows each sub--group to act independently of the other three. Thus instruction words may be constructed which cause

only one pulse from one sub-group to be issued. Other instruction words may issue two pulses at the same time, one each from two different sub-groups. Similarly, three or four pulses may be issued at the same time. No two pulses will be generated from the same sub-group.

When IR3 is at a 1, the other major group is selected, thus pulses may be issued from the two sub-groups PLA and PLB. Construction of the instruction word allows for the issuance of one or two pulses from this major group, one from each of the sub-groups.

It is important to note that no one instruction word can cause pulses to be issued from both major groups at the same time.

Further detailed information concerning the operation and purpose of the individual instructions within this group is provided in Figures 4-22 through 4-24. (See end of chapter.)

(3) ARITH (INC/INCR) Instructions. - The ARITH instructions are selected whenever the first three instruction word bits (IRO-2) are in a 100 state. The INC instruction (IR3 low) causes the register designated by IR4 through IR7 to be incremented once each time the instruction is executed. If an overflow occurs, a conditional jump is made to the address designated by the 8 least significant bits. Overflows are detected by the AR0 output from the selected register. If no overflow occurs, the next sequential instruction is executed. The INCR instruction (IR3 high) causes the RAM designated by IR4 through IR7 to be incremented once each time the instruction is executed.

An overflow will cause a conditional jump to the address designated by the 8 least significant bits. If no overflow occurs, the next sequential instruction will be executed.

Further detailed information concerning the operation and purpose of the individual instructions within this group is provided in Figures 4-25 through 4-27, (See end of chapter.)

(4) JMP/JMPS Instructions. - The JMP/JMPS instructions are selected whenever the first three instruction word bits (IR0-2) are in a 000 state. The JMP instruction (IR3 low) causes an unconditional jump from the current program address to a new address designated by the 12 least significant bits of the instruction, The four most significant bits of these 12 (IR4-7) indicate which of the Program PROMs shall be selected while the 8 least significant bits (IR8-15) indicate which of the 256 locations within that PROM shall be selected. The JMPS instruction (IR3 high) causes an unconditional jump from the current program address to a new address which is found in the RAM designated by IR4 through IR7. The address found in the RAM is only 8 bits wide so it can only specify a jump to an address within the currently selected PROM. The 8 least significant bits of the JMPS instruction serve no purpose.

Further detailed information concerning the operation of these instructions is provided in Figures 4-28 through 4-30.

(5) TST Instruction. - The TST instruction is selected whenever the first three instruction word bits (IR0-2)

are in a 010 state, TST allow a check to be made on the status of 32 separate logical points within the ALPHA, If the event bring tested is true (logical one), a conditional jump is executed to the address specified by the 8 Least significant bits (IR8-15) of that instruction. If the test is false, the next sequential instruction is executed. The tests are divided into four groups which are selected by IR3 and IR4. Each of these groups can test 8 separate and distinct functions. IR5, IR6, and IR7 are decoded to distinguish which of the eight functions will be tested within the group selected by IR3 and IR4.

Further detailed information concerning the operation and purpose of the individual instructions within these groups is provided in Figures 4-31 through 4-34. (See end of chapter.)

(6) **CMP/CMPR Instructions. - The CMP/CMPR instructions** are selected whenever the first three instruction word bits (IRO-2) are in a 101 state. The CMP instruction (IR3 bow) is actually an extension of the TST instruction with two additional groups of 8 tests allowed. If the test is true, a jump will be made to the program address designated by the 8 least significant bits of the instruction. The CMPR instruction (IR3 high) allows a magnitude comparison to be made between the output of the Compare MUX and the data in the selected RAM. The CMPR instruction causes the contents of the selected RAM to be loaded into the Accumulator. This is then compared with the data selected by the Compare MUX.

The Compare MUX must have been previously set as to which of its four input sources it will pass to the Comparator. The four possible sources are the Instruction Register bits (IR), the Line Buffer (OBFR), Keyboard (KBD), or Compare Latch (RAMC). The result of the comparison can only set the GRATR or EQUL latches. These must be tested later by a separate TST instruction in order to determine whether the output from the MUX was greater than, equal to, or by default less than the Accumulator value.

Further detailed information concerning the operation and purpose of the individual instructions within these groups is provided in Figures 4-35 through 4-38. (See end of chapter.)

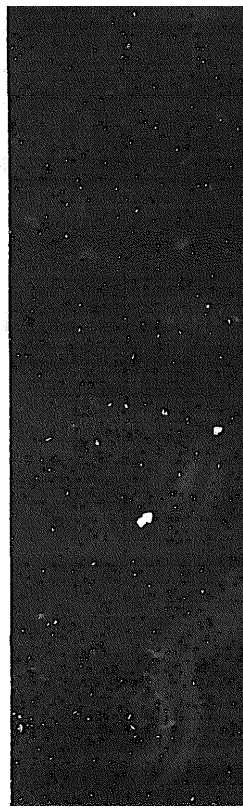
(7) XFR Instruction. - The XFP instruction is selected whenever the first three instruction word bits (IRO-2) are in a 110 state. The instruction provides for bidirectional transfer of data between the Core Memory and the RAMs of the Executive Macro. The direction of transfer depends upon the state of IR3. When IR3 is at the 0 state, transfer is made from the selected RAM to the Core Memory Module. This data may represent a portion of an address or it may be a portion of the actual data word which is to be written into memory. The reason that it may be only a portion of the address or data is because the memory requires a 12 bit address and can store a 12 bit wide word. The output from the RAM is only 8 bits wide. The address or data word must, therefore, be established in two portions, the high order 4 bits, then the low order 8 bits. When IR3 is at the 1 state, the transfer

operation takes place from the Core Memory back to the selected RAM. This transfer must also take place in portions, again due to the data lines being only 8 wide. Note that whenever 12 bit addresses or operands are used, the high order operation must be performed first.

Further detailed information concerning the operation and purpose of the individual instructions within this group is provided in Figures 4-39 and 4-40. (See end of chapter,)

b. Subcircuit Operation. - There are several subcircuits that may be described before the overall Executive Macro operation is described, In the following descriptions, all logic referenced can be found on the Executive Macro Main Board (if the IC number consists of a number followed by a letter) and on the Executive Macro P.C. Board (if the IC number consists of the letter U followed by a number). These subcircuits are:

(1) State Sequencer
(2) Instruction Decoder
(3) Instruction Register
(4) Program Counter
(5) IR/RAM Multiplexer
(6) Accumulator
(7) RAM
(8) Compare Multiplexer
(9) Comparator
(10) Compare Latch
(11) INC Instruction Decoder



(12) LOAD/LDR Instruction Decoder

(13) PULSE Gates

(14) TEST Gates

(15) System Reset and Power-On

The subcircuits are described in detail in the following paragraphs-

(1) State Sequencer. - The State Sequencer consists of a 74164 8 bit shift register (U1), a control flop (U6), and several associated gates, The State Sequencer is responsible for instruction execution timing. The State Sequencer has two modes of operation, one occurring whenever a Jump occurs (conditional or unconditional) and the other mode occurring for non-Jump instructions.

The State Sequencer operates as follows during the non-Jump instructions. Since the State Sequencer is a free-running circuit, this description will jump into the loop at the time when the control flop (U6) is reset. (Refer to the Executive Macro State Sequencer Timing Diagram, Figure 4-41, for non-Jump.) The numbers in parenthesis during this description refer to the circled numbers on the Timing Diagram, With the control flop (U6) reset, the State Sequencer (U1) is clamped clear (1). Since all the outputs of the State Sequencer are low, the "Qe" output causes the "3" input of the control flop to be high. The next rising edge of the clock causes the control flop to set (2). This removes the clear from the State Sequencer. The "Qe" output is inverted and applied to the data input of the Sequencer

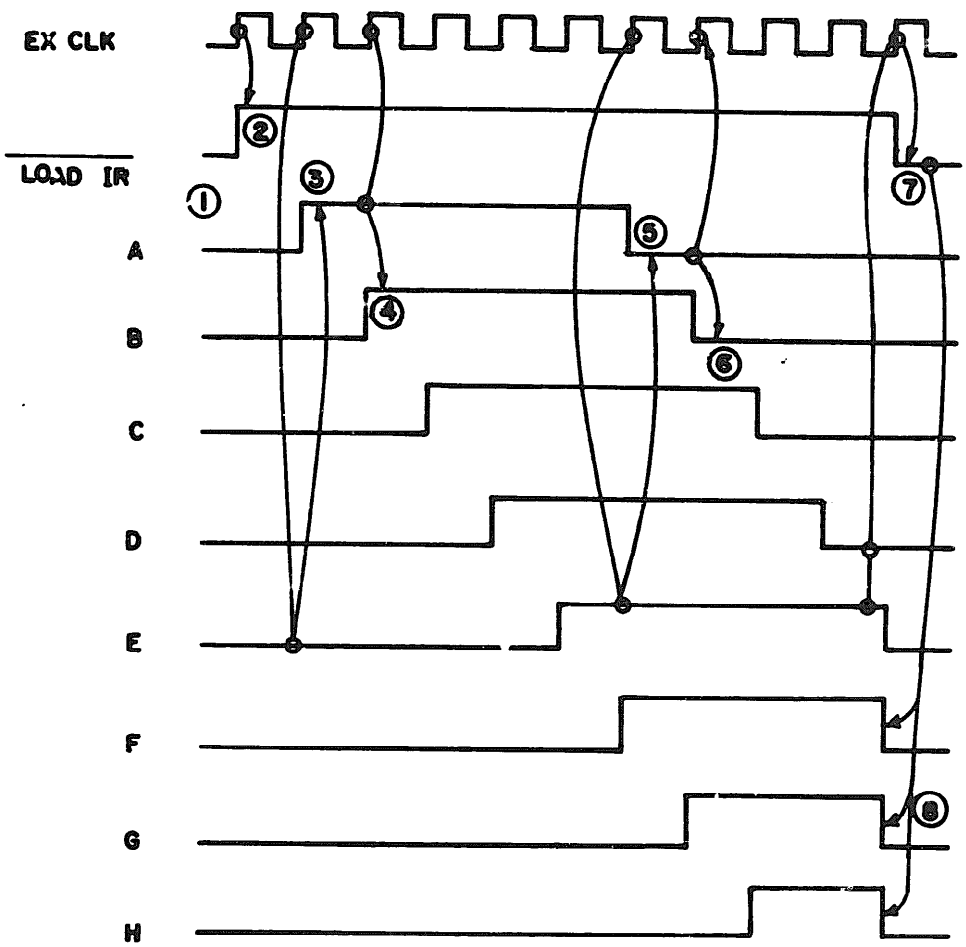


Figure 4-41. - Executive Macro State Sequencer Timing Diagram (Non-Jump)

holding it high. The next rising clock sets the first output, "Qa", high (3). The next clock pulse causes the high from the first stage to be transferred to the second (4). The first stage remains set because the data input is still high. This is repeated three more times thereby setting Qc, Qd, and Qe. With the Qe output now high, the data input to the State Sequencer is taken low. The next rising edge of the clock causes all stages to shift, however, the first stage is now Loaded with a low (5) ending state "A". The next clock shifts the zero into the second stage ending state "B" (6). Two more clocks will cause states "C" and "D" to end. This sets up the criteria for ending one non-Jump sequence. The Qd low and Qe high condition is ANDed by a portion of U5 causing the input to the control flop to go low, The next clock edge causes the control flop to reset (7) which in turn reapplies the clear to the State Sequencer and ends all the states (8). This completes one cycle of the State Sequencer for a non-Jump instruction.

The State Sequencer operates as follows during a Jump instruction (see Figure 4-42). Initially, the same conditions exist where U6 is reset thus holding the State Sequencer at all zeroes (1), The clock then sets LOAD IR high (2). The first stage then loads with a high (3) which is progressively shifted right with each clock. At some time prior to "E" time, the CJMP flop (U16) will be set by the detection of an overflow, JMP, or CJMP condition. The set condition of U16 prevents the input to the State Sequencer

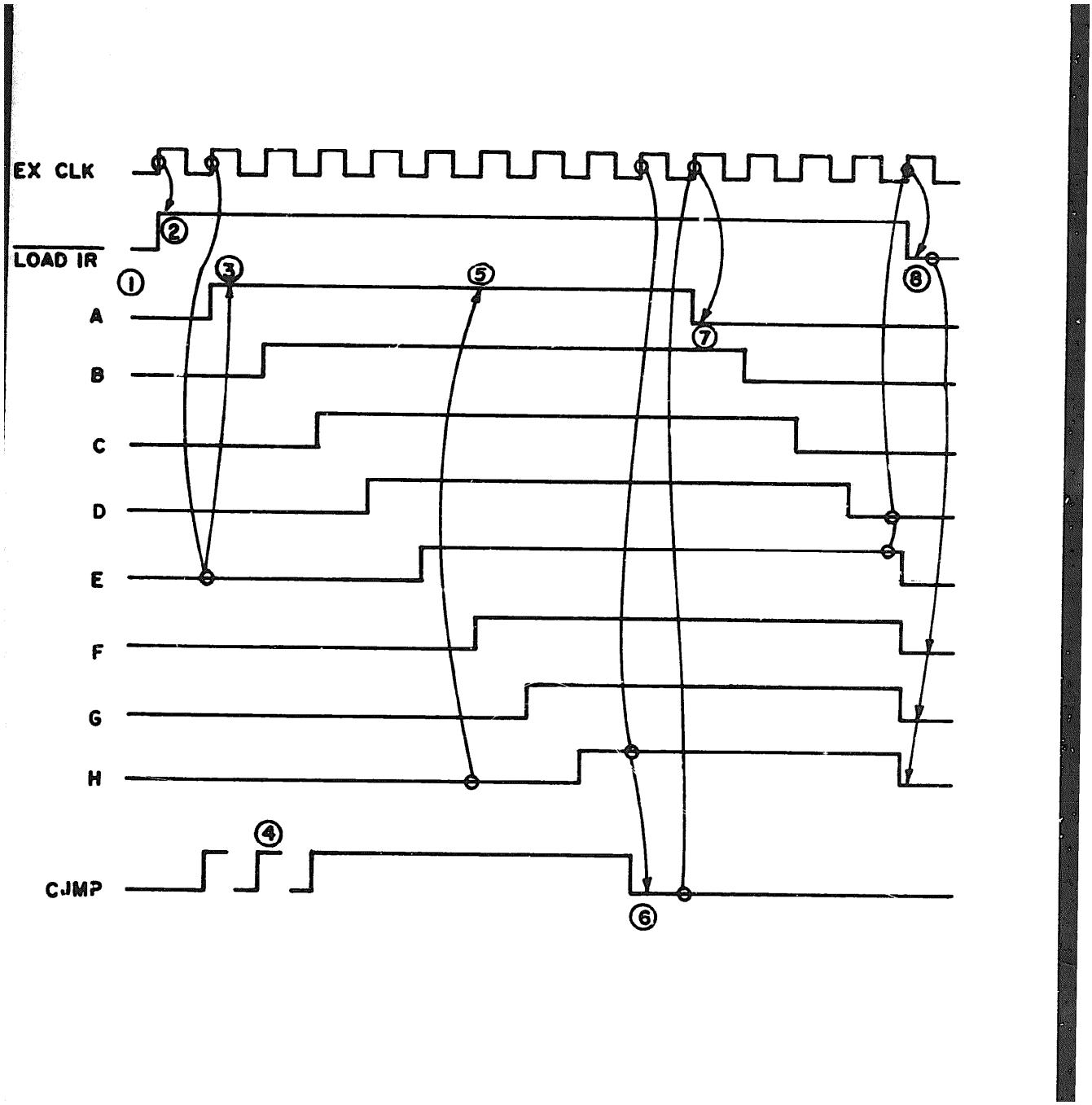


Figure 4-42. - Executive macro State Sequencer Timing Diagram (Jump)

from going low when "E" goes high as it did for a non-Jump instruction. The next clock pulse, therefore, does not start loading a low into the first stage and the Qa output remains high (5). The timing sequence will thus be stretched out from this point. The first stage will continue to be forced to load highs, When Qh is set, the "D" input to U16 will go high. The next clock will then set U16 (6) which will then remove the forced high on the input of the State Sequencer, The next clock will, therefore, load a low into the first stage of the Sequencer (7). This continues until finally the Qd output is low which allows the clock to reset U6 (8) which in turn resets the remainder of the states (9) by reapplying the clear to the Sequencer.

(2) Instruction Decoder. - The Instruction Decoder consists of two 7442 BCD to Decimal decoders (U3 and U32) that are used to select one of the major instructions. The major group will then be further broken down by other circuitry into an individual instruction. The Instruction Decoder is enabled during State "A" and may, in the case of a Jump instruction, stay active through State "G". Each of these major instructions feeds to further circuitry for breakdown into the individual instructions within that group. The TEST instruction enables the other decoder, U32, SO that one of the four GR TEST instructions can be selected by Instruction Register Bits 3 and 4.

(3) Instruction Register. - The Instruction Register is constructed with three 74174 hex D-latches (U34, U35, and U36) on the Executive Macro Memory Board. The

Instruction Register (IR) is loaded with a 16 bit instruction from the Program Memory during State Zero (LOAD IR) of the State Sequencer, The instruction will remain there until a new instruction is loaded in at the next LOAD IR. Since the instruction is in the register during the entire execution period, the register outputs can be used for control throughout the scanner.

(4) Program Counter. - The Program Counter consists of three 74193 presettable binary counters at U9, U10, and U11. The Program Counter is used to address instructions in the Program Memory Executive Macro Main Memory). Since the Program Counter is 12 bits wide, the maximum memory it can address is limited to 4096 (4K) words of 16 bits. At the conclusion of the instruction execution period, the Program Counter will always contain the address of the next instruction that is to be executed, If the current instruction being executed is a non-Jump type, then the Program Counter is incremented one location by LOAD IR to the next sequential Program address, A jump instruction will cause the IR/RAM multiplexer to load the Program Counter with a new Program address, The Program Memory is made up of 1702A EPROMs. Since each chip is 256 words of 8 bits, two chips are addressed together to give the 16 bit words needed for an instruction. The 8 least significant bits (EMAB0 through EMAB7) of the Program Counter addresses one of the 256 instructions contained in the chip set that is selected

by the four most significant bits (EMAB8 through EMAB11) of the Program Counter-

(5) **IR/RAM Multiplexer.** - The IR/RAM Multiplexer consists of two 74S257 quad/two input multiplexer with Tri-state outputs. The multiplexer will select either the Instruction Register outputs 8 through 15 or RAM 0 through 7, depending upon the select input status. The outputs of the multiplexer are connected to a bus that has two other outputs. The other outputs are from the External Memory and the Compare Multiplexer, The data on the bus can be inputted to either the Program Counter or the Accumulator, The IR/RAM multiplexer's outputs are always enabled except during a Transfer Instruction (XFER), Arithmetic Instructions will cause the IR/RAM multiplexer to select the data from the RAM so that it can be Loaded into the Accumulator. The Load Instructions will cause the IR/RAM multiplexer to select IR bits 8 through 15 which is then loaded into the Accumulator, All Jump Instructions will cause the Program Counter to receive the data selected by the IR/RAM multiplexer which is the RAM data if it is an Indirect Jump or IR bits 8 through 15 for the Direct and Conditional Jumps.

(6) Accumulator, - The Accumulator consists of two cascaded 74193 presettable binary up/down counters (U14 and U15) and an overflow/underflow memory (overflow flop U16). The Accumulator can except data from either the IR/RAM Multiplexer, the External Memory, or from the Compare Multiplexer.

The Accumulator is used for temporary storage during Load RAM (LDR), Compare (CMPR), and XFR Instructions. During INCR Instructions, the Accumulator is used to increment the contents of a selected RAM address. To increment the RAM, the data is read out of the RAM and loaded into the Accumulator where it is incremented or decremented, depending upon the status of the increment/decrement flop, then it is written back into the same RAM address. When an TNC/INCR Instruction causes an overflow or an underflow, the over flow flop is reset causing the current INC/INCR Instruction to be extended to a Conditional Jump. IR bits 8 through 15 determine the new address that is to be loaded into the Program Counter. Whether the INC/INCR Instruction is to be interpreted as an increment or decrement instruction is determined by the state of the increment/decrement flop (18P on the Main Wire-wrap Board). The increment/decrement flop has to be set to the desired state prior to the execution of an INC/INCR Instruction. A Pulse Instruction, either Set Inc (GRO-1) or Set Dec (GRO-2), is used to set the increment/decrement flop to the needed state.

(7) **RAM.** - The RAM consists of four 3101 64 bit Random Access Memories (U17, U18, U19, U20) and a RAM select flop (U30). The 3101 RAM can store sixteen words of 4 bits each. The RAM is used to store any data that is to be used by the Accumulator during either an Arith (INCR) or Compare (CMPR) instruction. It is also used to store the data and

addresses that are sent or received by the External Memory during a Transfer (XFR) instruction. All of the instructions that use the RAM require that a data word of 8 bits (1 byte) be stored or read from the RAM. Therefore, two 3101 RAMs must be addressed simultaneously, each contributing one half of the data word. The two sets of RAMs allow a maximum of 32 data words to be stored, with data words 0 through 15 stored in U18 and U19 and data words 16 through 33 stored in U17 and U20. The RAM select flop (U30) determines which set of RAMs is to be addressed. The status of the RAM select flop is set to the desired state by a Pulse Instruction, either Set RAM Select 0-15 or Set RAM Select 16-31. A Pulse Instruction must precede any instruction that has to address the RAM set that is not currently being addressed.

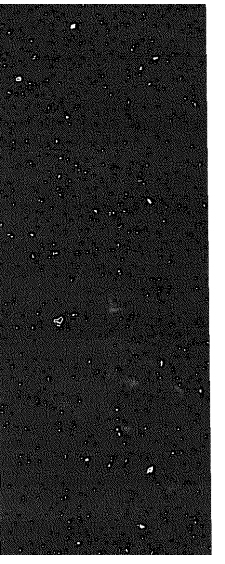
(8) Compare Multiplexer. - The Compare Multiplexer consists of four 74153 dual/quad input data selectors (11L, 12L, 13L, 14L) and two select latches (11M). The Compare Multiplexer is used to select which one of four data sources, the Instruction Register (IR 8-15). the Output Buffer (OBF 0-7), the Keyboard (KBD O-7), and the Compare Latch (RAMC 0-7), is to be outputted to either the Comparator or the Accumulator. The selection of the data sources is controlled by the select latches, which are loaded with IR bits 14B and 15B during a Pulse (CMP MX) Instruct ion. This instruction must precede the Compare (CMPR) Instruction. IR bits 14B and 15B

are decoded into four possible states; each state will select a different data source, with 15B being the least significant of the two bits.

(9) Comparator. - The Comparator consists of two 7485 four bit binary comparators (13M, 14M) and two 7474 D-type flops (12M) serving as the result latches. The Comparator allows for the direct magnitude comparison between the value in the Accumulator and the value of the data selected by the Compare Multiplexer. The results of the comparison are stored in the Result Latch where it can later be tested by a Test Instruction. Only the A greater than B (GRATR) and A equals B (EQUL) results are stored. To test for A less than B, two Test Instructions have to be executed since if A is not greater or equal to B, then A has to be less than B. It takes a minimum of three instructions to do a comparison between two values. First a Load (Set CMPMX) Instruction to select the source of the data that is to be inputted to the A side of the Comparater is executed. ThenI a test for GRATR followed by a test for EQUL is executed. If a GRATR is detected testing will end and suitable action will be taken. If no GRATR, then EQUL will be checked. If EQUL is detected, suitable action for that result will be taken. If no EQUL is detected, then A less than B must be assumed and the action taken will be based on that assumption.

(10) Compare Latch. - The Compare Latch consists of two 74193 presettable binary counters (26U, 20P) that are

used as latches. The Compare Latch is used when the two values that are to be compared reside in the RAM. One value is loaded into the Accumulator by a Pulse (PLB-4) Instruction and from there into the Compare Latch with a Pulse (PLB-3) Instruction. A Load (Set CMPMX) Instruction is used to have the Compare Multiplexer select the output of the Compare Latch (RAMC 0-7). The other value is loaded into the Accumulator by a Pulse (PLB-4) Instruction. A Compare CCMPR) Instruction can now be executed on the two values.



(11) INC Instruction Decoder. - The INC Instruction Decoder consists of a 7442 BCD to decimal decoder (11N) and a NAND gate (14N). The decoder is used to send increment or decrement pulses to certain registers. The register is selected by IR bits 5 through 7 of the INC Instruction. The decoder is enabled during the INC/INCR Instruction only if IR 3 of the instruction is at a logical zero. All the resultant pulses generated by the INC Instruction are used for incrementing or decrementing selected registers except Read Switch. The Read Switch output is used to shift the Switch Shift Register one place right. If the INC Instruction results in either an under or overflow, then a conditional Jump to the new Program address defined by IR bits 8 through 15 of the INC Instruction is executed.

(12) LOAD Instruction Decoder. - The LOAD Instruction Decoder consists of a 7442 BCD to decimal decoder (13N) and a 7400 NAND gate 14N). The decoder is used to select

the register in which data is to be loaded into. The decoder can select a maximum of eight different registers although only six are currently being used. IR bits 5, 6, and 7 of the LOAD Instruction are decoded to select one of the six registers. The decoder is enabled by gate 14N if IR 3 of the current LOAD Instruction is at a logical zero. IR bits 8 through 15 are used for any control information needed by the selected register.

(13) Pulse Gates. - The Pulse Gates consist of six 7442 BCD to decimal decoders (15M, 15L, 15S, 15P, 15N, 16S) and two 7400 NAND gates (14N), The Pulse Gates are used to send pulses to various areas throughout the scanner. There are a maximum of 44 possible pulse destinations. The pulses are divided up into six groups, Set, Reset, Toggle, Strobe, PLA, and PLB. PLA and PLB can only be used at the exclusion of the rest of the groups. IR 3 of the Pulse Instruction determines whether PLA and PLB are to be enabled or the four other pulse groups are enabled, IR 3 being a Logical one will cause PLA and PLB to be enabled. Four simultaneous pulses, one from each group (Set, Reset, Toggle, and Strobe), can be sent with one Pulse Instruction. If PLA and PLB are selected, two simultaneous pulses, one from each, can be executed with one Pulse Instruction. The destination of the pulses is selected by IR bits 4 through 15 of the Pulse Instruction. The pulses are low active and Last for a duration of 550 nanoseconds.

(14) Test Gates. - The Test Gates consist of six 74151 8 input data selectors (13P, 16N, 16L, 12N, 16M, 16P) and two 7400 NAND gates (16R). The Test Gates are used to test various flags and status bits throughout the scanner and cause a Conditional Jump if the result of the test is a logical one. The Test Gates are divided into six groups, GRO TEST, GR1 TEST, GR2 TEST, GR3 TEST, GR4 CMP, and GR5 CMP. Each group can test a maximum of eight different points throughout the scanner although not all of the Test Gates in each group are used. The test groups GR0 TEST through GR3 TEST are used only during the execution of the Test Instruction, The two remaining groups, GR4 CMP and GR5 CMP, are addressed during the execution of a Compare (CMP) Instruction only if IR 3 of the Compare Instruction is a logical zero. Only one of the Test Gates is enabled during the execution of either the Test or the Compare Instruction. IR 4 selects which one of the two Test Gates that are used for the Compare Instruction is to be enabled. A 7442 (U32) is used during the Test Instruction to decode IR4B and IR3 of the current instruction to select one of the four test groups, GR0 TEST through GR3 TEST, If either the Test or Compare Instruction finds a test true, at a Logical one, a Conditional Jump to the Program address specified by IR bits 8 through 15, of the current instruction, is executed.

(15) System Reset and Power-On. - The Reset Circuits provide Clear signals to many of the circuits within the system. There are two types of Resets, The first is

Power-On Reset, which is generated unconditionally whenever the Reset Switch on the Control Panel is toggled. It creates a Clear signal that, besides clearing various status flops and registers, also clears the Program Counter such that it is returned to the first instruction in the Program Memory. The other Reset is generated by an instruction generated by the Program, The PLA group of the Pulse Instruction has as PLA7 the signal GENERAL RESET(not) which, when executed, will issue a SYSTEM RESET(not). This will clear the status flops and certain registers, but will not cause the Program Counter to be reset to zero.

c. Circuit Operation. - The Executive Macro must follow a series of steps in order to select and execute each Program Instruction. First, an address is selected in the Program Memory (Executive Macro Memory). Then the instruction from that location is Loaded into the Instruction Register (IR). The instruction will remain there for the duration of the execution period following which a new instruction will be loaded into the Instruction Register,

The subcircuits are described in earlier portions of this section. In particular, the State Sequencer operation was described showing how the various states are created. Each of the states is responsible for one of the steps required for execution of the current instruction word. This description will briefly cover the order of events followed to execute an instruction word. It should be noted

that the Program Counter is set to the zero address by RESET, therefore, the Program will always be initiated from the first instruction of the Program Memory.

The first thing that has to be done before any instruction word can be executed is that the instruction word has to be selected and loaded into the Instruction Register where it can be decoded and the determination made as to which instruction word it is.

The State Sequencer generates a signal LOAD IR(not) which handles the task of selecting and loading the instruction word, The State Sequencer description showed how the State Sequencer Control Flop U6 would reset at the end of the Sequencer cycle. At that time LOAD IR(not) goes Low. This signal is sent to two places, the Program Counter on the same board and to the Instruction Register on the Executive Macro Memory Board, When the Control Flop U6 again sets, LOAD IR(not) returns high causing two things to happen simultaneously. At the Instruction Register, the Load inputs, pin 9 of U34, U35, and U36, will go high. These latches are positive edge triggered, thus they will load the data currently on their data input lines. This is the instruction word stored in the Program Memory at the address currently being selected by the Program Counter. The second thing that happens at this same time is that the UP Clock input on the Program Counter goes high. This causes the Program Counter to step ahead to the next address. It may seem

that the Executive Macro is trying to load an instruction word at the same time that it is selecting a new instruction, however, the PROMs of the Program Memory take a certain amount of time to respond to the newly selected address. This slow response provides sufficient time for the Instruction Register to complete its Load operation before the new data appears on its inputs. It is also the reason that the next instruction has to be selected so far in advance of the time it will actually be Loaded into the Instruction Register.

The State Sequencer will now start stepping through the states to execute the instruction which was just loaded into the Instruction Register. Two different sequences occur depending on whether a jump takes place or not.

A non-Jump type sequence will be described first. (See Figure 4-43.) These would be: LOAD, LDR, INC and INCR with no resulting overflow, CMP and TST with a false result, CMPR, and XFR.

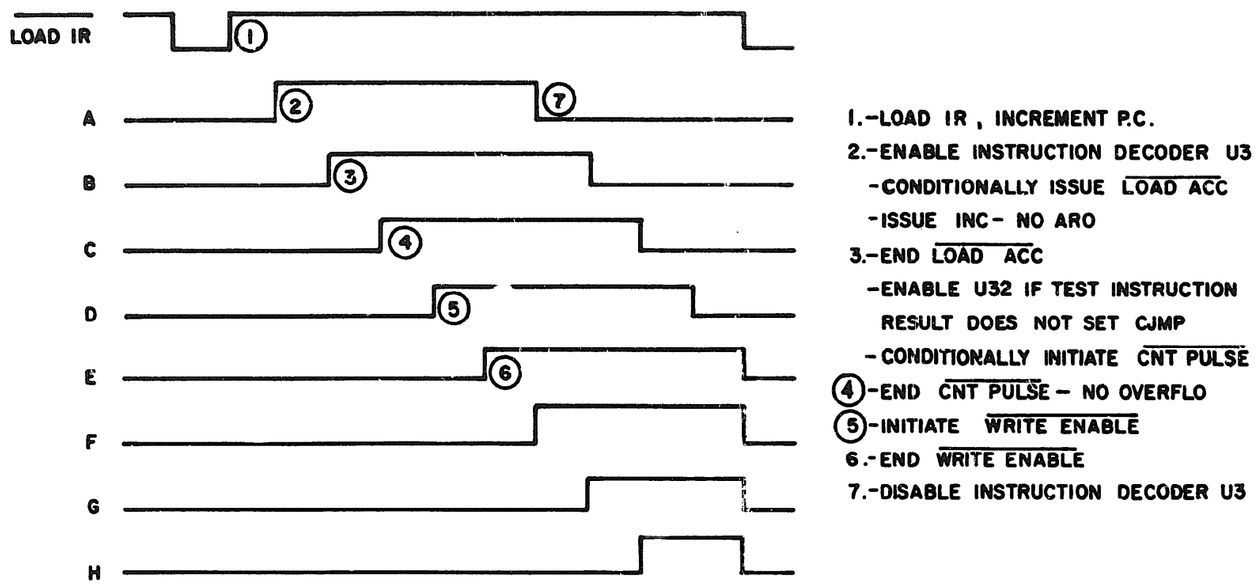
"A" state going high will enable Instruction Decoder U3, which determines which of the major instruction types is to be executed. I? the instruction word was an ARITH INC, the increment pulse will be issued to the selected register with no resultant overflow. If an overflow had occurred, a jump would have taken place. That condition will be described in the section detailing a jump sequence. Several of the instructions require that the accumulator be loaded. These instructions are ORed together at U21 and further gated with

IR3 to create the signal LDOAR(not) at U2-11. This signal is then gated with the “B” state to create LOAD ACC(not). Thus at the beginning of the "A” state the signal LOAD ACC(not) is initiated for those instructions which will load the Accumulator. The inputs to the Accumulator will be selected based upon the type instruction. For the INCR and CMPR instruct ions, the RAM inputs will be selected by the MUX. For LDR, the 8 LSB of the IR will be selected by the MUX. For XFR, the MUX is disabled and the data from the Memory Control Board on the IEMAB lines is enabled into the Accumulator.

The “B” state ends the LOAD ACC(not) signal, if it was initiated at state "A", thereby locking the data into the Accumulator. The “B” state will also enable the second half of the Instruction Decoder U32. If the current instruction is a TEST instruction, one of the groups will be selected. We assume here that the test would be false so CJMP is not set and no jump takes place. If the instruction is an ARITH INC, the signal CNT PULSE(not) will be generated at U23-6 and fed to the Accumulator in preparation for incrementing its contents.

The “C" state will end the signal CNT PULSE(not) causing the Accumulator to be incremented or decremented depending on the result of the Increment/Decrement flops of the Main Board Executive Macro circuitry. We are assuming no overflow.

The "D” state generates the signal WRITE ENABLE (not). Those signals which caused the Accumulator to be loaded



1.-LOAD IR , INCREMENT P.C.
2.-ENABLE INSTRUCTION DECODER U3
-CONDITIONALLY ISSUE LOAD ACC
-ISSUE INC- NO ARO
3.-END LOAD ACC
-ENABLE U32 IF TEST INSTRUCTION RESULT DOES NOT SET CJMP
-CONDITIONALLY INITIATE CNT PULSE
4.-END CNT PULSE- NO OVERFLO
5.-INITIATE WRITE ENABLE
6.-END WRITE ENABLE
7.-DISABLE INSTRUCTION DECODER U3

Figure 4-43. Sequencer Timing Diagram (Non-Jump)

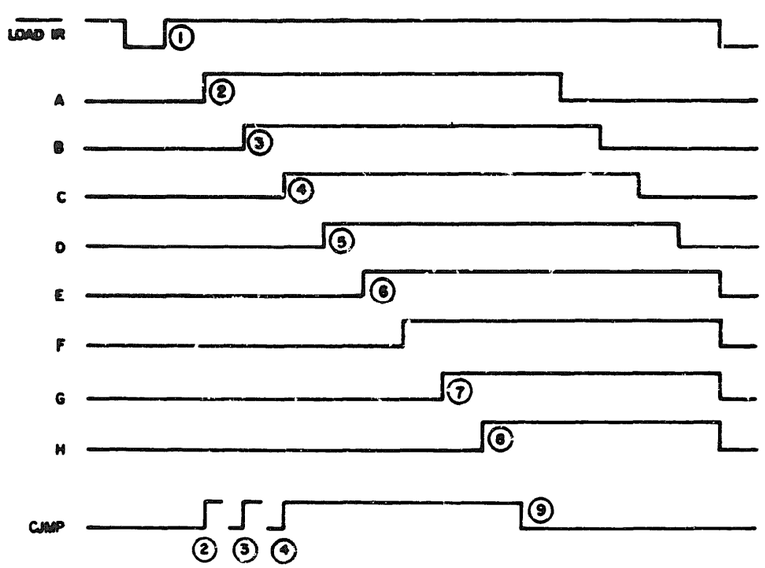
created the signal LDOAR(not) which is now gated with the "D" state to write the contents of the Accumulator into the RAM selected by the IR4, 5, 6, and 7 bits along with the RAM bank select flop U30.

The "E" state ends the WRITE ENABLE(not) by taking U23-9 low. This locks the data into the selected RAM.

The end of "A" state causes the Instruction Decoder U3 to be disabled causing further action on the instruction word to be discontinued. No operations will take place as the State Sequencer finishes its remaining steps, When the Sequencer finishes, the next instruction, the one currently addressed by the Program Counter, will be loaded into the Instruction Register and then the Program Counter wilt be stepped ahead to execute that next instruction.

A CJMP type instruction (Figure 4-44) is the other type of sequence. These instructions would be: INC and INCR with a resulting overflow, TST and CMP with true result, JMP, and JMPS. All of these will result in the CJMP flop being set which will then cause the extended sequence of the State Sequencer.

Initially, the same steps take place for the CJMP type instruction as for a non-jump. The end of LOAD IR(not) loads the instruction into the Instruction Register and then steps the Program Counter ahead to the next Program Address.



1.-LOAD IR., INCREMENT P.C.
2.-ENABLE INSTRUCTION DECODER U3
-SET CJMP IF JMP INSTRUCTION
-SET CJMP IF GR4 OR GR5 CJMP
-CONDITIONALLY INITIATE $\overline{\text{LOAD ACC}}$
-SET CJMP IF INC COUSES ARO
3.-END LOAD $\overline{\text{ACC}}$
-ENABLE U32 IF TEST INSTRUCTION SETTING CJMP
-CONDITIONALLY INITIATE $\overline{\text{CNT PULSE}}$
4.-END CNT PULSE SETTING $\overline{\text{OVERFLO}}$ @ CJMP
5.-INITIATE $\overline{\text{WRITE ENABLE}}$
6.-END $\overline{\text{WRITE ENABLE}}$
7.-END PROGRAM COUNTER - LOAD
8.-RESET $\overline{\text{OVERFLO}}$
9.-RESET CJMP

Figure 4-44. - Executive Macro State Sequencer Timing Diagram (CJump)

The "A" state enables the first part of the Instruction Decoder, U3. If the instruction is a JMP/JMPS, the CJMP flop is immediately set. Additionally, if it was the JMP instruction, the 4 most significant bits of the Program Counter are immediately set with the value of IR4 through IR7. If the instruction is a CMP type with a true result, the CJMP flop will be immediately set. If an INC instruction was issued, we are assuming here that it will cause an AR0 output from the incremented register which will set OVERFLO(not) which in turn sets CJMP. For the one instruction which will require that the Accumulator be loaded, INCR, the LOAD ACC(not) signal will be initiated. The RAM data will be selected via the MUX.

The "B" state will end the signal LOAD ACC(not) if it was initiated during "A" time thereby locking the data into the Accumulator. If the instruction is a TST, the second half of the Instruction Decoder will be enabled and, we are assuming here, will result in a true result which set CJMP via GRC JMP. For an INCR instruction, the CNT PULSE(not) signal will be initiated. Also, at this point the MUX outputs the 8 LSB of the IR to the PC for INC, INCR, TST, CMP, and JMP instructions. For a JMPS instruction, the RAM data is passed to the PC.

The "C" state will end CNT PULSE(not) if it was initiated during state "B" This will increment the Accumulator data

and, we are assuming here, set OVERFLO(not) which in turn sets CJMP.

Now CJMP has been set at one of three points depending on which of the instructions was being executed. This means that the Program Counter is going to be loaded with some new value which differs from the next sequential location it normal:, selects. Actually, the 8 LSB of the Program Counter are allowed to assume the value sitting on its inputs as soon as CJMP was set, again depending on which instruction set CJMP and when. Since the Program Counter is being changed, and since it has been explained that the PROMs of the Program Memory are slow to respond to the Program Counter, extra time has to be provided before the next instruction is loaded into the Instruction Register and executed. Thus, the extended State Sequencer operation takes place.

The "D" state initiates the WRITE ENABLE(not) signal to load the Accumulator contents back into the selected RAM for the INCR instruction.

The "E" state ends the WRITE ENABLE(not) signal thereby locking the data into the RAM.

The "G" state ends the loading of the 8 LSB of the Program Counter thereby locking the new address into it.

The "H" state resets the OVERFLO(not) flop U16.

The next EXCLK pulse after "H" is set causes CJMP to be reset.

The remaining steps taken by the State Sequencer allow the program PROMs to settle before the next instruction word is loaded into the Instruction Register.

4-7. CORE MEMORY AND OUTPUT CONTROL - OVERVIEW. - The ALPHA OCR is equipped with a core memory which the Executive Macro utilizes to store data such as Header Sheets, Scanning Parameters, Scratch Pad for Calculations and ASCII Characters from the Line Buffer. Also the Executive Macro -uses a portion of the core memory designated output buffer which it loads with the data to be output for the line just scanned- The Executive Macro controls all read/write operations with core except for the read operation from core to the output device. The Executive Macro will control the addressing, transmission, and reception of data with the core memory. The Executive Macro also initiates the circuitry to automatically take data from core and "hand shake" with the interface electronics, while simultaneously allowing the Executive Macro to access other parts of core,

a. General Operation, - When the Executive Macro addresses the core memory, the source of the address bits will come from the Executive Macro RAMs. When data is taken from the core memory by the Executive Macro, it will be transferred to the Executive Macro Accumulator. These operations are accomplished by the Executive Memory Control Logic, The output control Logic, once started, will take data from the core

memory at some transfer it to the interface circuits, increment the address and transfer that data to the interface circuits. Data flow will continue until the data character from core is a terminator (all ones), at which time outputting is terminated.

b. Subcircuit Description (Fig. A-20). - The core memory and output controller circuits are divided into three main sections: one for Executive Memory Operation; one for Output Control Operation; and another is circuitry used for both these operations, in a time-shared fashion. Each section is subdivided as follows:

(1) Time shared circuitry,-

(a) Memory Access Logic (U34, U37, U42, U44)

(b) Memory Address Multiplexer (U15, U19, U23, U29)

(2) Executive Memory Operations.-

(a) Instruction Decoders and Latches (U33, U41, U39)

(b) Executive Memory Address Registers (U3, U17, U21, U35)

(c) Executive Memory Data Out Registers (U1, U7, U11)

(d) Executive Memory Data In Registers (U5, U6, U14)

(3) Output Control Operation

(a) Output Control Logic and Terminator Detect U30, U31, U35, U2)

(b) Output Control Address Registers U18, U22, U26)

(c) Output Control Data Register (U24, U28)

The time shared circuitry will be discussed first.

(1) Time Shared Circuitry. -

(a) Memory Access Logic (U34, U37, U42, U44) - This logic is used in conjunction with the Executive Macro Instruction cycle timing in order to provide the correct timing for the core memory whenever data is written in or read out of it. -Basically, the only signal generated is xMEM STRT which is a 60 ns. pulse needed to start a read or a write memory cycle, The conditions which will cause a memory access are realized at U37. These are:

(1) I/O Cycle - when the output control wishes to read from memory.

(2) Load X Add Lo - when the Executive Macro loads the low order Executive Memory Address Register, a read from memory will occur.

(3) WRIT X DLO - when the Executive Macro loads the low order Executive Memory Data Out Registers a write to memory will occur and the Executive Memory Address Register will be incremented,

(4) READ X DLO - when the Executive Macro transfers the low order Executive Memory Data In Register bits to the accumulator a read will occur for the next Executive Memory Address Register value.

The detailed timing diagram, Figure 4-47, shows the relationship between the instruction cycles and the signal XMEM STRT.

(b) Memory Address Multiplexer (U23, U19, U15, U29) - Since the Output Control Logic and the Executive Memory Control Logic must both access different addresses in core, there are two 12 bit registers which must be multiplexed to the core memory address lines. The multiplexers which accomplish this are U23, U19, U15, and U29. When the signal I/O cycle is high the I/O ADD0 0-- 11 lines from the Output Control Address Register will be gated to the core memory address lines. When I/O cycle is low the XADDO 0-->11 lines from the Executive Memory Address Register will be gated. The signal I/O cycle is controlled by the Output Control Logic. It will be high when the Output Control Logic wishes to make a memory access.

(2) Executive Memory Operation. - The Executive Macro'0 will access the core memory by utilizing the Executive Macro to read or write data to the core memory. The main section consists of instruction decoders and an instruction latch-

(a) Instruction Decoders and Latch - The Instruction Latch U39 is used only to enable the Output Control Logic when the flag "enable" is raised, via a "Load 5" instruction. The Instruction Decoders, U41, U33, U37, U34, U42, are used to decode "XFR" instructions issued by the Executive Macro. The mnemonics for the instructions and

their use are as follows:

(1) LOAD XADD HI - Loads RAM data into the 'Hi Order Executive Memory Address Register.

(2) LOAD XADDLO - Loads RAM data into the Lo Order Executive Memory Address Register and accesses memory for a read operation.

(3) WRITE XD HI - Loads RAM data into the Hi Order Executive Memory Data Out Register.

(4) WRITE XD LO - Loads RAM data into the Lo Order Executive Memory Data In Registers and accesses memory for a write operation and increments the value in the Executive Memory Address Register,

(5) READ XD HI - Transfers the data in the Hi Order Executive memory Data In Register to the Executive Macro Accumulator via the "IEMAB O-->3" lines.

(6) READ XD LO - Transfers the data in the Lo Order Executive Memory Data In Register to the Executive Macro Accumulator via the "IEMAB O-->7" lines, also increments the Executive Memory Address Registers and access memory for a read operation.

(7) LOAD I/O DD HI - Loads RAM data into the Hi Order Output Control Address Register.

(8) LOAD I/O ADD LO - Loads RAM data into the Lo Order Output Control Address Register and starts the Output Controller's operation.

(b) Executive Memory Address Registers (U17, U21, U25). - U17 is the Hi Order Executive Memory Address Register; it is loaded with RAM data O-->3 at the instruction "LOAD X ADD HI". U21, and U25 are the Lo Order Executive Memory Address Registers; they are loaded with RAM data O-->7 at the instruction "LOAD X ADD LO". The value held in these registers is incremented during the instructions "READ XD LO" and "WRIT XDLO" in order to set up the address for a sequential read or write operation.

(c) Executive Memory Data Out Register. - U1 is the Hi Order Executive Memory Data Out Register; it is loaded with RAM data O-->3 at instruction "WRIT XD HI". U7 and U11 are the Lo Order Executive Memory Data Out Registers; they are loaded with RAM data 0-->7 at instruction "WRIT XD LO". The output of the Executive Memory Data Out Register hangs on the tri-state bidirectional bus for data going to or from the core memory. These outputs will be enabled onto the data bus whenever the core memory does not have data available to be read out of it.

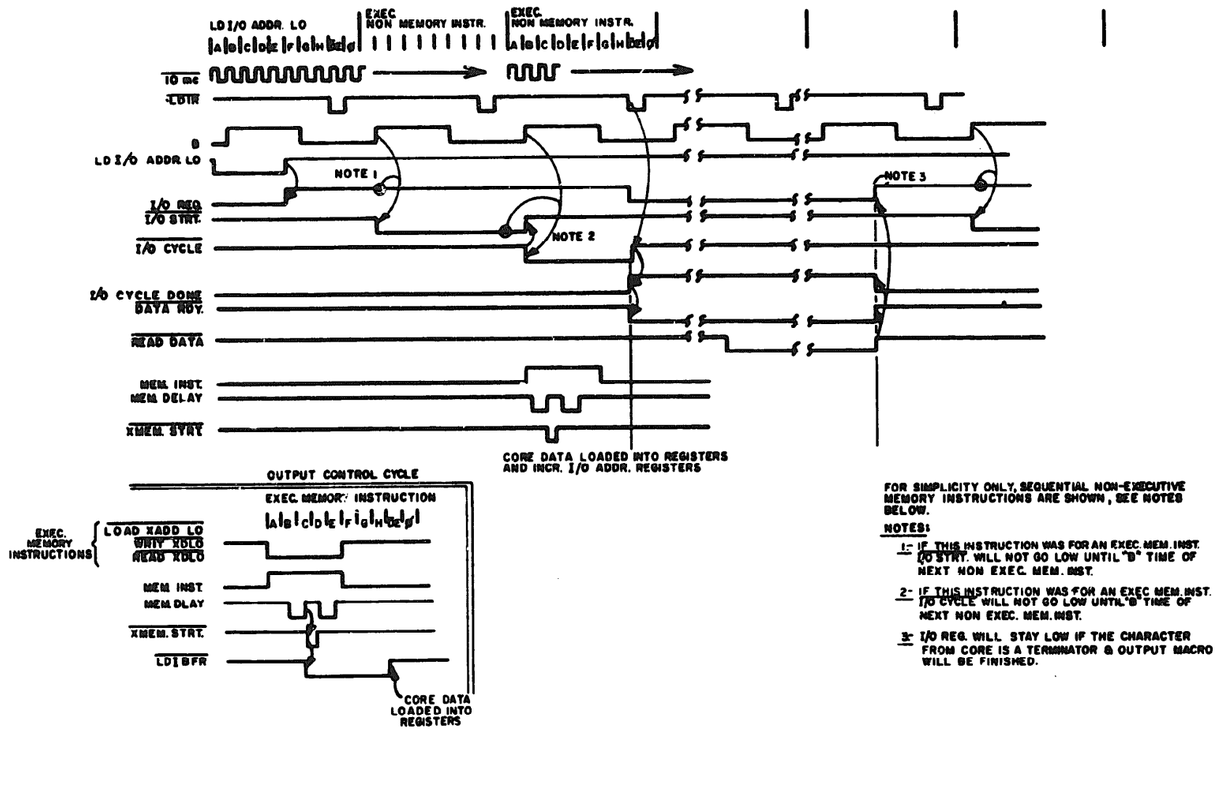
(d) Executive Memory Data In Register. - U5 is the Hi Order Executive Memory Data In Register; it will be loaded with the core memory's Hi Order data bits during an Executive Memory read operation via the signal "LDIBFR". U6 and U14 are the Lo Order Executive Memory Data In Registers; they will be loaded with the core memory% Lo Order data bits during an Executive Memory Read Operation also

via the signal "LDIBFR". The Hi Order Executive Memory Data In Register will be transferred to the Executive Macro Accumulator during the instruction "READ XDHI". The Lo Order Executive Memory Data In Registers will be transferred to the Executive Macro Accumulator during the instruction "READ XD LO".

At this point it should be noted that neither the signals "READ XDHI" nor READ XDLO" will directly cause these registers to be loaded. The previous "LOAD XADD LO" instruction or previous "READ XDLO" instruction are the instructions which load the Executive Macro Data In Register.

(3) Output Control Operations. - As was previously mentioned, the Output Control Operation must read data from core memory and transfer it to the Output Data Registers and transfer this data in a "hand shake" manner to the Interface Circuits This Output Operation must be accomplished without interfering with Executive Memory Operation. To do this, it must detect at the beginning of each Executive Macro Instruction Cycle whether the Executive Macro is going to access the core memory, If an Executive Memory Operation is going to be performed the Output Control Operation must halt until the next Non-Executive Memory Instruction Cycle. The circuit which controls this operation is the Output Control Logic.

(a) Output Control Logic (U30, U31, U35, U2). - For ease of explanation refer to the timing diagram (Fig. 4-45).



FOR SIMPLICITY ONLY, SEQUENTIAL NON-EXECUTIVE MEMORY INSTRUCTIONS ARE SHOWN, SEE NOTES BELOW.

NOTES:

1- IF THIS INSTRUCTION WAS FOR AN EXEC. MEM. INST. I/O STRT. WILL NOT GO LOW UNTIL "B" TIME OF NEXT NON EXEC. MEM. INST.

2- IF THIS INSTRUCTION WAS FOR AN EXEC MEM. INST. I/O CYCLE WILL NOT GO LOW UNTIL "B" TIME OF NEXT NON EXEC. MEM. INST.

3- I/O REG. WILL STAY LOW IF THE CHARACTER FROM CORE IS A TERMINATOR & OUTPUT MACRO WILL BE FINISHED.

Figure 4-45.- Executive Macro and Output Control Cycles Timing Diagram

To initiate the Output Control Logic circuitry, the Executive Macro will issue a "LOAD I/O ADD LO" instruction. This instruction will cause an output cycle to occur. Each "READ DATA" pulse from the interface circuitry will cause subsequent output cycles until the terminator character is detected. U2 will control this operation.

The signal "XFRO-7" signals the Output Control Logic that an Executive Memory Cycle is about to occur. This will hold off the lowering of "I/O STRT" until the next Non-Executive Memory Cycle. Once an Output Operation is initiated the signal "I/O Req" 'will go high. During the next Non-Executive Memory Instruction the signal "I/O STRT" will go low, At the next Non-Executive Memory Instruction after this, the signal "I/O cycle" will go low and cause a memory access for a read operation. Once data is loaded into the Output Data Registers via "I/O cycle" going high, then the signal "I/O cycle done" will go high and "DATA RDY" will go low signalling the interface circuitry that data is ready to be transferred to it. The interface circuitry will issue a "READ DATA" pulse which will transfer the data in the Output Data Latches to the interface circuits and also initiate another Output Cycle if U2-6 does not detect the all ones character (Hi Order memory data bits). If the all ones character (terminator) is present then the Output Operation is terminated.

(b) Output Control Address Register (U18, U22, U26). - U18 is the Hi Order Output Control Address Register. It is loaded with RAM data 0-->3 at instruction "LOAD I/O ADD HI" U22 and U26 are the low order output Control Address Registers; they are loaded with RAM data 0-->7 at instruction "LOAD I/O ADD LO". Since the loading of the Lo Order Address Registers initiates the Output Control Operation, the Hi Order Address Register will always be loaded first to set up the entire 12 bit address required to access the core memory. The signal "I/O cycle" will cause the Output Control Address Register to increment after every output cycle in order to address the next character in core memory to be output.

(c) Output Control Data Registers (U24 and U28). - U24 and U28 are the Output Control Data Registers. They are loaded by the signal "I/O cycle" which occurs during an output cycle after the core memory is accessed. Once an output cycle is done the signal "I/O cycle done" goes high which makes "DATA RDY" go low. "DATA RDY" signals the interface circuitry that data has been accessed from core and is ready to be transferred to the interface circuits. The interface circuits will lower "READ DATA" which will enable the Output Control Data Registers onto the Data B-->15 lines. Once the interface circuits have taken the data, "READ DATA" will go high and release the Output Control Data Register

from the data bus, and at the same time initiate another cycle of the Output Control Logic at U2.

4-8. INPUT TO LINE BUFFER AND KEYBOARD LATCH. - This circuitry is used to input data from either the Keyboard or BID Latches into a circulating memory referred to as the Line Buffer. The Executive Macro will utilize a Multiplexer to control which data will be gated into the Line Buffer, In addition there is another memory which circulates in conjunction with the Line Buffer. This memory is known as the Flag Buffer, The Flags from the Character Identification Circuitry will always be loaded into the Flag Buffer when the BID is loaded into the Line Buffer.

a. Subcircuit Description (Figs, A-15, A-16). - The circuits on these schematics can be broken into five basic blocks. These are:

(1) Instruction Decoders

(2) Keyboard Latch

(3) Line Buffer Multiplexer

(4) Line Buffer

(5) Flag Buffer

The following paragraphs describe the circuits in the five basic blocks-

(1) Instruction Decoders (Fig. A-15). - The Instruction Decoders consist of I.C.s ID, 17M, and 18M. The instruction mnemonics and their use are as follows:

(a) Select Kybd - This instruction will allow the keyboard data to be gated through the Line Buffer Multiplexer.

(b) STBO - This instruction will load the data from the Line Buffer MUX into the Line Buffer and also the Flags into the Flag Buffer if the signal "RECIRCBFRS" is low. If "RECIRCBFRS" is high the data within the Line and Flag Buffers will be recirculated instead of the data loaded.

(c) RECIRCBFRS- The Executive Macro will raise this Flag when it wishes to recirculate the Flag and Line Buffers and will lower this Flag when it wishes these Buffers to be loaded.

(2) Keyboard Latch (Fig, A-15). - The Keyboard Latch consists of I.C.s 1B and 2B. The input to the Keyboard Latch is connected directly to the Keyboard via a cable. The data transmitted into the Keyboard Latch is the ASCII code for a particular key on the Keyboard. Besides the ASCII code, there is a strobe line "'Keyboard Kbstb", which is a signal that goes high when a key is depressed.

The signals used by the Executive Macro to control the Keyboard Latch come from Instruction Decoders on the Executive Macro schematic, The instruction mnemonics and their use are as follows:

(a) ENABLE KEYBOARD - This is a pulse instruction wRich allows the Keyboard Strobe to load the Keyboard Latch.

(b) RESET KYBD - This is a pulse instruction which will clear the outputs of the Keyboard Latch to all zeroes.

(c) KYBD - This signal goes to an Executive Macro Test Gate and will be tested by the Executive Macro to see if the Keyboard Latch was loaded.

(d) INCKYBD - This is a pulse instruction used by the Executive Macro to increment the binary number held in the Keyboard Latch.

Once the Executive Macro has enabled the Keyboard Latch via the instruction "ENABLE KEYBOARD," then two operations will occur when a key is depressed. First, the signal "KEYBOARD KYSTB" will go high, loading the ASCII character for that key into the Keyboard Latch. Second, when the key is released, 2C-9 will set and alert the Executive Macro that there is data in the Keyboard Latch. 2C-8 will reset thereby not allowing any more Keyboard Strobes to load the Keyboard Latch until the pulse instruction "ENABLE KYBD" is issued.

When the Executive Macro wishes to load the Line Buffer with special codes (such as "Start of Page," "Start of Line," "End of Line," "End of Page") it will utilize the Keyboard Latch in the following manner. First, the Executive Macro will clear the Latch via a "RESET KYBD' instruction and then increment the latch via "INCKYBD" instructions a number of times equal to the ASCII code desired.

(3) Line Buffer Multiplexers (Fig. A-15). - This circuitry consists of I.C.s 1A, 2A, 27A, and 28A and is used to gate information from three separate sources into the Line Buffer. These sources are chosen via the signals "SELECT KYBD" and "SPACE SELECT." When "SELECT KYBD(not)" is low, the data from the Keyboard Latch will be gated. When "SPACE SELECT(not)" is low, the ASCII code for a space character will be gated. When neither of these signals are active, then the BID ASCII character from the Character Identification Circuitry will be gated through.

(4) Line Buffer (Fig. A-16). - This circuitry appears on the interface board in slot J48 of the card cage. This Buffer has a capacity of 128 words, each 8 bits wids. The input to the Line Buffer comes from the Line Buffer MUX. The output of the Line Buffer goes to the Executive Macro Compare MUX. This Buffer is either loaded and shifted or just shifted via the instruction "STBO", depending upon the state of the "RECIRCBFRS" Flag.

(5) Flag Buffer (Fig. A-15).- This circuitry consists of I.C.s 17N and 17P. This Buffer is a 4 x 128 Shift Register consisting of two 1 x 128 Shift Registers, The Flags stored in this Buffer are "UNREC FLG," "Touching Character Flag" and the two Vertical Misalignment Flags, VMF1 and VMF2. The Flag Buffer rotates in coincidence with the Line Buffer/ so that the Flags correspond to the BID in the Line Buffer.

The outputs of the Flag Buffer are gated to the Executive Macro Test Gates.

4-9. MIL 188 INTERFACE (Fig. A-16). - The MIL 188 interface electronics extracts the character codes coming from the Memory Output Controller, in parallel form, and transmits this data serially with the proper start, stop, and parity bits, at a user specified baud rate. This logic is located on the Interface Board (P48) along with the Line Buffer in the card cage. The ALPHA uses this interface to communicate with the external device. When in this configuration, an external clock will be supplied to both the external device and the MIL 188 interface.

The signal "Receive Ready Output" coming from the TTY to the interface will be lowered when data is requested from the Alpha. The signal "DATA RDY" coming from the Memory Control Board will Load the data lines, (DATA 8 through DATA 15) into the transmitter on the MIL 188 interface. The signal "READ DATA" from MIL 188 to the memory controller will go low if the transmitter buffer is empty, and the character code will be enabled and Loaded into the transmitter. When "READ DATA" goes high "'DATA RDY" will go low again if another character is to be transmitted.

There are jumperable options on this interface which allow the user to select the number of bits per character (5, 6, 7, 8), one or two stop bits, odd or even parity and an internal or external baud clock. When selecting these

options, the user must be sure that the external device is set up for the same options.

4-10. ELECTRO-MECHANICAL - OVERVIEW. - The Electro-Mechanical portions of the ALPHA link the electronic circuitry to the mechanical motions of various assemblies in the machine. There are two different modes of operation. One causes a mechanical operation to take place as a result of an electronic instruction. The other mode causes an electronic signal to result from the occurrence of a mechanical motion.

a. General Operation. - The circuits which will be described in this section are all concerned with linking mechanical and electronic operations. In order to control mechanical operations with electronic signals, the low level signals used in the digital circuits must be converted into a form with sufficient voltage and/or amperage to drive the mechanical assembly. In order to generate an electronic signal as a result of a mechanical motion, some type of detection circuit must be established to generate this signal. The circuits described in the following paragraphs perform these functions.

b. Circuit Descriptions (Figs. A-23 and A-24). - There are various Electro-Mechanical circuits within the ALPHA.

These circuits consist of the Page Feeder Control and Detection Control Panel Switch Detection and LED Drivers; and the Format Panel Switch Detection.

(1) Page Feeder Control and Detection. - The Page Feeder Control and Detection circuitry is located in two places. Part of it is in the Page Feeder Assembly itself and another part is located on the Control Panel Assembly All the mechanical assemblies are located within the Page Feeder. This description will cover the various electro-mechanical operations one at a time.

The first operation necessary is to turn the Page Feeder Motor on or off. The Motor is driven by 115 WAC. In order to switch the 115 WAC on or off, a Relay with a 12V coil is placed in series with the motor. When the Relay is de-energized, the 115 WAC, which is tied to the common and normally open contacts of the Relay, is interrupted and the Motor is stopped. Energizing the Relay allows the 115 WAC to reach the Motor. The Relay is controlled by a 12 VDC signal across its coil, pins 1 and 4. Pin 4 is tied directly to 12 VDC. The other side of the Relay is controlled by the signal P.F. MOTOR (Relay)(not). When this is at ground, the Relay is energize& This signal is generated on the Control Panel by transistor Q3. The signal P.F. MOTOR ON(not) from the Instruction Decoder of the Vertical Servo circuitry is inverted by IC 6. When P.F. MOTOR ON (not) goes low, the base of Q3 is taken high, Q3 turns on, and its collector

takes the output P.F. MOTOR (Relay) (not) low thereby energizing the Relay and causing the Motor to run.

Another operation which must take place involves the use of a Brake and Clutch to allow the Paper Movement Belts to move. The Clutch Assembly links the Paper Movement belts to the Page Feeder Motor. When the Clutch is engaged, the Belts will move. When the Clutch is disengaged, the Brake is engaged and the Belts are held motionless. The Brake and Clutch control circuitry is arranged so as to assure that one is on and the other off. The Brake and Clutch are both electromagnetic coils which cause two plates to be pulled together. One plate is attached to the drive shaft and one to the driven shaft. When the plates are pulled together, the motion is transferred from one to the other. Both have one side of the coil tied to 12 VDC. The other sides are controlled by the signals BRAKE(not) and CLUTCH(not). When one of these goes low, the respective device will be engaged. These signals are also created on the Control Panel. The signal FEED from the Instruction Register of the Vertical Servo section drives the inputs of two inverters, IC 6-5 and IC 4-5. Observe that the signal is inverted only once before reaching Q1 while it is double inverted before reaching Q2. When FEED is Low, the base of Q1 will be high turning it on and the base of Q2 will be low turning it off. This will cause BRAKE(not) to be low turning the Brake on and CLUTCH(not) to be high turning the Clutch off. When

FEED goes high the conditions reverse, thus the Clutch is engaged and the Brake turned off.

The Page Feeder also has a Paper Gate which is lowered in front of the page. When the page' starts moving forward, it is momentarily driven against this gate resulting in the page being squared with the line along which the Read Head will scan. The Paper Gate will then be lifted and the page allowed to proceed. The Paper Gate is pushed down by a solenoid. When the solenoid is not energized, a return spring pulls the gate up out of the way. The solenoid is tied with one side attached to 12 VDC and the other side driven by the signal PGS DOWN(not). This signal also comes from the Control Panel. The signal PGS DOWN/UP(not) from the Instruction Decoder of the Vertical Servo circuitry provides the input to the Control Panel. When this signal goes high at IC 6-9, Q5 turns off and the pullup resistor on the base of Q4 turns Q4 on. PGS DOWN(not) therefore goes low and the Paper Gate solenoid pushes the gate down. When the input goes low, Q5 is turned OR, which grounds the base of Q4 and turns it off. The solenoid is de-energized and the return spring pulls the gate up.

Within the Page Feeder there is a Paper Sense Micro Switch which detects when the page is being driven against the lowered Paper Gate. It may happen that when the Page Feeder is requested to move another page into the machine, no more pages are in the Paper Tray. It may also happen

that it takes the Page Feeder different amounts of time to lift each page off the pile and move it against the gate. For this reason, the Micro Switch has been provided to detect when the page has actually reached the Gate. The switch is normally closed and opens when the page strikes it. On the Control Panel there is a pullup resistor tied to the output line of the switch. While the switch is closed, the signal line PAPER SENSE SWITCH is tied low through the switch. When the switch opens, the resistor pulls the line up to 5 VDC. This high or low signal passes directly through the Control Panel without modification and ties to the Executive Macro Test Gates where it may be detected. This indicates to the Executive Macro that the page has reached the Paper Gate and that the Gate should be lifted.

One last function is included in this area. The Page Feeder has built into it an Infrared LED and Photocell assembly which serves to detect when a double page is being forwarded by the Page Feeder. Obviously, if a double page were allowed to pass through, the lower page will be hidden by the upper page and will never be scanned. The Page Feeder mechanically tries to prevent this, but a double page may be processed on occasion. At the rear of the Page Feeder there is an Infrared Light Emitting Diode shining on a phototransistor. The pages leaving the Page Feeder must pass between these two.

The light from the LED can pass through these pages, however, less light will pass through two pages than through one. The more light striking the phototransistor, the harder it will conduct. The phototransistor is part of a voltage divider which also contains R22, R23, and R24. The transistor is tied to ground and R22 is tied to 5 VDC. As the transistor increases or decreases conduction, the voltage at TP2 will go lower or higher respectively. This feeds the inverting input of the Opamp IC8. The variable resistor R22 is adjusted such that the voltage at TP2 is approximately 2 VDC when a single page is between the LED and phototransistor and 4 VDC for a double page. The other input of the Opamp is tied to the midpoint of another voltage divider, thus it is biased to 2.5 VDC. The Opamp circuit has no feedback resistor, thus the circuit is a voltage comparator with only two possible outputs, high or low. When the single page causes the 2 VDC at TP2, the Opamp compares it with the bias level on its other input, the 2.5 VDC. Since 2 VDC is lower than 2.5 VDC, the Opamp output will go high. When a double page takes TP2 to 4 VDC, the comparator output will go low. The final output from this circuit is a signal called DOUBLE PAGE(not) which is high for a single page and low for a double page. This signal is sent to the Executive Macro Test Gates where it is monitored during the feed process. Should a double page condition be detected, the feed process will be halted

and a Double Page Detect Error Message (P2) will be displayed in the Control Console LEDs.

If the Double Page Detect Error Messages occur on occasion even though only a single page has been forwarded, or if a double page condition cannot be detected, the setting of the variable resistor, R22 on the Control Panel, should be checked. The voltage between TP1 and TP2 should be approximately 2 VDC for a single page and 4 VDC for a double page.

(2) Control Panel Switch Detection and LED Indicators. - The Control Panel has two switches mounted on it which are used by the operator to control machine operation. The LEDs display the operational status of the machine and indicate which of the mechanical operations is currently being performed,

The two switches are three position switches, They are momentary switches in the up or down positions. The switch returns to its normal center position whenever released. The two positions on one switch are RESET and STOP. When the switch is toggled to RESET, the output signal RESET(not) will be taken low through the switch. This signal i s sent to the Main Board Executive Macro circuitry where it unconditionally creates a system reset, If the switch had been toggled down to the STOP position, the input to IC 1-13

would have been taken low thereby causing IC 5-3 to go high. Since IC 5 is a positive edge triggered D-flop with the D-input tied high, the closing of the switch will cause the flop to set. The output from the circuit is the signal STOP which will then go high. This passes to the Executive Macro Test Gates. The Executive Macro tests for this condition when the machine is running and takes appropriate action when it is detected. Once the Executive Macro has detected that the STOP flop is set, it issues a signal RESET SW(not) to clear the flop thus acknowledging the toggling of the Stop Switch.

The Start and Continue flops work the same as the Stop flop. They are set as a result of the switch being toggled and are reset by the signal RESET SW(not) once the Executive Macro has recognized that the flop has been set. It is important to remember that these flops do not cause any direct action within the machine, but rather they depend upon the Executive Macro for recognition followed by its issuing commands to the appropriate circuitry.

The LEDs indicate which of the machine functions are in operation. Whenever the machine is in the RUN condition, the RUN LED will be lit. The input signal, RUN LAMP, comes from the Main Board Executive Macro circuitry. The FEED indicator will be lit whenever the page movement belts of the Page Feeder are moving in an attempt to forward a page into the machine for scanning. The FEED lamp signal comes from the Servo circuitry. The KEY lamp will light to

indicate that the keyboard is enabled and the-operator is expected to perform some action at the keyboard. This is the case at a Key Optics Stop or whenever the rotary switch on the Format Panel is moved to select one of the margin positions. In the first instance, the operator is expected to change or accept the unrecognized or questionable character. In the second case, the operator is allowed to alter the margin selected. The KEY LAMP signal comes from the Main Board Executive Macro circuitry.

The Control Panel also has an amplifier attached to it which drives the speaker which is mounted to the Control Panel. This speaker is used to emit the tones used for the various alarms. The signal alarm from the Servo circuitry is a square wave which has been generated at a constant frequency. This is amplified for current drive and sent to the speaker. The various tones are created by varying the frequency of the signal ALARM.

The remainder of the circuitry on the Control Panel is devoted to the drivers for signals being used by the Page Feeder as described in the previous section.

(3) Format Panel Switch Detection. - The Format Panel contains the switches which establish the parameters to be used while scanning the pages. One switch is a rotary switch while the others are two position toggle switches.

The outputs from the toggle switches go to the Executive Macro Test Gates where they may be checked by the program to

determine the scanning parameters. It may thus be determined, for example, whether the copy is single or double spaced and which alphabet to use.

The status of the rotary switch is determined differently. The wiper of the rotary switch, which is grounded, will connect to only one of the switch contacts depending on its position. Thus, one of the inputs to the Shift Register U1 will be low and all others high, When the Executive Macro wants to check the position of this switch, it first issues a LOAD SWITCH(not) signal. This loads all stages to a one except the one corresponding to the selected switch position, The Executive Macro then starts issuing the READ SWITCH(not) signal. For each one it issues,, the shift register shifts its data toward the output by one bit. After each shift, the signal ARO4(not) will be either high or low. As long as the data from the one stage containing the low has not yet reached the Shift Register output, AR04(not) will remain high. When the low bit has finally been shifted to the Shift Register output, ARO4(not) will go low causing the Executive Macro to execute a conditional jump The number of shifts required to get the low to the Shift Register output dictates where the Conditional Jump will lead the program-

4-11. LED DISPLAY LOGIC - OVERVIEW. - The LED Display is used during machine operation to display the first three characters of each scanned line; the value for the selected margin when the machine is in Standby Mode; and questionable

or unrecognized character during a Key Optics stop. The character preceding and following the one shown in the center LED will appear in LEDs 1 and 3 respectively.

a- General Operation - The LED Display Logic controls the processes required to cause characters to be displayed in the three LEDs of the Control Console. Information concerning when the LEDs display data and the meaning of the displays is explained in the operating section of this manual.

The LED circuitry is free-running in that it continually displays the last information sent to it, Three Input Latches may be loaded with the ASCII codes defining the characters to be displayed in the three LEDs. The logic then looks. up each of the three characters in the Character Generator and displays the characters one horizontal row at a time. After all the rows have been displayed, the process is repeated again and again, The characters thus appear to be continuously lighted,

b. Subcircuit Operation. - There are several subcircuits that may be described before the overall LED Display Logic circuitry is covered. The subcircuits are:

(1) Clock Generator

(2) Timing Generator

(3) Character Input Latches

(4) Character MUX

(5) Character Generator

(6) Display Latches

(7) Display Column Drivers

(8) Row Selector

(9) Row Driver

The following paragraphs describe the function of each of these subcircuits.

(1) Clock Generator. - The Clock Generator is a voltage controlled oscillator set to oscillate at approximately 42 KHz. This clock will be used by the Timing Generator portion to produce all necessary timing for the LED Displays.

(2) Timing Generator. - The Timing Generator creates a series of signals in the sequence required to operate the remainder of the LED Display Logic. The circuit consists of the Up Counter U25 and a series of decoder gates tied to its outputs- Several signals may be defined as occurring at specific states of U25. These are:

OUTPUT	D	C	B	A	RESULTANT
U25 Pin No.	7	6	2	3	OUTPUT
	0	0	0	0	SLC(not)
	0	0	0	1	SMC(not)
	0	0	1	0	SRC(not)
	0	0	1	1	NONE
	0	1	0	0	
	through				(Display)
	1	1	1	1	
	1	1	1	1	Inc Row

(3) Character Input Latches. - The Character Input Latches are three pairs of latches into which are loaded the ASCII codes for the three characters which are to be displayed. There is one pair of latches assigned to each display position. The LED display data is stored in the pair U29 and U42, the middle data in U30 and U43, and the right data in U31 and U44.

The Batches may be parallel loaded from the Accumulator of the Executive Macro The ASCII code would be set on the paralleI input lines to the latches and the load executed by the signal SET CH DISP(not) 1, 2, or 3 for left, middle, or right respectively. The ASCII value in each latch may be incremented by one through the issuance of the signals INC CH DISP(not) 1, 2, or 3. All the latches may also be cleared at the same time by the signal RESET CHAR DISP(not).

(4) Character MUX,, - The Character MUX selects the data from one of the Character latches and feeds it to the Character Generator inputs, The SLC (not), SMC(not), and SRC(not) outputs from the Timing Generator section are converted into the signals "A" and "B" by two NAND sections of U22. These two lines become the addressing information to the multiplexer packages U40, U41, U32, and U33, The schematic shows which combination causes which data to be passed through the multiplexer.

(5) Character Generator. - The Character Generator (U3) is partially addressed by the outputs from the Character Multiplexers. The CB1-CB6 outputs from the Multiplexer are

tied to the A4-A9 address lines of the Character Generator. The CB7 line is tied to a Multiplexer on the output side of the Character Generator. Three additional lines, A1-A3, are generated by the Row Selector, U19. The combination of addresses selects a five bit data word stored in the Character Generator. This five bit word is one row (defined by A1-A3) of one character (defined by A4-A9 plus CB7).

The LEDs are capable of displaying characters five dots wide by seven dots high. The five horizontal dots compose the rows of the characters. The seven vertical dots compose the columns of the characters. Thus one character contains seven horizontal rows of five dots. The characters are displayed by sequentially displaying the rows of each character starting from the bottom. First, the bottom row is caused to light and go out. Then the second lights and goes out. When the top has been displayed, the process is repeated from bottom to top, etc. It is this process which requires that only one row be output from the Character Generator. The full process will be explained in greater detail in the circuit operation section.

(6) Display Latches. - The Display Latches store the information as to which dots are to light in the row currently being selected. There is one five bit latch for each of the three LEDs. Each of these latches will be loaded prior to the time when the current row will be lighted.

(7) Display Column Drivers. - The Display Drivers cause the individual dots to turn on or remain off depending on the information contained in the Display Latches. They contain transistor drivers which provide adequate current drive for the individual LED dots.

(8) Row Selector. - The Row Selector is incremented after each row has been displayed. The next row is then selected and the Timing Generator will cause that next row to be displayed. The Counter will count from zero to seven, which is actually eight rows. During the time the eighth POw is selected, none of the dots will be lighted. The Counter will then overflow back to zero and select the bottom row.

(9) Row Driver. - The Row Drivers cause ail the dots of one row to be enabled. Which of the dots actually light depends on the data stored in the Display Latches.

C. Circuit Operation. - The LED Display Logic provides the link between the Executive Macro and the three LEDs on the Control Console. The Executive Macro is able to load data into a set of latches in the LED Display Logic which then takes over and repeatedly displays that data in a fashion which makes the display appear constant.

Since the LED Display Logic is a free- planning circuit operating in a repetitive Loop, this discussion must jump into that loop at some selected point disregarding what has previously occurred. We shall define this starting

point as being the occasion when the Executive Macro sends new data to the LED Logic.

The Executive Macro can cause any combination of displayable characters to be placed in the LEDs. Let's pick an example which can be used for the remainder of this description. Assume that the three LEDs are to display (H=I). The Executive Macro will cause the ASCII codes for these three characters to be Loaded into the three pairs of Character Input Latches. The latches for the Left LED will, therefore, contain an ASCII 110, the center latch an ASCII 75, and the right latch an ASCII 111. This might have been loaded two ways. first, the Executive Macro can load the appropriate code into the Accumulator, then issue a SET CHAR DISP(not) to the latch which is to receive that code. The other possibility is that the Executive Macro will issue RESET CHAR DISP(not) clearing all three latches. It will then issue INC CH DISP(not) to each of the latches until they are incremented to the desired ASCII value. The remainder of the circuitry is involved with displaying the characters defined by the ASCII codes in the latches.

Let's define some further conditions. First, assume that the Timing Generator Counter (U25) has just overflowed to the all zeroes condition. Also, the Row Selector (U19) is at the all zeroes state. The signal SLC(not) at U35-3 is low as a result and the address inputs CA and B) to the Character MUX is set to a 1-0 condition respectively. This

allows the ASCII code from the Left Character Input Latch to pass to the Character Generator inputs A4-A9. The Row Selector is also holding the A1-A3 inputs at all zeroes, This causes the Character Generator to output the bottom row data for the left character which we have defined to be the "H". If the LED Patterns Illustration is checked, it may be noted that the bottom row of an "H" has only two of the five dots lighted. This fact is stored in the Left Display Latch when the Timing Generator advances to its next state and the CK input on U37 returns high.

The new state of the Timing Generator creates SMC(not) which changes the Character MUX such that it passes the ASCII code from the Middle Character Input Latch. The Row Selector is still set at zero. The Character Generator consequently outputs the bottom row data for the center character which has been here stated to be an Equal Sign. The LED Patterns Illustration shows that the bottom row for an Equal Sign has none of the dots lighted. This information will be stored into the Middle Display Latch by the trailing edge of SMC(not) which occurs when the Timing Generator Counter advances to the next state taking U28 high.

This third state selects the third latch through the multiplexer thus sending the three center dots of the bottom row to the Right Display Latch. When the Timing Generator advances, this data is stored in the latch. The fourth state is a no operation state.

The remaining states of the Timing Generator Counter will turn on the Bottom Row Driver thereby causing the dots designated by the Display Latches to be lighted in the bottom row. Using our stated example, the Left LED will have two dots lighted, one in each lower corner, no others. The Center LED will have no dots Lighted, and the Right LED will have the middle three dots of the bottom row lighted. This result is achieved by having only the Bottom Row Driver energized thereby tying one side of all the individual diodes in the bottom row to +5 VDC. The data in the Display Latches then causes the Column Drivers to energize those columns which should be lighted and not energize those which should be out. This is done through the transistor drivers which take the column lines to ground if a dot in that column is to be lighted. Since only the bottom row has +5 VDC on one side of the diodes, when the other side of the diodes in a column is grounded, only the dot in the bottom row will light.

When the Timing Generator Counter overflows, the Row Selector will be incremented to the next higher row. The entire process is repeated for the dots of the second row of the characters stored in the Character Input Latches. Then the next row is selected, etc. This process is continuous with the result being that the eye sees what appears to be a constantly displayed set of characters.

4-12. POWER SUPPLY SUMMARY. -

a. Base Frame (Fig. A-26). - Primary power enters the base frame through terminal strip J201, POWER switch S202, and main power fuse F9. This AC input is then applied to terminals 1A and 3A on the primary of power transformer T1. One side of three of the four secondary windings is connected through magnetic switches in relay K1. This relay is set to de-energize when fan B1 fails to operate or air flow is blocked activating thermal switch S201. When K1 is de-energized it will open the supply circuit from secondary winding terminals 5 and 6, 16 and 17, and 9 and 11. Secondary winding 14 and 15 is protected by fuse F5 which is mounted on the fuse block. In addition, each of the other secondary windings is fused in case of supply malfunctions.

b. + Supply (Fig. A-26). - The + supply is obtained from secondary winding 5 and 6 of transformer T1. This step-down AC voltage is applied to full wawe rectifier network CR1. The DC output of CR1 is then applied to filter network Cl, C2. Resistor RI is a bleeder resistor which allows C1 and C2 to discharge when power is turned off.

(1) +5 Volt Power Supply (Fig. A-28). - The +5 voltage regulator is a switching regulator capable of handling a 27 amp load. When power is first applied the 723 voltage regulator U1, pin 11, and the base of transistor Q1 will be how causing Q1 to turn on. When Q1 turns on, the voltage at the base of Q7 becomes lower than collector

enabling Q7 to turn on. When on, Q7 will lower the voltage at the base of the pass transistors, Q3, Q4, Q5, and Q6, turning them on. This brings the output up to 5 volts and charges coils Cl and L2. The voltage at U1, pin 5, increases through resistor R9 until it reaches a level set by the voltage divider composed of resistors R5, R6, R7, and R8. When this level is reached U1 will turn off allowing the base of Q1 to be pulled up to the + supply voltage level by pullup resistor R2 turning Q1 off. This allows the base of Q7 to be pulled high by R20 turning it and the pass transistors Q3, Q4, Q5, and Q6 off. Coils L1 and L2 now discharge, supplying power load. When the output voltage sensed at pins 3, 4, and 10 drops 300 millivolts U1 will turn on. The time it takes L1 and L2 to discharge depends upon the sire of the load. The larger the load the faster C1 and L2 discharge and the higher the switching frequency. With no load the regulator switches at 2.5 KHz while with full load the regulator switches at 20 KHz, The +5 voltage can be varied from 4 to 7 volts using potentiometer R6. The +5 volts is to be set so that +5 volts ±0.05 volts is measured at the core, the red wire is the +5.

(2) +5 Volt OCG Circuit. - The resistor network, composed of R21, R22, and R23, is in series with the load, the voltage drop across the network is proportional to the current drawn by the load. When this voltage drop becomes

greater than 0.6 volts for more than 50 microseconds, Q2 will turn on. Q2 will bring the gate of OP2 high. When the gate of OP2 goes high it latches on, bringing pin 2 up to the + supply level while pin 3 is at +5 volts. Pin 2 and pin 3 are inputs to an internal comparator, when pin 2 is more than .6 volts greater than pin 3 the U1 turns off. To reset CR2 the Alpha must be powered down. Upon power up, if there are no shorts across the +5 volt power supply, CR2 will be off and the +5 volts supply will then return.

(3) +12 Volt Power Supply (Fig. A-29). - The +12 voltage regulator is a switching regulator capable of handling a 3 amp load. When power is first applied the 723 voltage regulator U1, pin 11 and the base of transistor Q2 will be held low causing Q2 to turn on. When Q2 turns on the voltage at the base of Q1 drops lower than the collector enabling Q1 to turn on, bringing the output up to 12 volts and charging coil L1. The voltage at pin 5 increases, after a delay determined by R13 and C13, until it reaches a level set by the voltage divider R12 and R13. When the voltage at pin 5 is greater than the voltage level at pin 4, U1 will turn off allowing the base of Q2 to be pulled up to the + supply level by R2 turning it off. RI pulls the base of Q1 high turning it off,, Coil L1 discharges, supplying power to the load. When the output voltage, sensed by pin 4 by way of the voltage divider composed of resistors R14, R15, and R16, drops 300 millivolts U1 will turn on. The time it

takes L1 to discharge depends upon the size of the load. The larger the load the faster L1 discharges and the higher the switching frequency, With no load the regulator switches at 5 KHz while with full load the regulator switches at 20 KHz. The +12 volt supply can be varied from 10 to 15 volts by R15. The +12 volts is set to +12 ±0.1 volts on the main wire wrap board.

(4) +12 Volt OCG Circuit. - Resistor R3 is in series with the load and the voltage drop across this resistor is proportional to the current drawn by the load. When this voltage drop becomes greater than 0.6 volts for more than 50 microseconds, Q3 will turn on. Transistor Q3 will bring the gate of CR3, by way of the current limiting resistor R7, high. When the gate of CR3 goes high it latches on, bringing pin 2 up to the + supply level while pin 3 is at +12 volts. Pin 2 and pin 3 are inputs to an internal comparator U1. When pin 2 is more than 0.6 volts greater than pin 3 U1 turns off. To reset CR2 the Alpha must be powered down. Upon power up, if there are no shorts across the +12, CR3 will be off allowing the +12 to return.

(5) Read Head Lamp Supply (Fig. A-29). - The Read Head voltage regulator is a switching regulator capable of handling a 2 amp load. When power is first applied the 723 voltage regulator U2, pin 11, and the base of transistor Q5 will be low enabling Q5 to turn on. When Q5 turns on the voltage at the base of Q4 drops lower than the collector.

This enables Q4 to turn on bringing the output up to 17 volts and charging coil L2. The voltage at pin 5 increases, after a delay determined by R29 and C24, until it reaches a level set by voltage divider R28 and R29. When the voltage at pin 5 is greater than the voltage level at pin 4, U2 will turn off allowing the base of Q5 to be pulled up to the + supply level by R21, turning it off. Resistor R17 can now pull the base of Q4 up to the + supply level, turning it off. Coil L2 now discharges supplying power to the load. When the output voltage, sensed by pin 4 by way of the voltage divider R30, R31, and R32, drops 300 millivolts U2 will turn on. The time it takes L2 to discharge depends upon the size of the load. The larger the load the faster L2 discharges and the higher the switching frequency. With no Load the regulator switches at 5 KHz while with full Load the regulator switches at 20 KHz. The Read Head can be varied from 11 to 21 volts by potentiometer R30. The Read Head is set to +17 ±1 volt on the power supply test panel.

(6) Read Head OCG Circuit. - Resistor R18 is in series with the load and the voltage drop across the resistor is proportional to the current drawn by the load. When this voltage drop becomes greater than 0.6 Volts for more than 50 microseconds Q6 will turn on. Transistor Q6 will bring the gate of CR7, by way of the current limiting resistor R24, high. When the gate of CR7 goes high it latches on,

bringing pin 2 up to the + supply level while pin 3 is at +17 volts. Pin 2 and pin 3 are inputs to an internal comparator when pin 2 is more than 0.6 volts greater than pin 3 the U1 turns off. To reset CR7 the Alpha must be powered down. Upon power up, if there are no shorts across the Read Head supply, CR7 will be off allowing the Read Head supply to return.

The Read Head supply can be turned on or off by the logic circuits, thereby allowing the Read Head lamp to be an only when scanning. 'Control from the logic circuits comes in at J12 to the base of Q7. When a low logic level is received at the base of Q7, Q7 will turn off. This makes pin 2 of U2 more than 0.6 volts higher than pin 3. With pin 2 higher than pin 3, U2 will turn off. When a logic high is received at the base of Q7, Q7 will turn on. The anode of CR9 is now pulled down to ground potential by Q7 and the Read Head supply now can operate as described above.

c. - Supply (Fig. A-26). - The - supply is connected to the power transformer's secondary at pin 16 and at pin 17, by way of K1. The AC voltage from T1 is fully rectified by CR2, then capacitor C3 is used to allow C3 to discharge when the power is turned off. Fuse F2 is used to protect the - SUPPLY. The RC network R6 and CR5 will be described later under OVG. The voltage across - supply and - RET will be 33 ±2 volts.

(1) -9 Volt power Supply (Fig. A-30). - Upon power up U1 is off, and this allows resistor R3 to pull the base of transistor Q1 down to the - supply level turning Q1 on. Transistor Q1 forces the base of Q3 to go higher than the emitter of Q3, turning on Q3. Transistor Q3 brings the base of the pass transistor, Q2, up to the ground potential. Transistor Q2 turns on, supplying -9 volts to the load and charges L1. After a time delay of 50 microseconds, generated by the RC network composed of R11 and C9, pin 5 will be pulled down to -9 volts. When the voltage level at pin 5 goes lower than the limit set by the voltage divider network, composed of R8, R9, R10, and R12, U1 will turn on. Pin 9 now is pulled up to -6.2 volts, turning Q1 off. The base of Q3 is pulled down to -27 volts forcing Q3 to turn off. The base of Q2 now is pulled down to the - supply level by RI. Transistor Q2 turns off, Cl discharges supplying power to the load. When the voltage at pin 7, connected to the -9 output voltage through CR7 and CR8, drops 300 miiiivolts, U1 will turn off. The time it takes C1 to discharge depends upon the size of the load. The Larger the load the faster L1 discharges and the higher the switching frequency. With no load the regulator switches at 5 KHz while with full load the regulator switches at 20 KHz. The -9 can be varied from -7 to -11 volts by R9. The -9 is set to -9 ±0.1 volts on the main wire wrap board.

(2) -9 OCG Circuit (Fig. A-30). - The resistor R32 is in series with the load and the voltage drop across this resistor is proportional to the current drawn by the load. When this voltage drop becomes greater than 0.6 volts for more than 50 microseconds, Q4 will turn on. Transistor Q4 will then pull the base of Q5 down to -9 volts, turning Q5 on. When Q5 turns on it will bring the gate of CR1 up to ground. When the gate of CR1 is at the same voltage potential as the anode of CR1 it latches on bringing pin 9 up to ground potential. A ground level at the base of Q1 will turn off the -9 volt supply. To reset CR1 the Alpha must be powered down. Then upon power up, if there are no shorts across the -9 supply, CR1 will be off allowing the -9 volt supply to return.

(3) -12 Volt Supply (Fig, A-30). - Upon power up U2 is off allowing R19 to pull the base of transistor Q6 down to the - supply level turning Q6 on. Transistor Q6 forces the base of Q8 to go higher than the emitter of Q8, turning on Q8. Transistor Q8 brings the base of the pass transistor Q7 up to the ground potential. Transistor Q7 turns on supplying -12 volts to the load and charges L2. After a time delay of 50 microseconds, generated by the RC network composed of R30 and C24, pin 5 will be pulled down to -12 volts. When the voltage level at pin 5 goes lower than the limit set by the voltage divider network, composed of R27, R28, R29, and R31, U2 will turn on. Pin 9 is pulled UP

to -6.2 volts, turning Q6 off. The base of Q8 is pulled down to -27 volts forcing Q8 to turn off. The base of Q7 is pulled down to the - supply level by R16. Q7 turns off, L2 discharges supplying power to the load, When the voltage at pin 7, connected to the -12 output voltage, drops 300 millivolts, U2 will turn off. The time it takes L2 to discharge depends upon the size of the load. The larger the load the faster L2 discharges and the higher the switching frequency. With no load the regulator switches at 5 KHz while both full load the regulator switches at 20 KHz. The -12 volt supply can be varied from -10 to -15 volts by potentiometer R28. The -12 is set to -12 volts ±0.1 volt on the main wire wrap board.

(4) -12 Volt OCG Circuit (Fig. A-30). - The resistor R22 is in series with the load and the voltage drop across this resistor is proportional to the current drawn by the load. When this voltage drop becomes greater than 0.6 volts for more than 50 microseconds transistor Q9 will turn on. Transistor Q9 will then pull the base of Q10 down to -12 volts, turning Q10 on. When Q10 turns on it will bring the gate of CR4 up to ground. When the gate of CB4 is at the same voltage potential as the anode of CR4 it Iatches on, bringing pin 9 up to ground potential. A ground level at the base of Q6 will turn off the -12 volt supply. To reset CR4 the Alpha must be powered down. Upon power up,

if there are no shorts across the -12 volt supply, CR4 will be off allowing the -12 volt supply to return.

d. Servo Supply (Fig. A-26). - AC voltage from pin 9 and pin 11 on the secondary windings of T1 is fully rectified by CR3. Pin 10 on T1 is used as a common return point giving a positive and negative voltage. Capacitor C4 is used to filter out any AC component of the positive servo supply, R3 is a bleeder resistor to allow C4 to discharge when the power is down. The positive Servo supply is protected by F3. Capacitor C5 is used to filter out any AC component of the negative Servo supply, R4 is a bleeder resistor to allow C5 to discharge when the power is down. The negative Servo, supply is protected by F4,

e- Power Supply Test Panel (Fig. A-27). - Power Supply Test Panel located in the rear of the Alpha has 7 LEDs, one for each of the voltage supplies. The LEDs are basically go, no-go testers, they only show that a given voltage is on or off. The other circuitry on the board is for the Data Save and the OVG, both of which are described in detail below.

(1) OVG + Supply (Fig. A-27). - The +5 volt supply is monitored by zener CR14 and diode CR15. When the breakdown voltage of 6.2 volts for CR14 and 0.6 volts for CR15 is reached the voltage at R24 can be raised. The +12 is monitored by zener CR16 and diode CR17. When the breakdown voltage of 16 volts for CR16 and .6 volts for CR17 is reached the voltage at R24 can be raised. R24 and R25 comprise the

voltage divider, a 1 volt drop across the voltage divider will generate 0.91 volts at OVG. OVG is connected to the gate of CR4 in the + supply. When the gate of CR4 is higher than 0.8 volts, CR4 latches on crowbarring the + supply and causing fuse F6 to blow. The Alpha must be powered down to reset CR4. The OVG for the +5 volt supply is set at 7.8 volts and the +12 is 17.6 volts.

(2) - Supply OVG (Fig. A-27). - The -9 volts is monitored by zener CR12 and diode CR13. When the breakdown voltage of 16 volts for CR12 and 0.6 volts for CR13 is reached the voltage at R20 can be raised, The -12 is monitored by zener CR10 and diode CR11. When the breakdown voltage of 16 volts for CR10 and 0.6 volts for CR11 is reached the voltage at R20 can be lowered. R20 and R21 comprise the voltage divider, a -4.4 volt drop across the voltage divider will generate -0.65 volts at the base of Q3. Q3 will turn on, pulling the -OVG up to the ground potential. -OYG is connected to the gate of CR5 in the - supply, when the gate of CR5 is at the same voltage as the anode, CR5 Latches on crowbarring the - supply and causing F2 to blow. The Alpha must be powered down to reset CR5. The OVG for the -9 volt supply is set at -21 volts and the -12 is -21 volts.

(3) Data Save (Fig. A-26). - The Data Save circuitry is used to protect data in the event of a power failure or when the Alpha is turned off. The 8 volts AC from pins 14 and 15 on the secondary of transformer T1 is fully rectified

by full wave rectifier network CR8. Capacitor C8 is used to filter out the AC components. This power supply is used for relay K1. The output from the +5 power supply is connected to the voltage divider composed of R19 and R26. Approximately 82 percent of the +5 volts appears at the base of Q2 turning it on. Transistors Q2 and Q1 are wired in a darlington configuration, turning on Q2 will turn on Q1 Transistor Q1 will ground pin 4 of K1 energizing it. This will open the contact and allow Data Save to go high. When the +5 drops to 4.85 the base of Q2 drops to 4 volts, turning Q2 and Q1 off, Relay K1 de-energizes, closing the contacts and grounding Data Save. When Data Save goes low the CPU sends all the data to the core to be saved until the power comes up.

4-13. OPERATING PROGRAM SEQUENCE OF EVENTS (Fig. 4-46). -

a. Order of Events After "Reset". -

(1) The following will be turned off:

(a) Run Light

(b) Read Head Lamp

(c) output

(d) Horizontal and Vertical Servos

(2) LEDs will read "NULL NULL NULL" if Mode Selector Switch is not in a margin position. If Mode Selector is in a margin position, that margin will be displayed in tenths of an inch.

b. Order of Events After "Start" (Mode Selector Switch

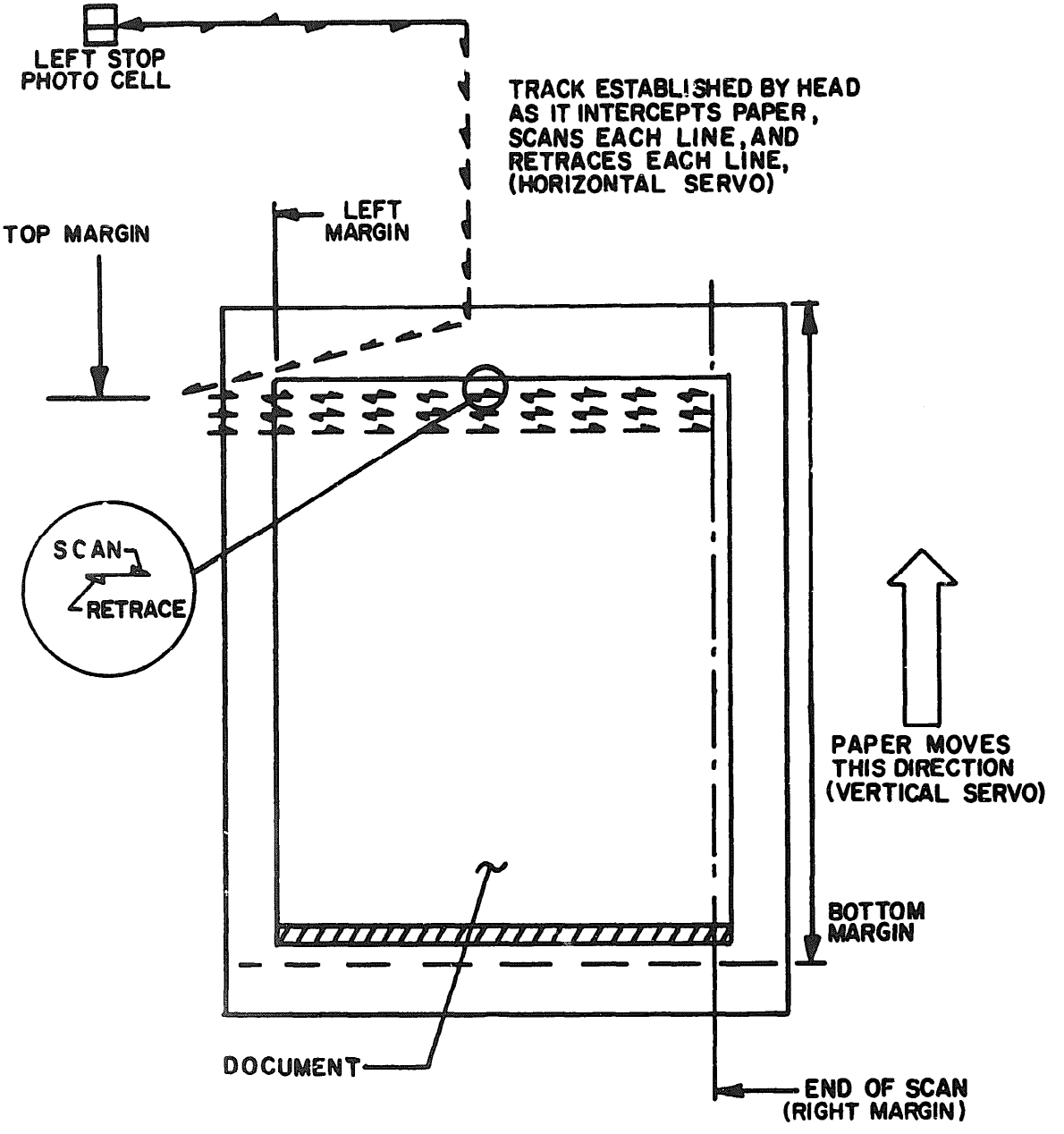


Figure 4-46. - Horizontal and Vertical Servos Movement

in Operate), -

(1) Run Lamp, Read Head, Stackfeeder all turn on. However rubber belts do not turn until they are clutched,

(2) Read Head drives Left in velocity mode.

(3) Program detects L stop (left photo cell), this clears the Horizontal Position Counter, then loads the Margin Counter with a value 7" (1/2 the carriage length).

(4) Read Head drives right in velocity mode.

(5) Program is checking for horizontal margin (LT/RT Margin). This is the first time the horizontal encoder pulses are used.

(6) Program detects horizontal margin (7") and"

(a) Enters horizontal position mode-

(b) Issues "FEED" signal. Rollers roll, stack-feeder feeds.

(7) Paper Gate Solenoid routine:

(a) Gate comes down.

(b) Paper comes through, trips a micro switch, and aligns up with gate.

(c) 1/4 second after the micro switch was tripped the gate rises and allows paper through-

(8) Read Head detects paper present.

(9) The Vertical Position Counter which was previously held clear by no paper present is now allowed to count and the Vertical Position Mode Logic will position paper to top margin.

At this same time as the paper moves forward, the Read Head drives left until it is off the paper.

(10) Read Head drives right when:

(a) "Paper in position" i.e. rollers stopped and

(b) Read Head is off paper; this zeroes the Horizontal Position Counter and loads the left margin into the Horizontal Margin Counter.

(11) Read Head is driving right and the Horizontal Position Counter is now counting from left edge of paper.

(12) Program detects left margin and starts accepting encoder samples and starts acquiring video, Also, the Horizontal Margin Counter is loaded with the value of the right margin, and the program is checking for "LT/RT margin."

(13) The Video Processing Circuitry will use the flags "FB1", "FB2". "TSZF", and "BSZF" to center the Read Head over the line to be scanned. This will be accomplished by the Read Head driving left again and the paper moving forward if necessary to center the Read Head when it drives right again,

(14) The Video Processing Circuitry will use the flags "FB1", "FB2", "FC", "POPF" to start and end the storing of video,

(15) The "unknown" character stored is processed through the Character Identification Circuitry and its ASCII code is loaded into the Line Buffer (Buffer 0). Each succeeding character on the line will go through steps 14 and 15.

(16) The program detects that the Read Head has reached the right margin and the Read Head drives left in Velocity Mode looking for the left margin.

(17) While the Read Head is driving left, the program extracts the "unknown" character's ASCII code from the Line Buffer and converts these codes into output codes specified by header sheets.

(18) These output codes are stored in the Output Buffer Section of core memory and the output "Macro" is started. This "Macro" will sequentially take data from core and load it into the Output Interface Circuitry (J48) to be transmitted to an external device.

(19) When the left margin is reached, the vertical Servo pushes the paper forward and the Read Head will drive right after it has

(a) Gone off the edge of the paper, and

(b) The paper is in position.

Each line will be scanned in the same manner until the Vertical Position Counter reaches bottom margin. At this time the page is ejected, and the program jumps to step 2.

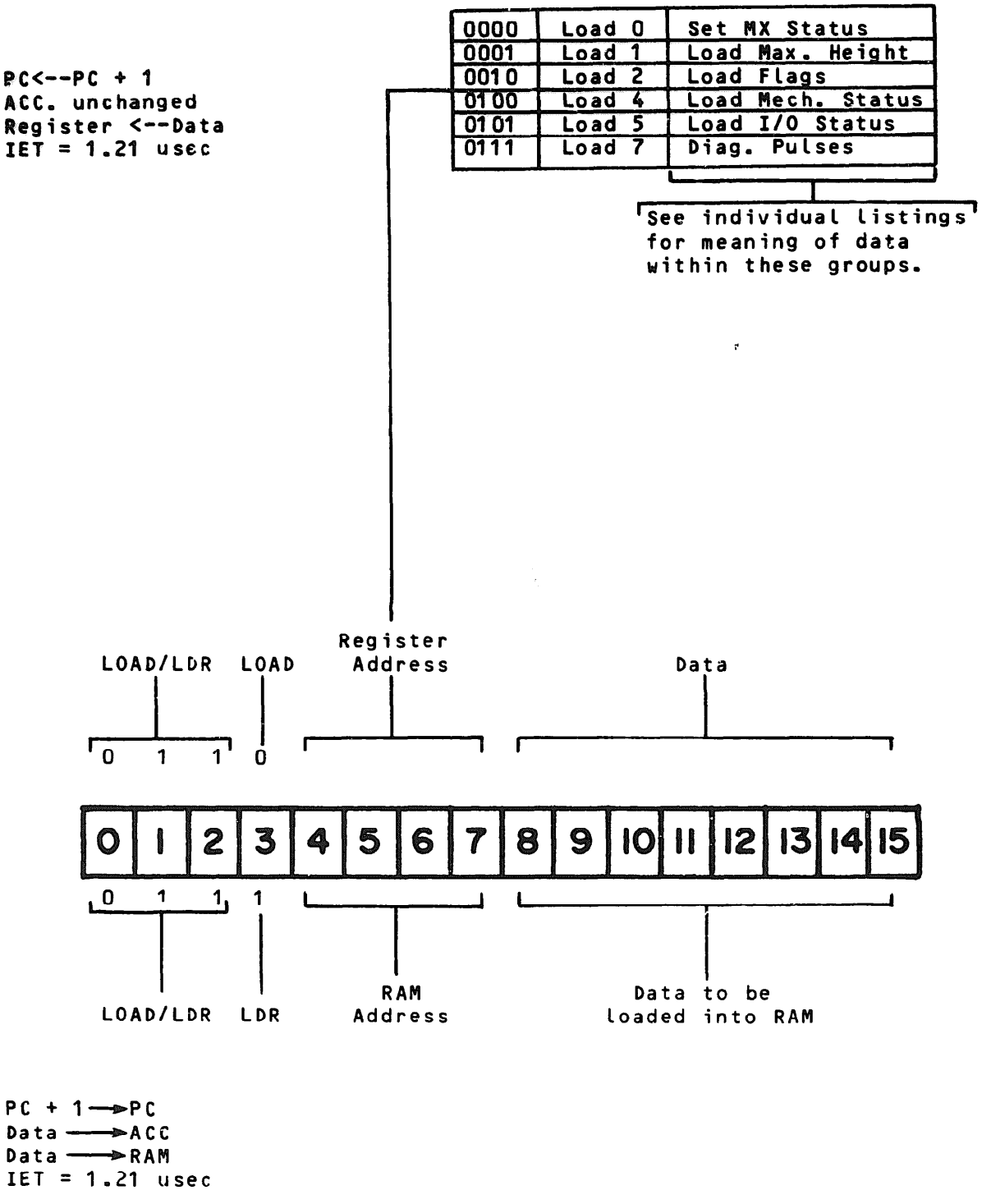


Figure 4-16. - Instruction Word Format - LOAD/LDR

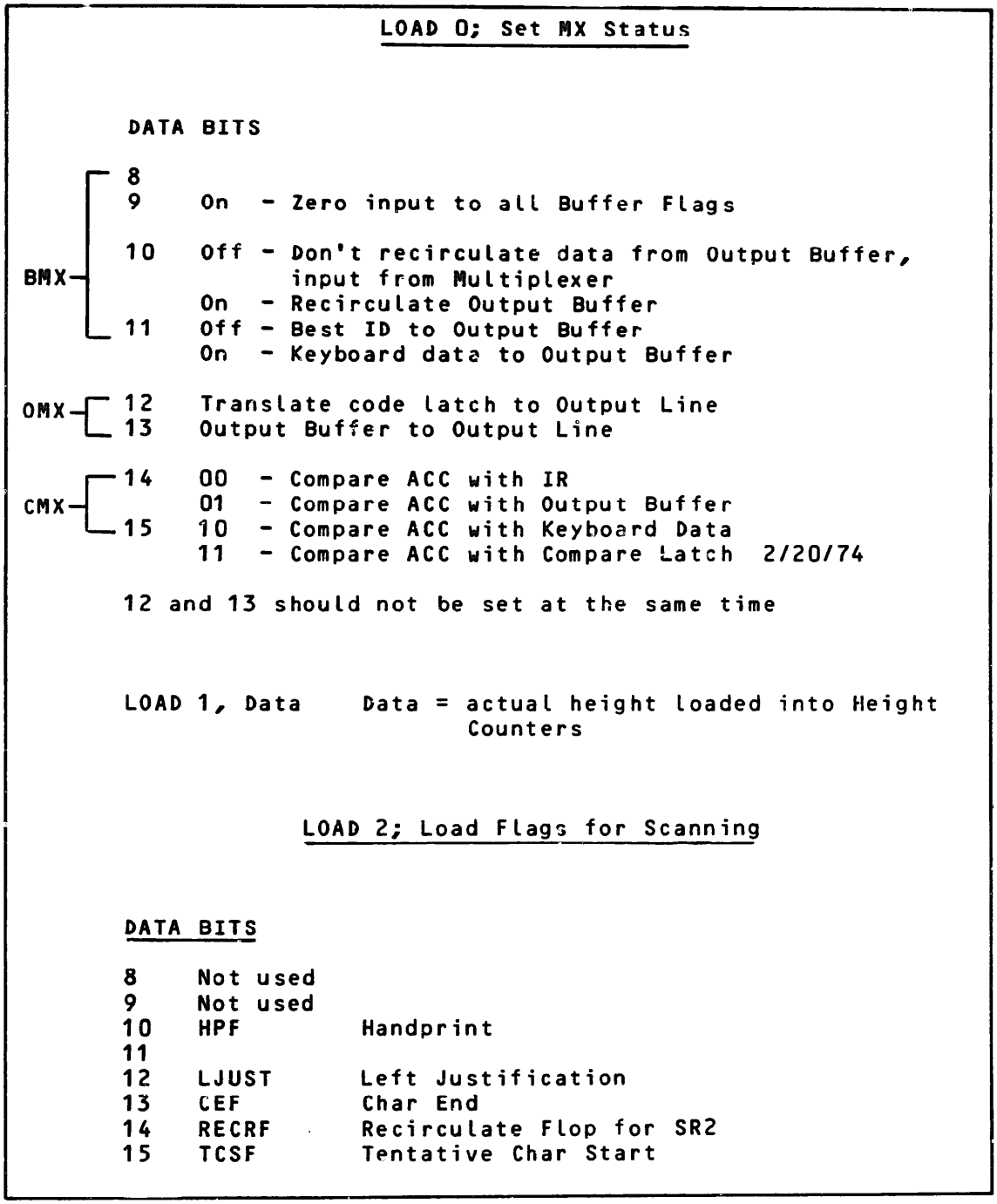


Figure 4-17. - Load Instructions 0, 1, 2

8	9	10	11	12	13	14	15
1	1	0 LOAD RIGHT SPEED	1	24 IN/SEC	12 IN/SEC	6 IN/SEC	3 IN/SEC
LOAD SPEEDS		1 LOAD LEFT SPEED	0				
		1 LOAD VERTICAL SPEED	1				
0	1				1/0 HOR. POS. COUNTER CLEAR INH/ $\overline{\text{ENABLE}}$	0 HORIZONTAL STOP	0
LOAD HORIZONTAL MECHANICAL MODES						0 HOR. POSITION MODE	1
						1 DRIVE RIGHT	0
						1 DRIVE LEFT	1
1	0		1/0 PAPER GATE SOLENOID ON/$\overline{\text{OFF}}$	1/0 FEED ON/$\overline{\text{OFF}}$	1/0 VERT. POS. COUNTER CLEAR INH/ $\overline{\text{ENABLE}}$	0 VERTICAL STOP	0
LOAD VERTICAL MECHANICAL MODES						0 VERT. POSITION MODE	1
						1 DRIVE UP	1
0	0		1/0 PAPER GATE SOLENOID ON/ $\overline{\text{OFF}}$	1/0 FEED ON/$\overline{\text{OFF}}$	1/0 HOR & VERT POS COUNTER CLEAR INH/ $\overline{\text{ENABLE}}$	0 VERT & HOR STOP	0
LOAD HOR & VERT. MECHANICAL MODES						0 VERT & HOR POS MODE	1
						1 DRIVE RIGHT	0
						1 DRIVE UP & LEFT	1

Figure 4-18. - Load Instruction 4

LOAD 5; IO Status

DATA BITS

8
9
10
11
12 - Turn on Punch
13 - On-Line Interface ON
14 - Special I/O Pulse ON
15

LOAD 7; Diagnostic Load

DATA BITS

8 - Ex Macro H. sample - requires 4 loads. Bit 9 or 10 should also be on
9 - 1 = sample all 1's
10 - 1 = sample all 0's
11 - Ex Macro V. sample
12 - 1 = Inc. or clear CPM Ctr.
13 - 1 = Start Recog
14 - 1 = Inc. or clear Ref. Alph. Ctr.
15 - 0 = Clear
1 = Inc. - use with bit 14 or 12

Figure 4-19. - Load Instruction 5, 7

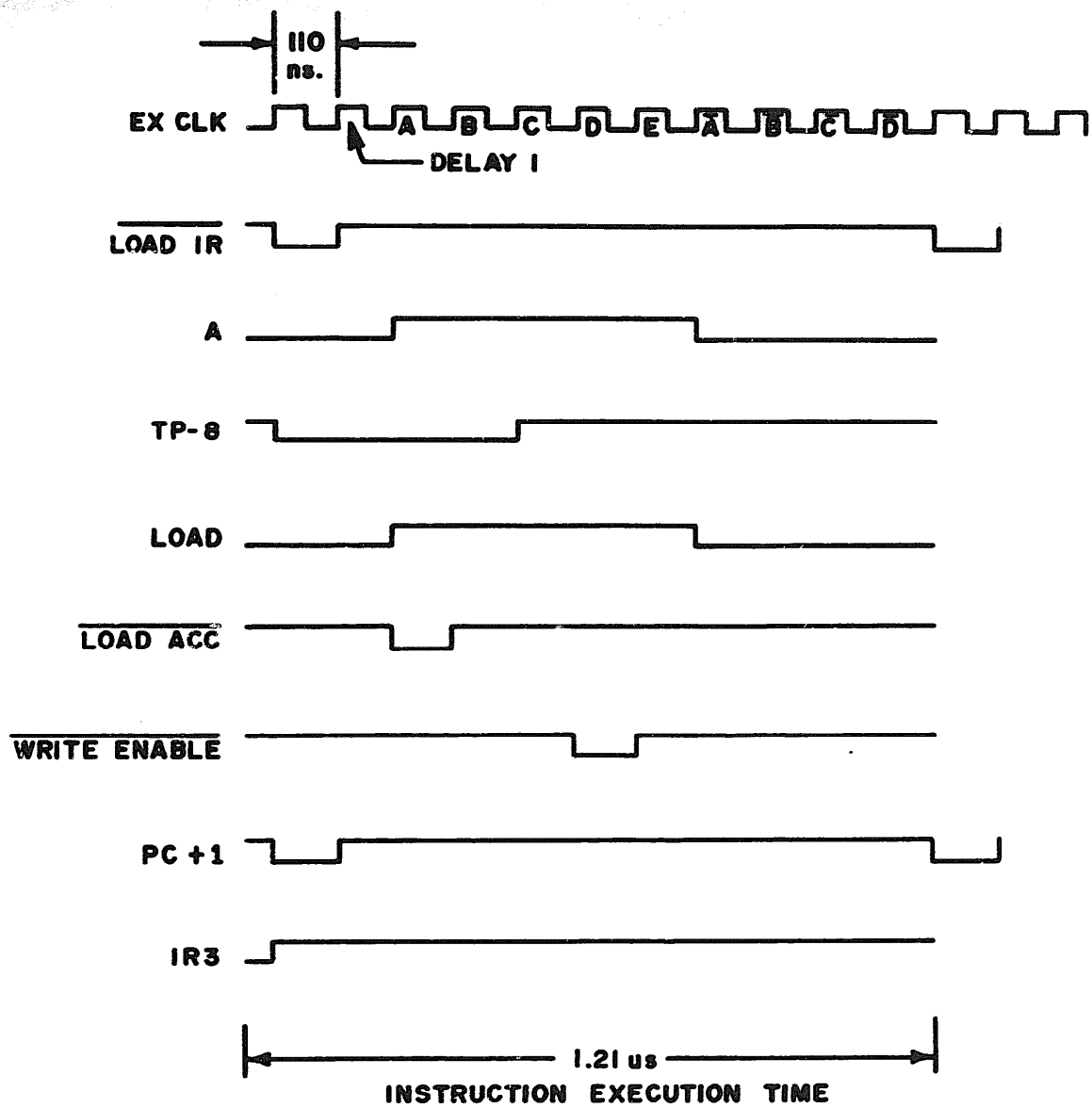


Figure 4-20. - LDR Instruction

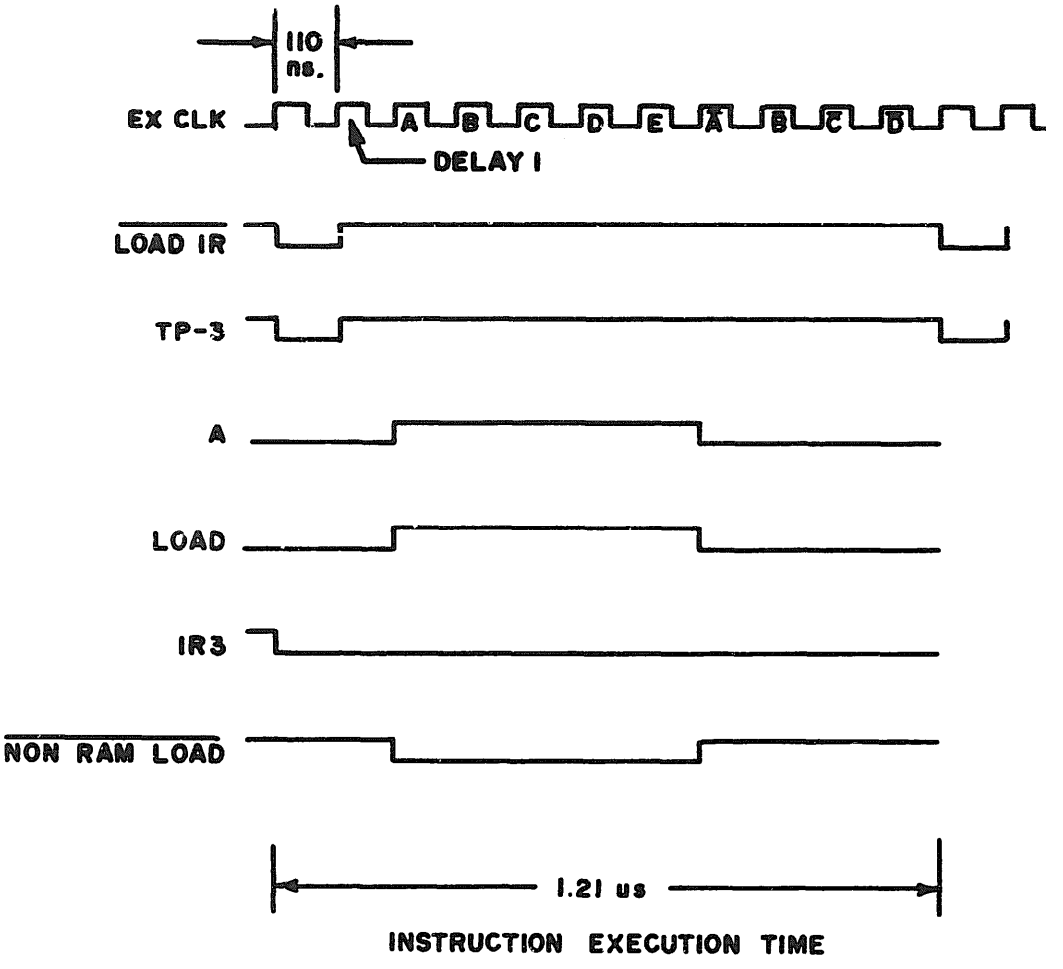
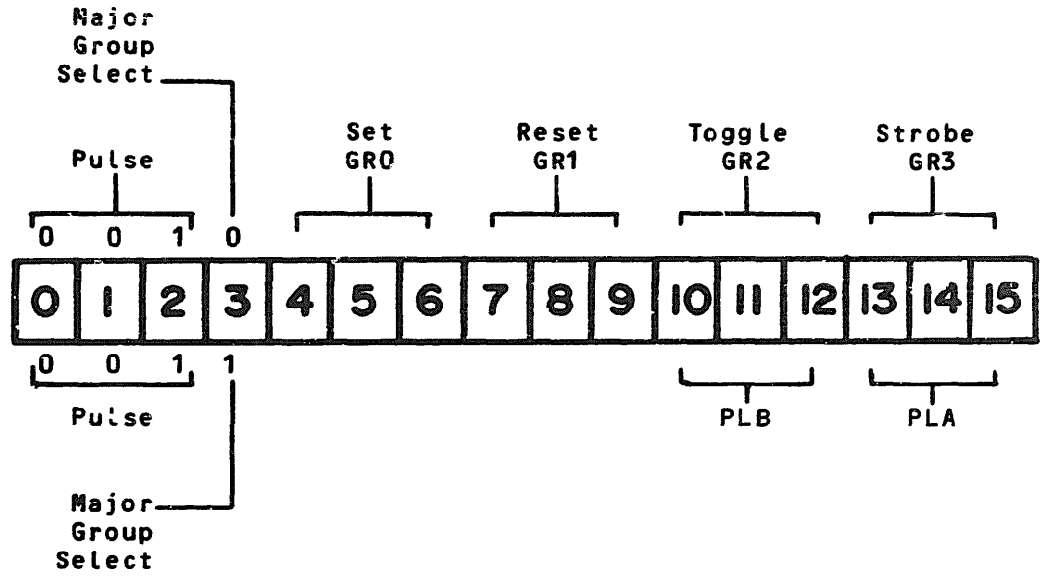


Figure 4-21. - Load Instruction Timing Diagram



PC<--PC + 1

Figure 4-22. - Instruction Word Format - PULSE

GR0 (Set)

1	Set Inc FF
2	Set Dec FF
3	Enable KYBD
4	Set Req for Service
5	Set CHDISP 1 from Output Buffer
6	Set CHDISP 2 from Output Buffer
7	Set CHDISP 3 from Output Buffer

GR1 (Reset)

1	Reset Inc, Dec FF
2	Reset Sample, (EMSPLF)
3	Reset KYBD Register (DISABLE KYBD)
4	Reset Char Display
5	Reset Vert Position
6	Reset Switches
7	Halt

PLB (Pulse B)

1	Set RAM select 0 to 15
2	Set RAM select 16 to 31
*3	Load COMPARE latch from ACCM 2/20/74
**4	Load RAM from ACCUM
5	
*6	Set Single Mode
*7	Load ECTA

PLA (Pulse A)

*1	Load Buffer select 0, 1, 2, 3
*2	Load Top Space Crit
3	Toggle Run light
4	Toggle Speaker Alarm
5	
6	Shift SR2 by 1
7	General Reset

GR2 (Toggle)

*1	Load Bottom Window - LDBWL
*2	Load Top Window - LDTWL
3	Output Strobe
*4	Load Char Width
*5	Load Recog Group Status - (Bit 1 and 2 of accum)
6	Inc Kybd register
7	Load Switches

GR3 (Strobe)

1	Shift Output Buffer
2	Shift SR1 and 2 SSHTS
*3	Set CPU status, XLATE Latch
4	Inc Char 1
5	Inc Char 2
6	Inc Char 3
7	

PC<--PC + 1

ACCUM unchanged

IET = 1.1 usec

Pulse = 0.5 usec

* Instructions load contents of accumulator into specified latch. Accumulator should be set up before pulse instruction is executed.
** PLB 4 is only PULSE instruction which also specifies a RAM.

Figure 4-23. - Pulse Instructions

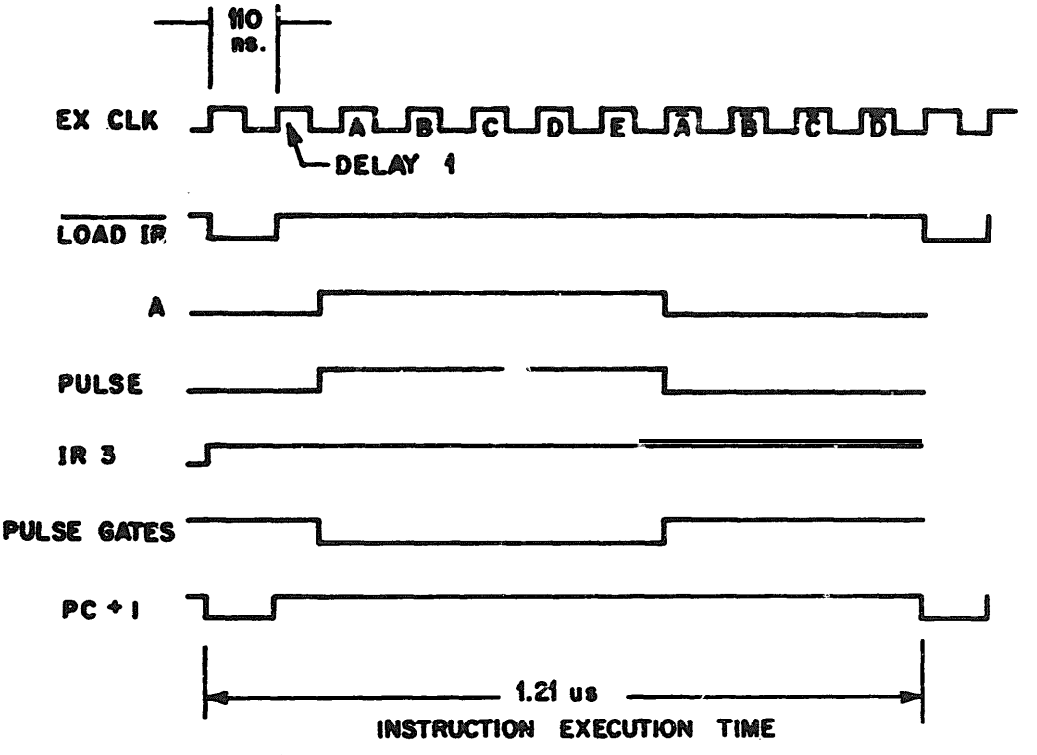
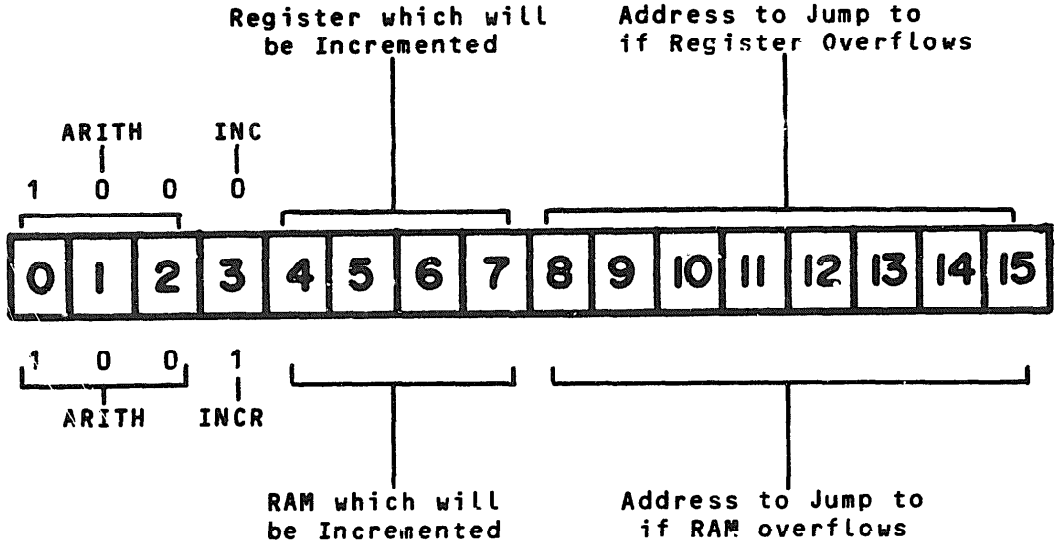


Figure 4-24. - Pulse Instruction Timing Diagram

No overflow
PC + 1→PC
ACC unchanged
Reg + 1→Reg

Overflow
Add→PC0 to 7



No overflow
PC + 1→PC
RAM + 1→RAM and ACC
IET = 1.21 usec

Overflow
Add→PC0 to 7
RAM + 1→RAM and ACC
IET = 1.65 usec

INC

2 Inc Top Margin
3 Inc Left/Right Margin
4 Read Switches (Shift switch shift register by 1)
5 Decrement Top Margin

Figure 4-25. - Instruction Word Format - ARITH (INC/INCR)

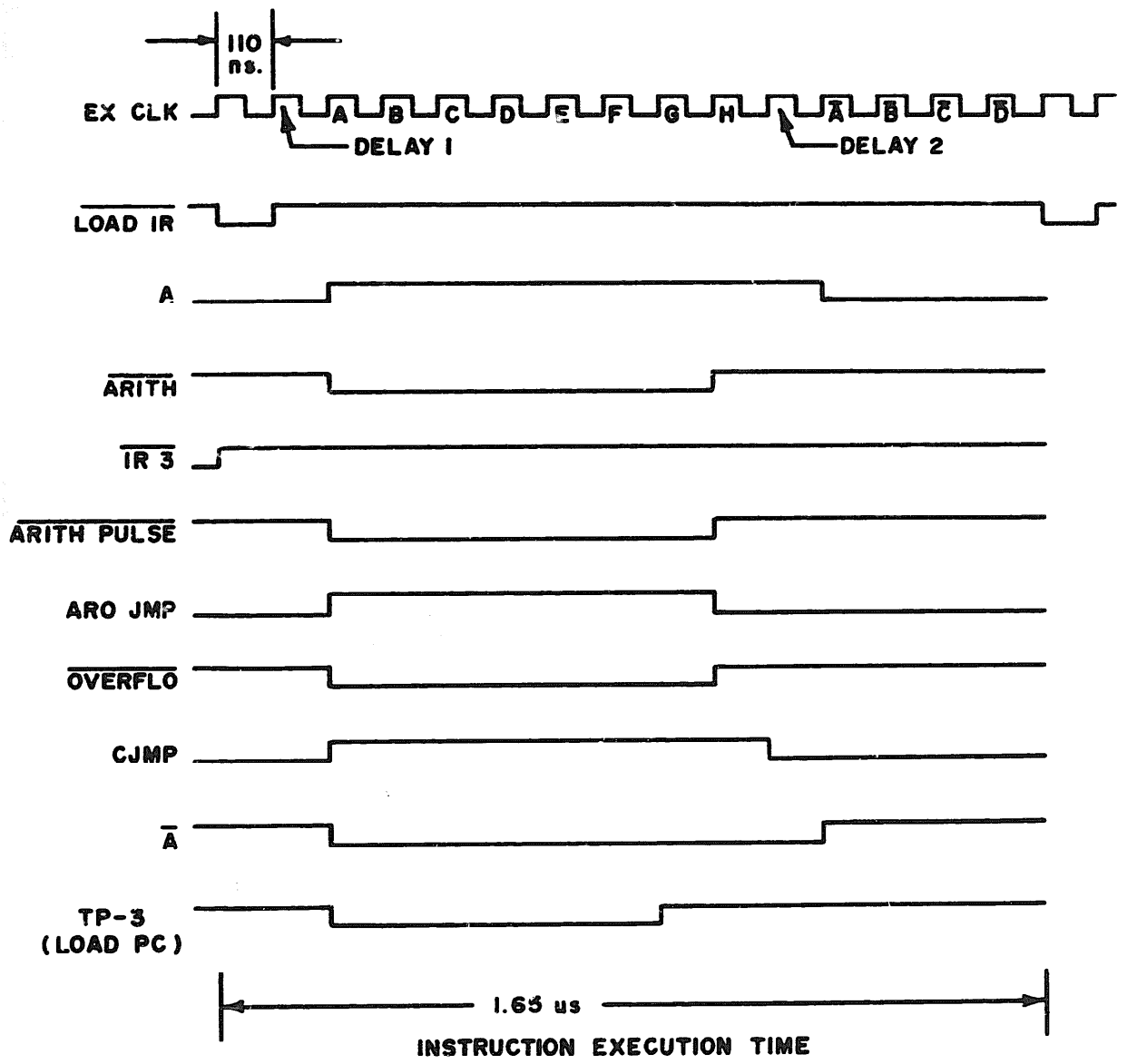


Figure 4-26. - ARITH Instruction Timing Diagram

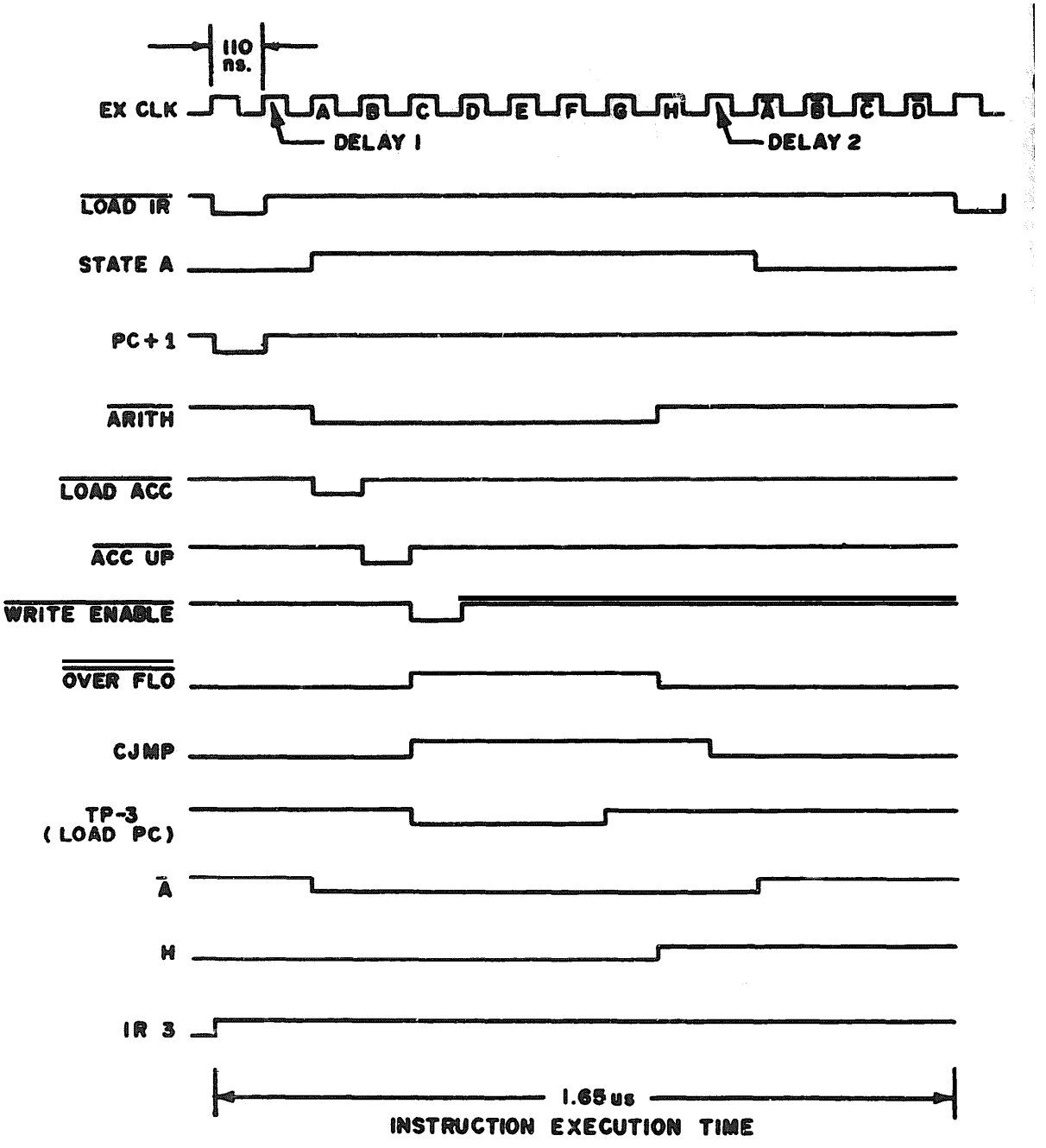


Figure 4-27. - ARITH (Jump) Instruction Timing Diagram

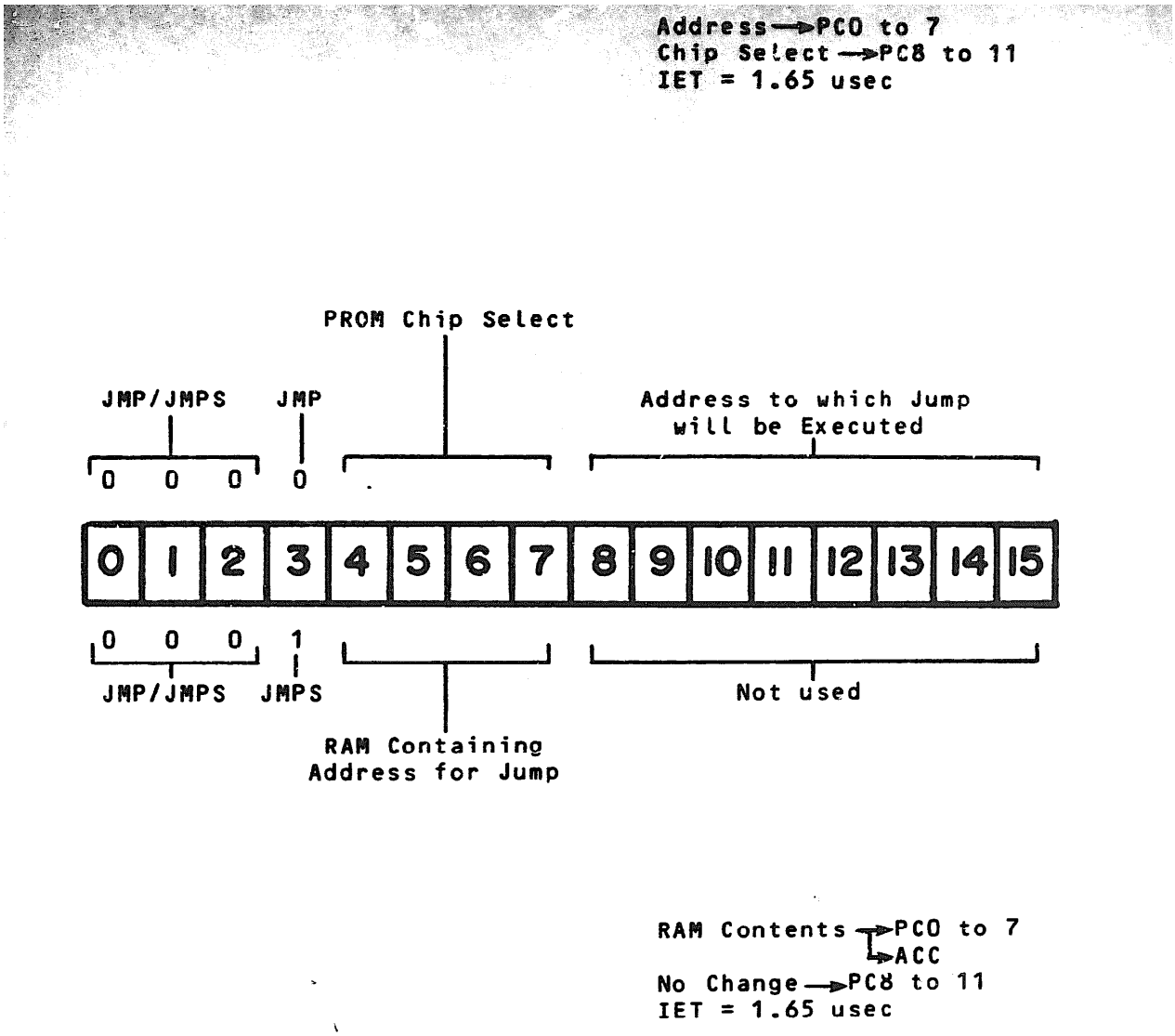


Figure 4-28. - Instruction Word Format - JMP/JMPS

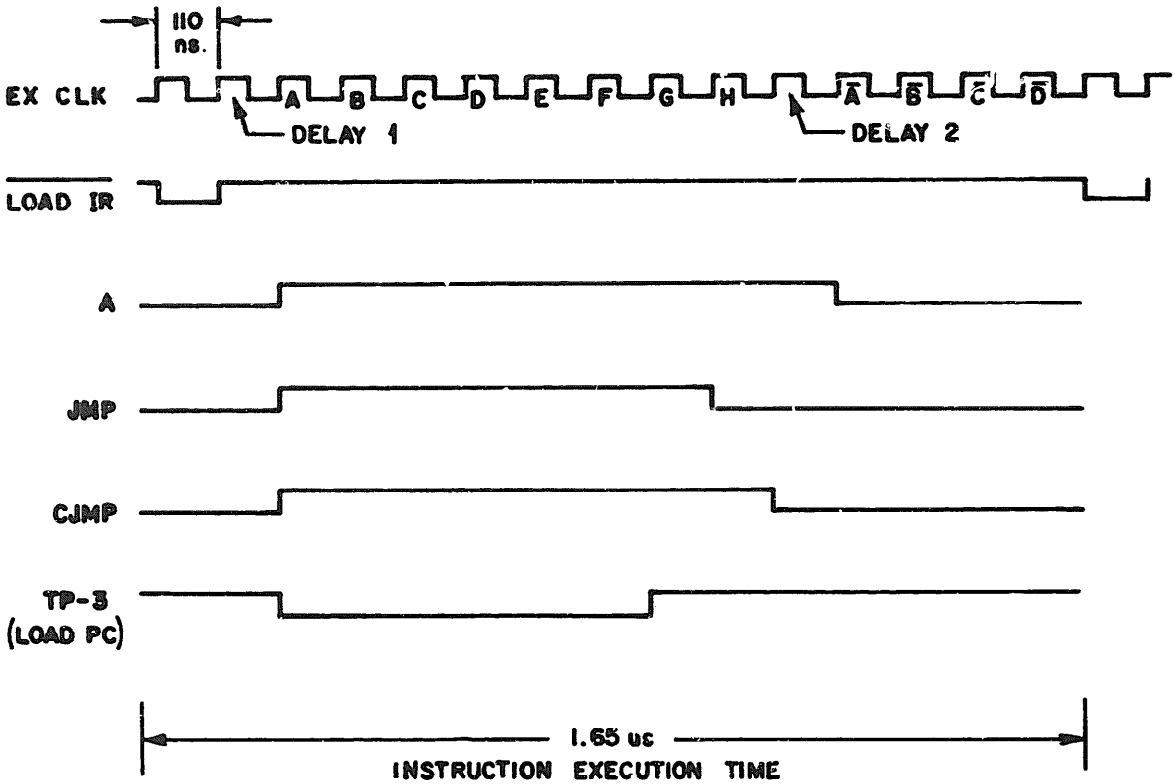


Figure 4-29. - Jump (Direct) Instruction Timing Diagram

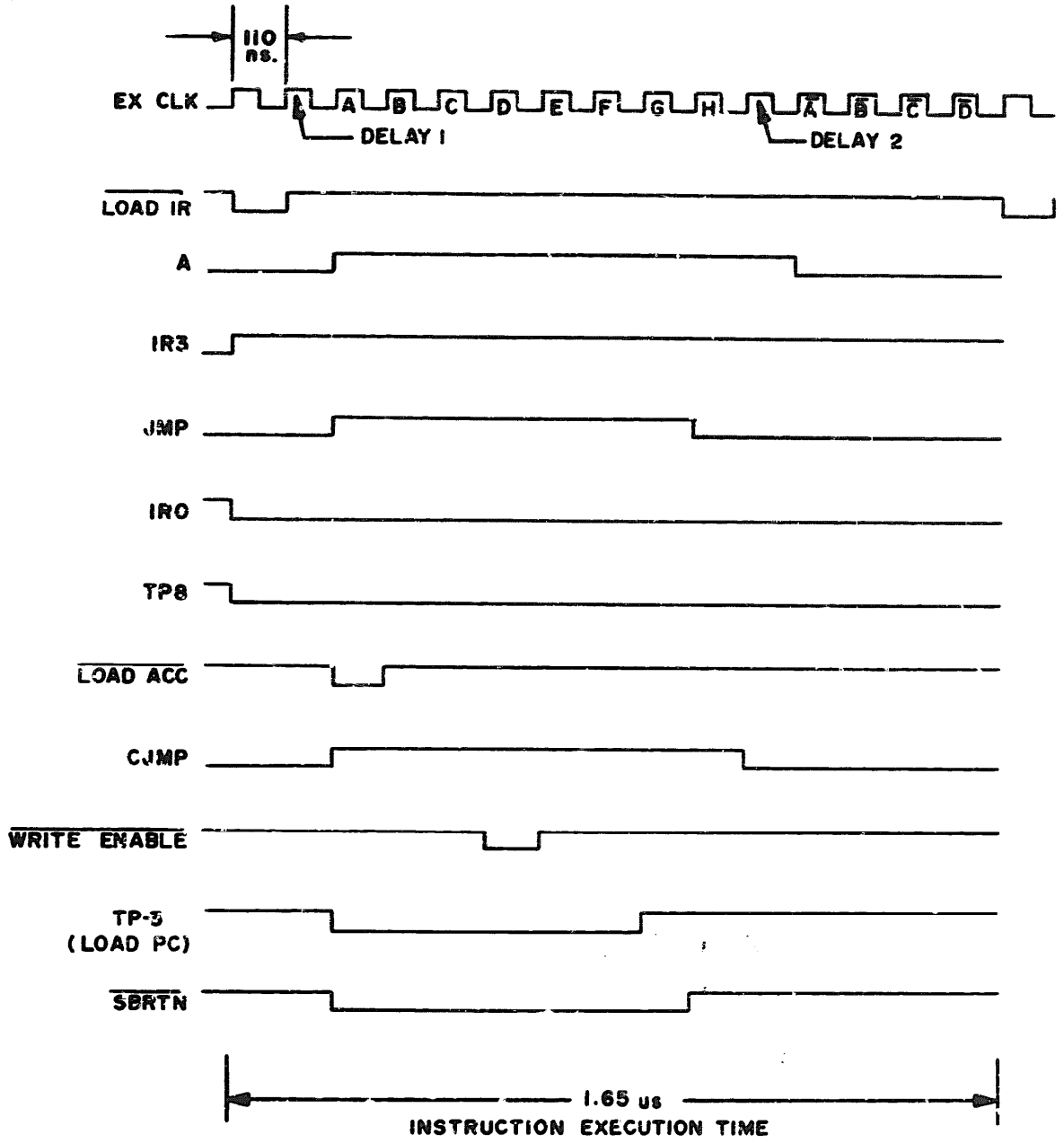


Figure 4-30. - Jump (Indirect) Instruction Timing Diagram

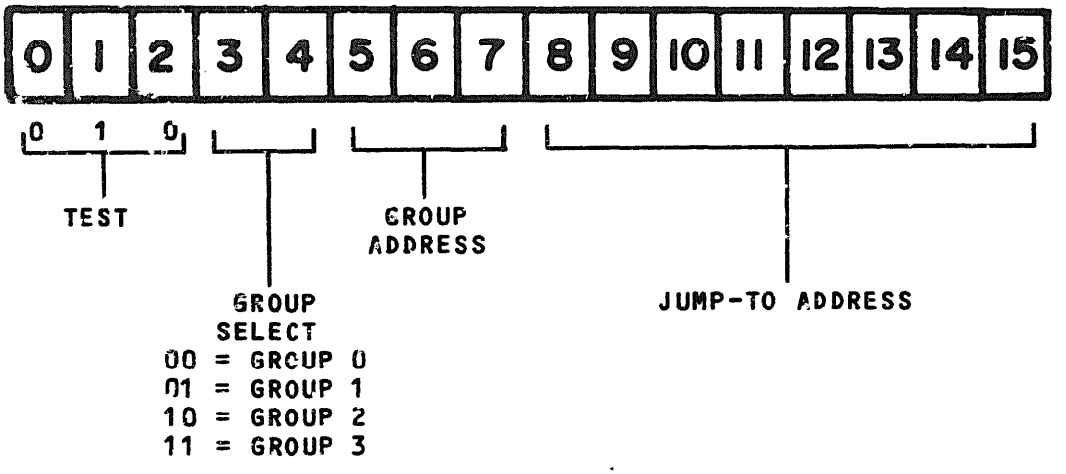


Figure 4-31. - Instruction Word Format - TST

		Function			
G	0	Greater Than		0	Recog ON
R	1	Equal		1	Step Up
O	2	Top Space Zero TSZF		2	Step Down
U	3	Bot Space Zero BSZF		3	VMF1 (Buf) see note 1
P	4	SR1, 2 Shifting SCCF	Group	4	Left of Horiz. Margin
	5	FB1	2	5	VMF2 (Buf) see note 1
0	6	FB2		6	Paper Present
	7	FC1		7	Left Stop
G	0	Single Cycle		0	Rollers Stopped
R	1	Pop Flop POPF		1	Head not in Motion
O	2	Char. Broken Flop BKNF		2	Start
U	3	Sample EMSPLF		3	Stop
P	4	Char. Too Tall	Group	4	Continue
	5	Single	3	5	SIMV
1	6	Unrecog. Char.		6	TCHF (Buffer) see note 2
	7	Just ON		7	Unrecog. Flag (Buffer) see note 3

TEST TRUE	TEST FALSE
Add-->PC 0 to 7	PC<--PC + 1
Add-->ACCM	ACCM Unchanged
IET = 1.65 usec	IET = 1.21 usec

note 1: VMF1=1) VMF2=1) Char. is too tall =>. crossout, scan edit corr.

VMF1=1) 2=0) Top space is zero, key optics stop

VMF1=0) 2=1) Bottom space is zero, key optics stop

note 2: TCHF=1 - touching char., horiz. crossout, scan edit corr.

note 3: UNRECG. flag=1 - bad recognition, key optics stop

Figure 4-32. - TST Instructions

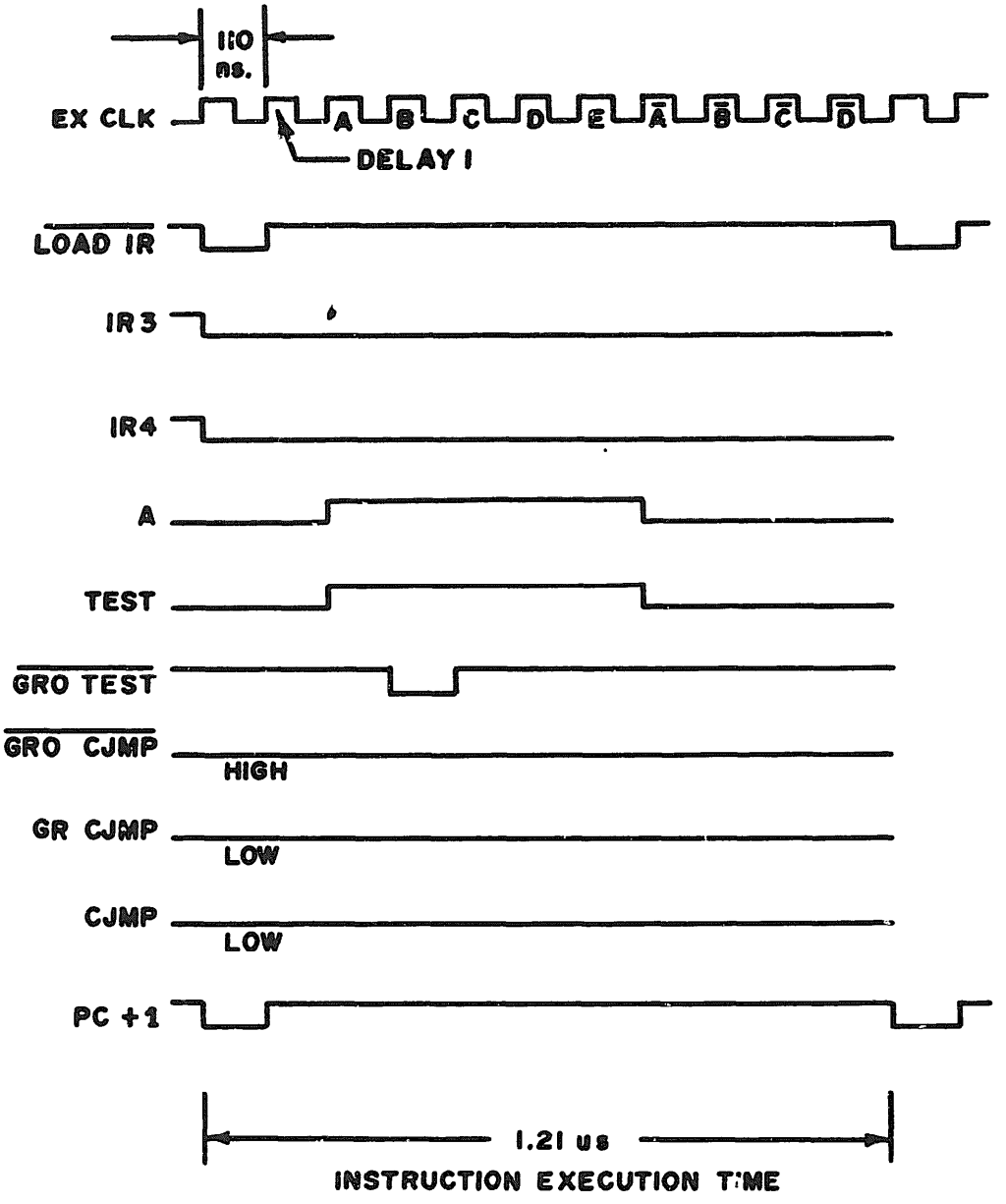


Figure 4-33. - Instruction Timing Diagram

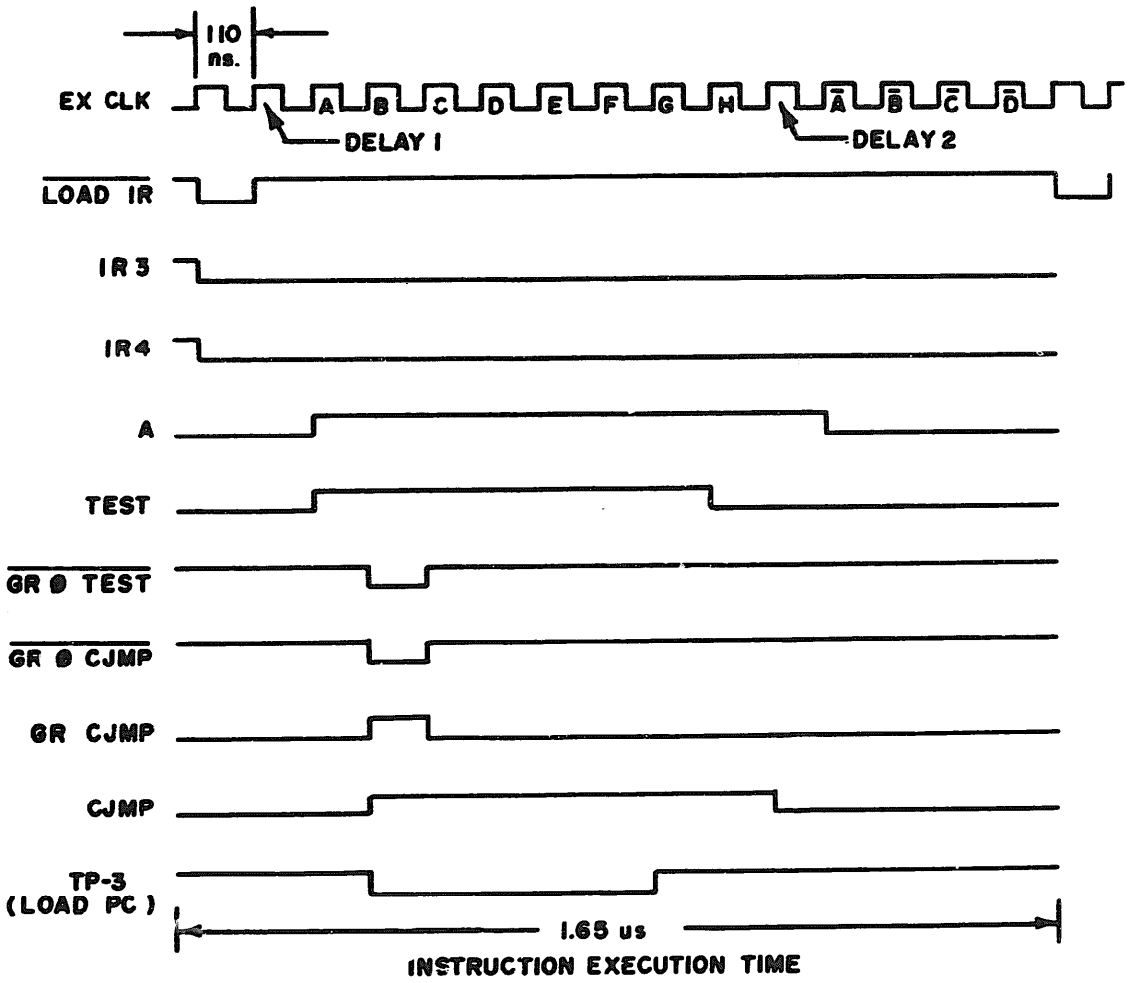
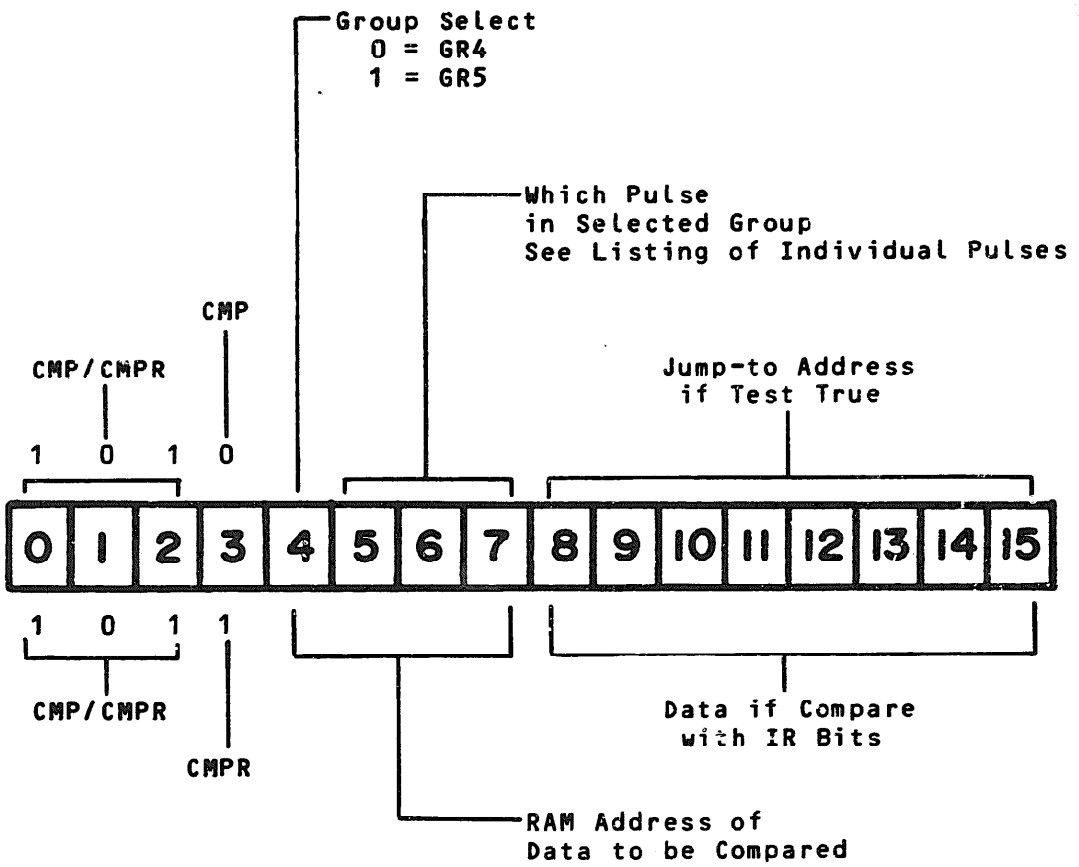


Figure 4-34. - TST (IMP) Instruction Timing Diagram

Test Pulse
PC + 1 PC
IET = 1.21 usec
Test True
PC<--Jump to ADDR
ACC<--Jump to ADDR
IET = 1.65 usec



PC + 1⟶PC
ACC<--RAM
IET = 1.21 usec

Figure 4-35. - Instruction Word Format - CMP/CMPR

Instruction: CMP

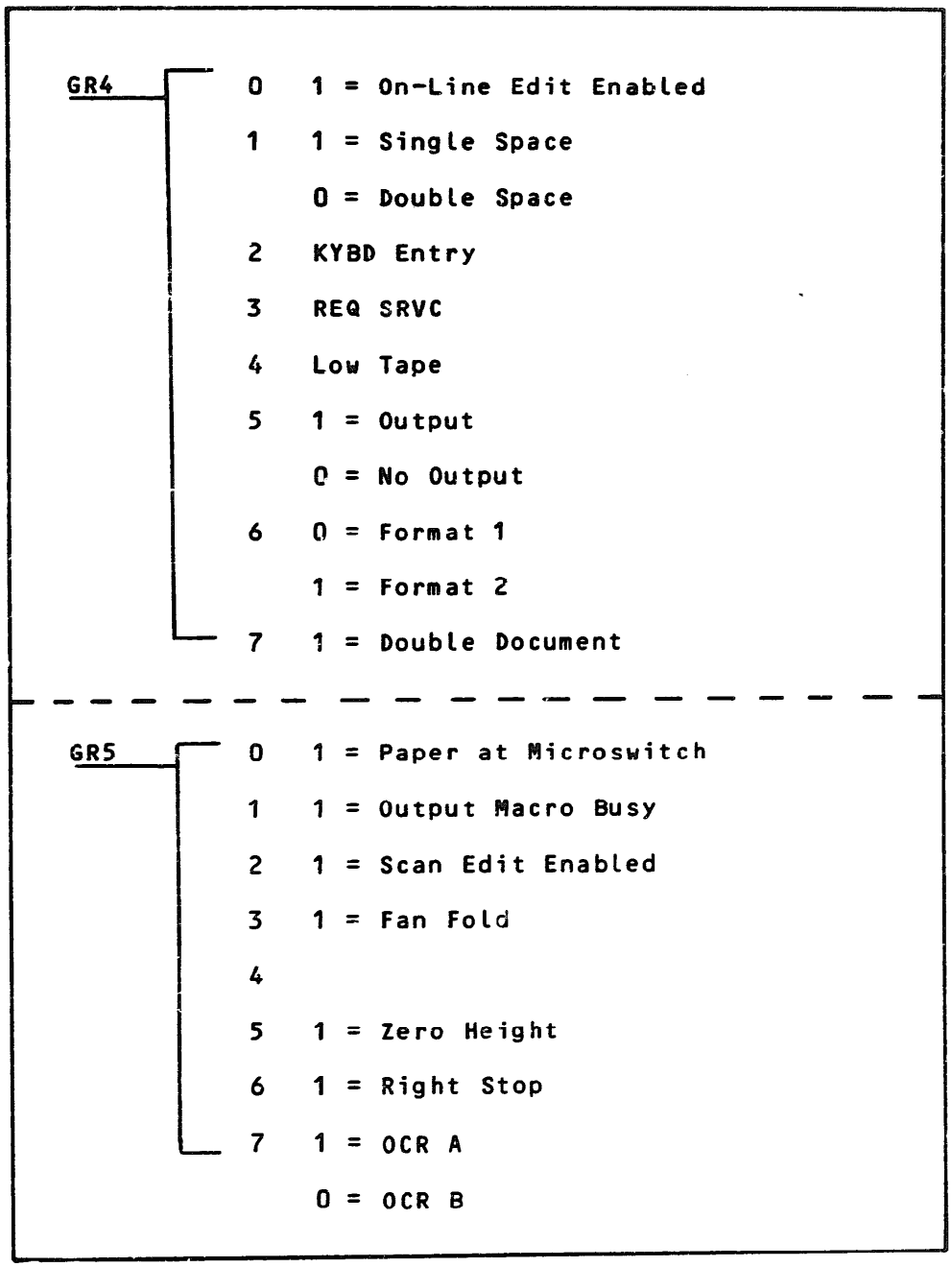


Figure 4-36. - CMP Instructions

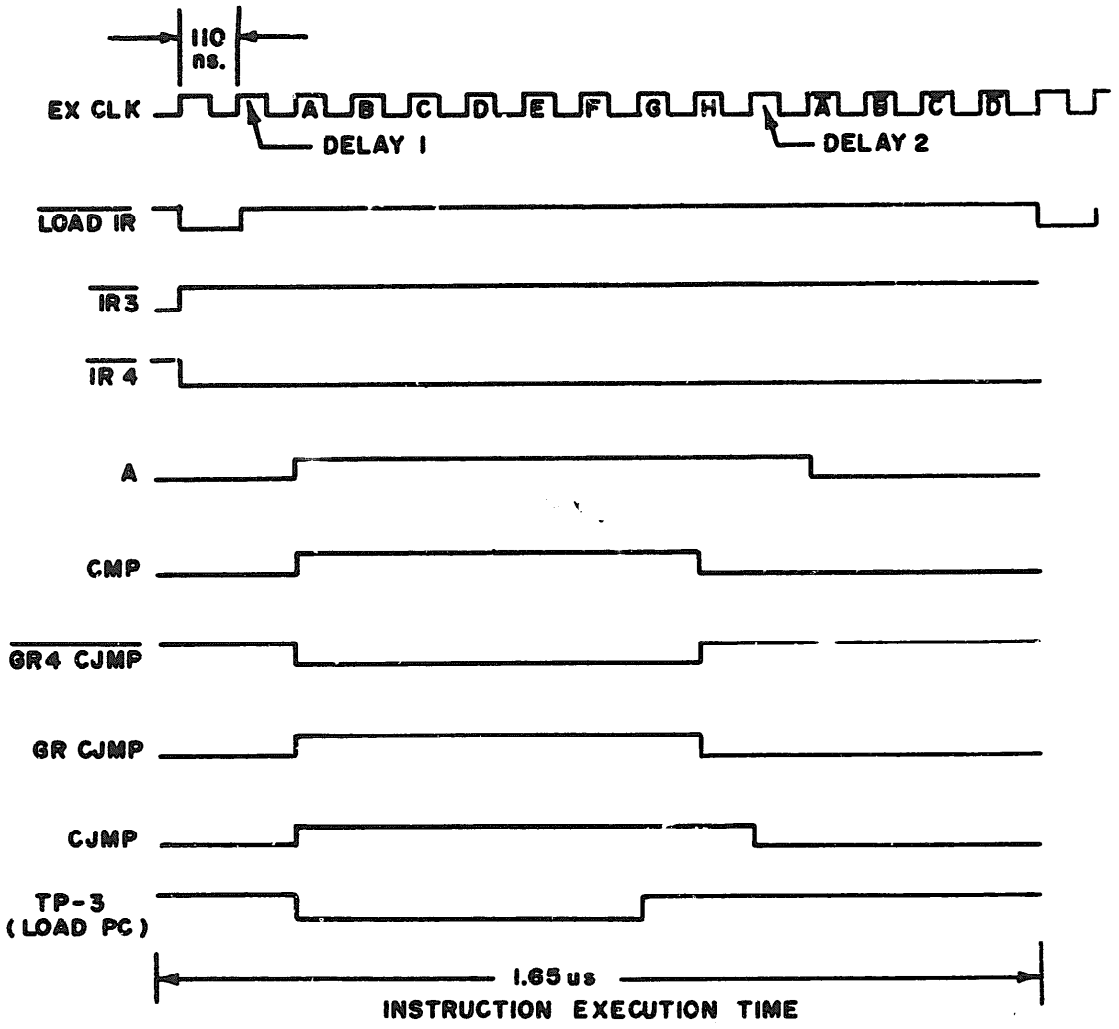


Figure 4-37. - CMP (Jump) Instruction Timing Diagram

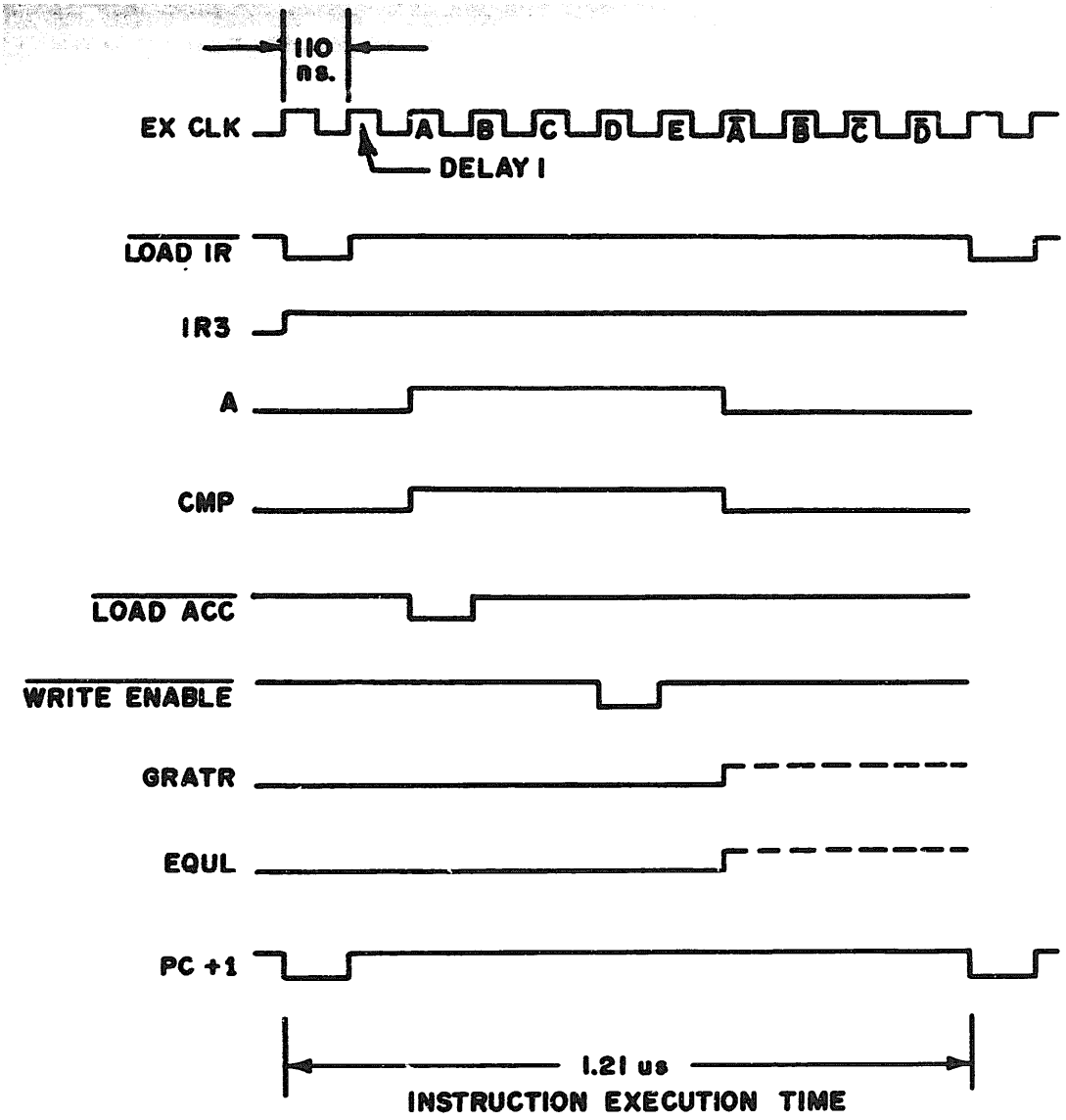


Figure 4-38. - Compare (CMPR) Instruction Timing Diagram

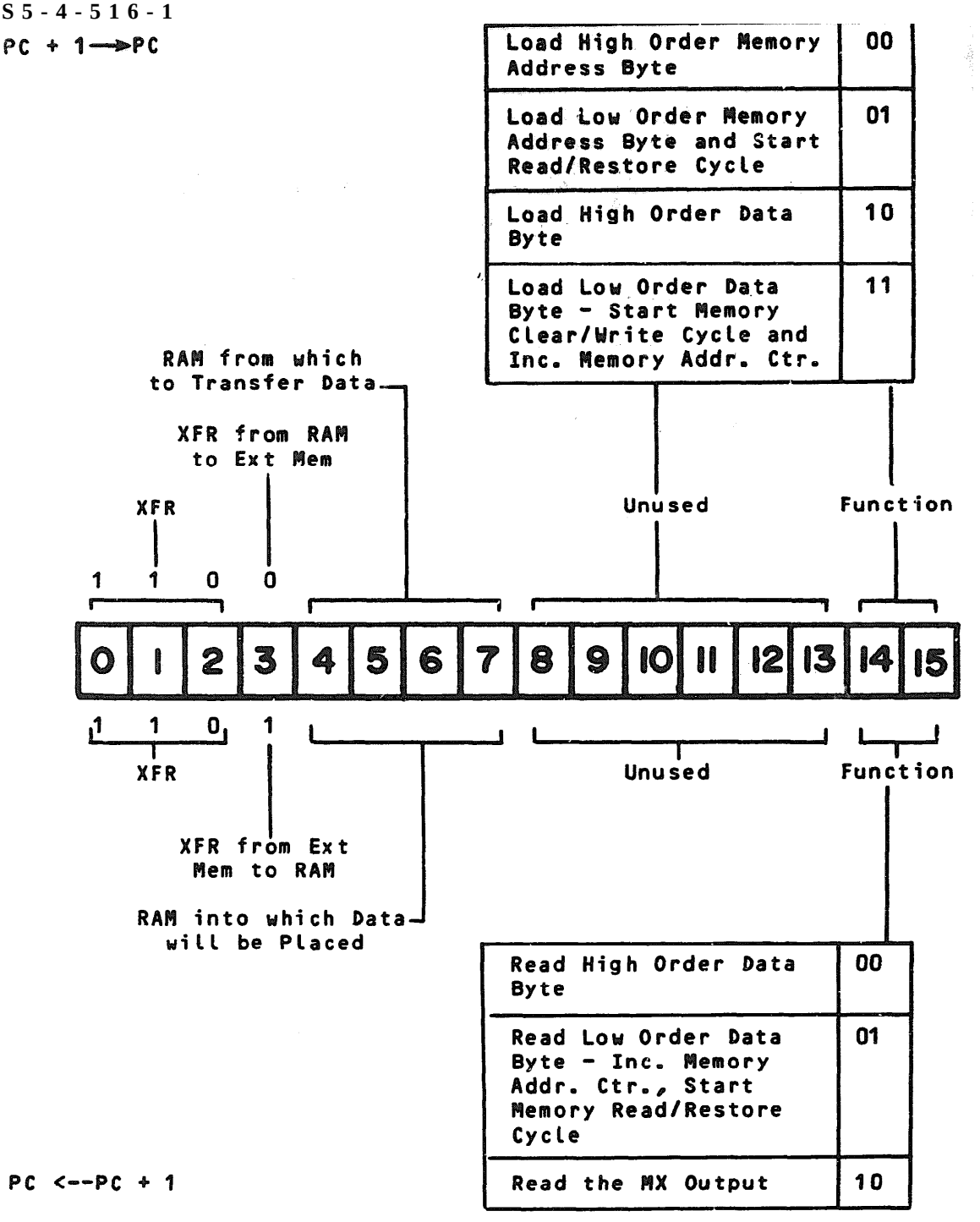


Figure 4-39. - Instruction Word Format - XFR

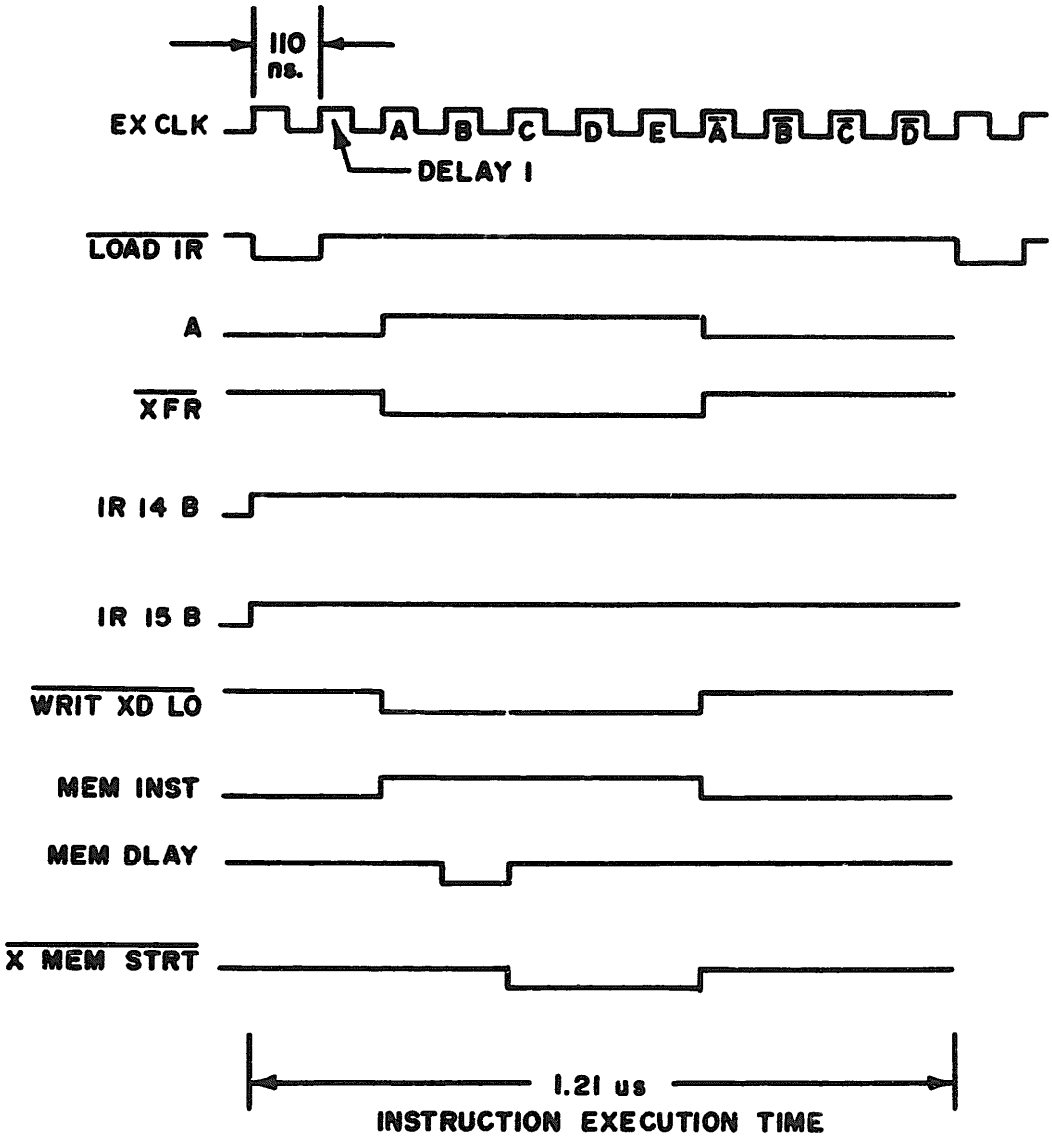


Figure 4-40. - Transfer (XFR) Instruction Timing Diagram

CHAPTER 5

PREVENTIVE MAINTENANCE

5-1. INTRODUCTION. - This chapter contains the necessary preventive maintenance procedures that should be performed periodically to prevent major equipment failures. Preventive maintenance depends primarily upon performance checks of the equipment, and includes visual inspection of mechanical components. Visual inspections aid in the discovery of conditions, which,. if not remedied, may result in faulty operation, unwanted service interruptions, and breakdowns. Adherence to the preventive maintenance procedures presented herein ensures optimum equipment performance, maximum service life, and minimum down time resulting from equipment failure.

5-2. TOOLS AND TEST EQUIPMENT REQUIRED. -

a. Standard Tools and Test Equipment. - Standard test equipment required for preventive maintenance of the ALPHA is listed in table 5-1. The table contains the name of the test equipment, manufacturer, and its application. Tools normally found in a maintenance tool box are not listed.

TABLE 5-1

Standard Tools and Test Equipment

NOMENCLATURE	ALTERNATE MANUFACTURER AND PART NUMBER	APPLICATION
Oscilloscope AN/USM-196	Tektronix, Type 545A with probe	Observe wave-shapes
Voltmeter	Cimron, Type 6000 or equivalent	Measure voltages
Multimeter AN/PSM-6	Simpson, Type 260	Check continuity

TABLE 5-2

Special Tools, Test Fixtures and Test Equipment

NOMENCLATURE	PART OR MODEL NO.	APPLICATION
Clutch Alignment Tool	CompuScan 101907	Align clutch in stack feeder assembly
Bearing Inserter	CompuScan 102005	Remove/insert bearing in side plates of upper and lower platen of Read Head and paper drive assembly.
Bearing Remover	CompuScan 102006	
Vertical Encoder Gear Holder	CompuScan 102007	Set split gears on encoder.
Test Set	TS-3596/GYX	Test ALPHA circuits

b. Special Tools, Test Fixtures, and Test Equipment. - Special tools, test fixtures and test equipment required for preventive maintenance procedures are listed in table 5-2. Table 5-2 contains the name of the tools, fixtures, and test equipment, and their manufacturers and application.

5-3. PREVENTATIVE MAINTENANCE SCHEDULE. -To ensure optimum operating performance of the ALPHA, the preventive maintenance schedule set forth in table 5-3 should be rigidly observed. Table 5-3 lists the maintenance routine and the intervals at which the routine should be performed,

5-4. INSPECTION. - Periodic inspections should be made to determine if any unusual or abnormal wear is occurring and to determine the need for cleaning. Particular attention must be paid to wear of belts and rollers and to dust out paper residue that may collect inside the machine.

5-5. CLEANING - Proper cleaning of the machine is essential for efficient operation. When cleaning, do not allow any liquid to run or drip into the machine. Similarly, when cleaning with compressed air, use only moderate pressure to avoid injury to components, Clean the machine as follows:

a. Exterior Surface. - Exterior surfaces may be cleaned with a cloth moistened with a detergent solution.

Note: Do not apply aerosol spray cleansers directly to the exterior of the machine.

b. Interior. - The interior of the machine may be cleaned as required with compressed air and/or a vacuum

TABLE 5-3

Preventative Maintenance Schedule

Period	Item	Action
Daily	1. SRECO Test	Test SRECO operation (para 5-8)
Quarterly	1. Double Page Detector	Adjust double page detector circuit (para 6-12a)
	2. Read Head and Roller Drift	Adjust read head and roller drift (para 6-12b)
	3. Power Supply	Measure the power supply voltages (para 6-14)
	4. Upper Platen	Inspect and clean upper platen (para 5-5d)
	5. ALPHA	Remove dust and dirt (para 5-5a, b)
	6. Stack Feeder	Clean and inspect stack feeder (para 5-5c)
	7. Lower Assembly	Clean and inspect lower assembly (para 5-7)
	8. Doors	Check that doors open easily and close securely. If doors do not open and close properly, notify appropriate maintenance personnel to perform corrective action as may be required.
	9. Cabinet	Check for dents, scratches, and rusted or bare metal. Notify appropriate maintenance personnel regarding dents greater than one-quarter inch that impair operation of doors.

WARNING

TO PREVENT INJURY TO PERSONNEL, ENSURE THAT MAIN POWER SWITCH (FIG. 3-2) IS IN THE OFF POSITION DURING THE REMAINING PREVENTIVE MAINTENANCE SCHEDULE PROCEDURES.

TABLE 5-3

Preventative Maintenance Schedule (continued)

Period	Item	Action
Quarterly (cont.)	10. Switches	Operate switches. Performance should be smooth and positive; detents should hold switch firmly in selected position. Spring loaded switches should return sharply (snap) to their off position.
	11. Fuses	Check that properly rated fuses a e in fuseholders. Replace incorrectly rated fuses.
	12. Connectors	Check that all connections are tight. Tighten loose connectors, if required.
	13. Electrical Components	Check electrical components for bulges, discoloration, and blisters. Replace defective component as described in corrective maintenance, chapter 6.
	14. Cables	Check all interconnecting and intraconnecting cables for cracked cut, or frayed insulation. Repair or replace defective cables as described in corrective maintenance, chapter 6.
	15. Cabinet Access Door Hinges	Lubricate with Type 100 centistroke viscosity G.E. Versilube Silicone Oil (OH).
	16. Read Head Rails	Lubricate with a thin film of Anderol No. 795.

cleaner. This is accomplished as follows:

(1) Disconnect main power cord.

(2) Open rear access door (Fig. A-35) to expose main wire wrap assembly.

(3) Loosen the knurled knob and swing out the main wire wrap assembly; this will expose the rear of the power supply.

(4) Carefully remove and clean each board if required. Use a soft brush or a gentle stream of clean dry compressed air to remove any dust or dirt and a contact cleaner for the electrical contacts.

(5) Blow out and vacuum the rear of the power supply.

(6) Close and secure main wire wrap assembly and rear access panel.

(7) Remove the front access panel by lifting it from the bottom straight up approximately 1/2 inch.

(8) Loosen the knurled knob and swing out the hinged panel; this will expose the external memory board-

(9) Blow out and vacuum the front port ion of the power supply.

(10) Upon completion, secure the hinged panel and front access panel. Do not apply excess pressure on the panel as the top screws could break.

c. Stack Feeder Assembly,- Periodically the Stack Feeder plastic belts and paper handler assembly rollers acquire a buildup of waxes and/or sizing from the paper stock. To remove this buildup of foreign matter proceed as follows:

(1) Set the POWER switch on the Format Panel to ON-

(2) Toggle the START position of the START-CONTINUE switch on the Control Panel.

(3) Moisten a gauze pad or cloth wit h denatured alcohol.

(4) As the Stack Feeder operates, hold the pad against each of the rotating plastic belts, one at a time.

CAUTION: Do not allow the cloth or pad to be pulled into the mechanism.

d. Paper Handler Assembly. - Clean the Paper Handler Assembly as follows:

(1) Turn power off.

(2) Loosen the two Control Console hand screws (Fig. A-34) fastening the Control Console Assembly to the Cabinet Assembly.

(3) Slowly raise the Control Console from the front until it stops in the vertical position,

(4) Using a gauze pad or cloth moistened with alcohol, clean the rollers by turning them by hand, and the upper and lower platens.

(5) Slowly lower the Control Console Assembly to the Cabinet Assembly and fasten in place with two Control Console screws.

e. Paper Viewing Window and Mirrors. - If the viewing window or mirror(s) become dirty, proceed as follows:

(1) Gain access to the viewer window and mirrors by following the procedure given in Chapter 6, paragraph 6-9(a) (accessing the Paper Handling Assembly),

(2) Clean the window or mirror(s) with a lens tissue or lint free cloth. In some cases it may become necessary to lightly moisten the cleaning cloth with a commercial cleaner to remove accumulations of foreign matter.

CAUTION: Always handle the mirrors by metal frames; this will keep oil from the fingers off the reflecting surfaces.

5-6. INSPECT AND CLEAN STACK FEEDER. -

a. Place unit in off line status.

b. Remove any paper from stack feeder.

c. Turn POWER switch to OFF,

d. Loosen the two knurled locking screws in the front of the unit and raise the operating console to the full open position.

e. Loosen the single page feeder assembly retaining screw and carefully slide the unit straight out of the cabinet.

(1) Place the page feeder on its side on a flat padded surface.

f. Remove the four corner screws from the bottom of the unit.

(1) Place the unit in its normal upright position.

g. Remove the four flat head screws from the back, two in each lower rear corner.

h. Carefully lift the cover off the page feeder assembly.

i. Blow out the page feeder assembly with low pressure filtered air.

(1) Use the small parts cleaning brush to dust all interior and exterior portions.

j. Inspect the page feeder assembly for:

(1) Presence of foreign matter.

(2) Loose or cracked drive belts.

(3) Loose or missing hardware.

(4) Burned or cracked wiring.

(5) Loose mounting of solenoids.

CAUTION: When installing page feeder back into ALPHA, extreme caution must be exercised to avoid damaging exposed drive train.

k. Install page feeder in ALPHA and secure with the retaining screw.

l. Turn POWER switch to ON.

m. Toggle STOP, RESET, and START.

n. Inspect unit for:

(1) Excessive bearing noise or vibration.

(2) Misalignment of pulleys, shafts or drive belts.

(3) Smooth operation of paper feed mechanism and clutch.

o. Toggle RESET.

(1) Inspect for smooth operation of the brake assembly.

p. Turn POWER switch to OFF.

q. Loosen the page feeder assembly retaining screw and carefully slide the unit straight out of the cabinet.

(1) Place the page feeder on the flat padded surface.

r. Replace the cover on the stack feeder and secure with the eight screws previously removed.

s. Install the paper feeder in the ALPHA and secure with the retaining screw.

t. Lower the operating console and secure with the two knurled locking scre

5-7. CLEAN AND INSPECT LOWER ASSEMBLY. -

a. Open the rear door of the ALPHA.

b. Unlatch the mother board and swing it open.

c. Remove the lower front cover.

d. Open the door containing the external memory assembly.

e. Using clean dry Cow pressure air and a soft cleaning brush blow out and clean:

(1) Entire lower assembly including power supply.

(2) Exterior only of the external memory and inter.. face card.

f. Inspect unit; look for:

(1) Loose, disconnected, or broken wires on mother board and lower assembly.

(2) Loose or missing I.C. on mother board.

(3) Loose or damaged cables.

(4) Presence of foreign matter.

(5) Discolored or scorched components.

(6) Cracked or frayed insulation.

(7) Loose connections.

(8) Loose Circuit cards.

(9) Bulged or leaking capacitors.

g. Close and secure the external memory door.

h. Replace the lower front cover.

i. Close and secure the mother board.

j. Close and secure the rear door.

k. Return equipment to normal. operating condition.

5-8. CHECKING SRECO VIA THE RAD PANEL. - The RAD Panel provides a means for checking the security of ALPHA operations from external monitoring. A failure of any of these tests indicates that the ALPHA operations may not be secure and the machine should not be placed back in on-line operation without proper corrective maintenance. The proper authority should be notified immediately of any failure in this area.

a. This test procedure should be performed daily.

b. To get to the test panel, open the rear door of the machine. Looking in, it is on the right side panel.

c. Normal operation is to have all switches in the "Off" position.

d. Turn switch "a" to the "On" position. Start scanning a sheet of test copy - that is one with every other character position blank.

e. Within two scanned lines an S2 and S3 error condition will appear.

f. Turn switch "a" to the "Off" position.

g. Repeat steps 4 to 6 for switches b, d, and e.

h. When running test sheet with switch "c" "On", all the spaces will be filled with the previous character read.

i. If all the above errors occur, that will indicate that the RAD Panel is functioning properly.

CHAPTER 6
CORRECTIVE MAINTENANCE

IMPORTANT NOTICE

THIS MANUAL CONTAINS NO ILLUSTRATED PARTS BREAKDOWN. ALL DATA RELATIVE TO FIGURES 7-1 THROUGH 7-35 REFERRED TO IN THIS PUBLICATION WILL BE FOUND IN T.O. 31S5-4-516-4 AND ARE LISTED AS FIGURES 1 THROUGH 35.

6-1. GENERAL. - Corrective maintenance must be performed after an equipment malfunction has been noted. Corrective maintenance procedures comprise minimum performance standards, diagnostic routines, trouble analysis, removal, repair, replacement, adjustment, and calibration. The method of determining the location of a malfunction is covered in paragraph 6-4. Upon completion of the corrective maintenance, the minimum performance as specified in paragraph 3-5, Operation, must be performed to ensure satisfactory operation of ALPHA. Troubles encountered in the ALPHA will generally provide some clue as to their causes. In performing corrective maintenance, first isolate the cause of the trouble using the usual methods of elimination.

a. Testing. - Make certain that the connecting equipment to the ALPHA is functioning properly. All discussion in this chapter is based on the assumption that test equipment used for testing the ALPHA is operating properly at the time of test. Before repairing or testing the ALPHA, maintenance personnel should be thoroughly familiar with the theory of operation, mechanical assemblies, and operational procedures.

b. Troubleshooting Limitation. - The troubleshooting procedures in this chapter indicate malfunctions and remedies for a unit that has already been installed and was operating

properly at the time a malfunction occurred. If the suggested remedies do not correct a malfunction, the wiring must be checked and repaired through use of the mnemonic and point-to-point wiring lists and wiring and schematic diagrams. Schematic, wiring, and power distribution diagrams are illustrated in the Appendix.

6-2. TOOLS AND TEST EQUIPMENT REQUIRED. -

a. Standard Tools and Test Equipment. - Standard tools and test equipment required for corrective maintenance of the ALPHA includes all the test equipment listed in the preventive maintenance chapter (chapter 5) and is supplemented by the standard tools listed in table 6-1. Table 6-1 contains the name and type or size of all standard tools used for the removal and replacement of components in the following paragraphs.

b. Special Tools and Test Fixtures. - Special tools and test fixtures required for corrective maintenance of the equipment includes all the items listed in table 5-2 and is supplemented by the items Listed in table 6-2. Table 6-2 identifies the special tools and test fixtures and gives their application,

6-3. REFERENCE DESIGNATIONS- The unit numbering method of assigning reference designations has been used to identify units, assemblies, subassemblies, and parts. This method has been expanded as much as necessary to adequately cover the various degrees of subdivision of the equipment. Examples of

Table 6-1

Standard Tools

NOMENCLATURE	SIZE
Screwdriver Set, Phillips Head	No. 1, 2, 3, 4
Screwdriver Set, Standard Blade	3/16, 1/4, 9/32, 5/16, 3/8
Screw Starter, Magnetic	Standard
Nut Driver Set	1/4, 5/16, 11/32, 3/8, and 7/16 inches dimension across flats.
Hammer	4 oz.
Pliers, Slip Joint	Standard
Pliers, Long Nose	Standard
Pliers, Needle Nose	Standard
Pliers, Gripping	Standard
Pliers, Diagonal	Standard
Wrench Set, Open End	1/4, 5/16, 3/8, 7/16, 1/2, 9/16, 19/32, 5/8, 11/16, and 3/4 inch dimension across flats
Pliers, Standard, Retaining Ring	Waldes Truarc Inc., Model M152
Feeler Gauges, Set	Standard
Feeler Gauges, Long	.007, 015
Punch, Pin	3/32, 1/8, 3/16 point diameter
File, Flat, Needle	Standard
Wrench Set, Hex Head	0.050, 1/16, 5/64, 3/32, 7/64, 1/8, 9/64, 5/32
	Snap-On AW-9K or equivalent
Wire Wrap Tool, Hand Operated	Gardner-Denver Model 14H-1C

Table 6-1

Standard Tools (continued)

NOMENCLATURE	SIZE
Wrapping Bit, 28 Gauge	Gardner-Denver Model 504155 (Use with Wire Wrap Tool 14H-1C)
Sleeve, Bit	Gardner-Denver Model 18840 (Use with 28 Gauge Bit 504155
Unwrapping Tool, Dual Left/ Right Hand Operated	Gardner-Denver Model 500130
Cutting and Skinning Tool, 28 Gauge	Gardner-Denver Model A-5406-1
Soldering Iron, Pencil	Standard
Braid Wire	Standard Sizes (Used for Desoldering Components from Printed Circuit Boards)
Spring Hook	No. 17113131
Spring Hook	No. 6313019
Set of Allen Wrenches	Standard

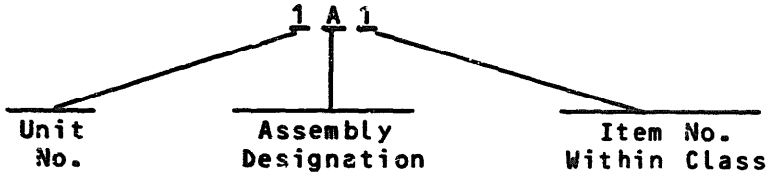
Table 6-2

Special Tools and Test Fixtures

NOMENCLATURE	PART OR MODEL NO.	APPLICATION
Extender Board	CompuScan P/N 102933	Extend printed circuit boards from assembly for trouble-shooting purposes.
Dip Clip	Pomona Electric 3916	Provide access to integrated circuit leads for test.
Extractor Tool	Molex Prod. Corp. HT-2038	Remove damaged pins from connector.
Extractor Tool	Molex Prod. Corp. HT-2285	Remove damaged pins from connector.
Extractor Tool	Molex Prod. Corp. HT-A2174	Remove damaged pins from connector.
Lens Focusing Tool	CompuScan 101615	Used to rotate lens during focusing adjustment.
Clutch Aligning Tool	CompuScan 101614	Adjusts space on clutch shaft.

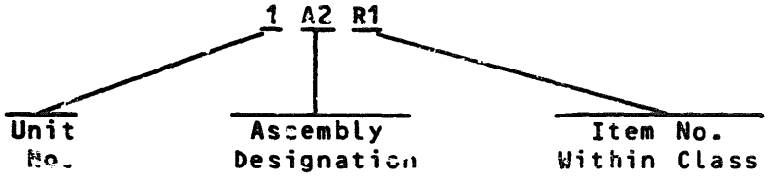
the unit numbering method and typical expansions are illustrated below:

Example:



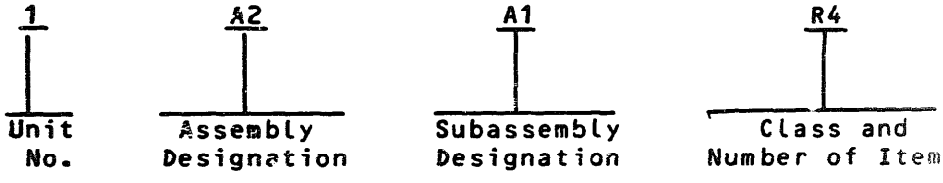
Read as: First (1) Assembly (A) of the First (1) Unit.

Example:



Read as: First (1) Resistor (R) of Second (2) Assembly in the First (1) Unit.

Example:



Read as: Fourth (4) Resistor (R) in the First (1) Subassembly (A) of the Second (2) Assembly (A) in the First (1) Unit

Note: The ALPHA consists of only one unit.

6-4. **GENERAL ANALYSIS PROCEDURES.** - Corrective maintenance on the ALPHA is required whenever a malfunction is discovered during normal operation due to improper recognition, paper feed failure, or causes indicated by lighted indicator lamps. The cause of a malfunction, once discovered, must be isolated first

to a defective assembly, next to a defective printed circuit board or individually mounted component, and lastly, if applicable, to a defective printed circuit board component. If adequate spares are available, the defective assembly or printed circuit board is normally replaced to return the ALPHA to operational status, and the assembly is then repaired during a regular scheduled maintenance period,

a. Visual Indication. - An LED display and LED indicator tamps are provided on the ALPHA to give the operator or maintenance technician an immediate indication of not only certain operating functions being performed but also of loss of power, paper jam, and other indications of malfunction listed and described in Operation, Chapter 3.

6-5. OVERALL TROUBLESHOOTING. - The troubleshooting information contained in table 6-3 shall be used to isolate faults to a maintenance significant part. The table is not so complete as to offer a listing of all possible failures of a unit, however, the most probable failures and remedies are listed. If one symptom has several probable causes, the most probable is discussed first. In the event that the malfunction cannot be identified using table 6-3, perform the troubleshooting test procedure provided in table 6-4. Perform this procedure from the beginning until the malfunction is identified.

6-6. TROUBLESHOOTING UTILIZING THE OPERATING PROGRAM. - Troubleshooting utilizing the ALPHA Operating Program can be accomplished to a certain extent by carefully and logically

analyzing the sequence of events, In order to scan text, we observe that the Read Head drives left and right, and the Vertical Servo positions the paper under the Read Head. Mechanical control of the paper is required before video can be acquired.

The Sequence of Events Flow Chart (Fig. 6-1) provides a logical flow of events which may be used to determine proper operation of the electro-mechanical portions of the ALPHA, Each event has associated with it a probable cause letter which relates to table 6-3. It is important that the events listed in the Flow Chart be used in the order specified as certain steps assume successful operation of previous steps.

When the electro-mechanical portion is working properly and characters are being misrecognized, the procedures listed in paragraph 6-7 should be followed to determine the source of trouble.

One portion of the electro-mechanical circuitry not checked by the Sequence of Events Flow Chart is the Double Page Detector. It may be checked as follows once it has been determined that no sequence of events problems exist.

a. Testing Double Page Detect. -

(1) Turn Power on; set Mode Selector switch to Operate-

(2) Tape or paste two pages together at edge and place into the Stack Feeder.

(3) Toggle Start.

(4) Allow pages to be pulled into the Stack Feeder-

(5) Once the paper gate rises allow them to pass through the Double Detector.

(6) As soon as the two pass between the LED and phototransistor, the ALPHA should stop, sound the alarm, and display a “Bell P2” error.

(7) If no double detect error is generated, adjust the detector via the following procedure:

b. Adjusting the Double Page Detect. -

(1) Raise the control console.

(2) Insert a double page between the two detector elements as described above.

(3) Measure the voltage between TP1 and TP2 on the rear of the control panel.

(4) Adjust the pot for 4 VDC with the double page.

(5) Insert a single page.

(6) Check that voltage is approximately 2 VDC.

(7) Recheck double page voltage.

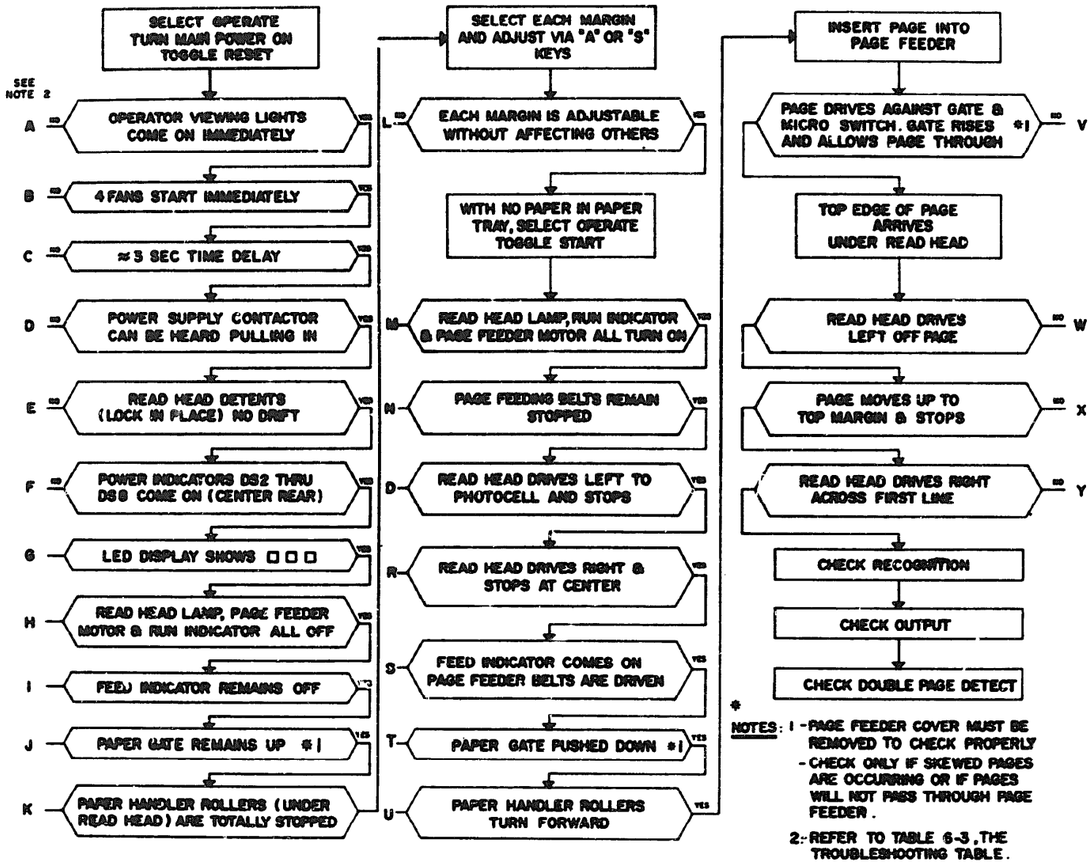


Figure 6-1. - Sequence of Events Troubleshooting Flow Chart

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart

FIG. 6-1	SYMPTOM	ACTION/REMEDY
A	Viewing lights did not light	See if fans are running A. If fans do not run (1) Check main fuse. (2) Check that machine is plugged in and that outlet is "live". B. If fans do run (1) Check Fuse F5. (2) Check 8 VAC from Power Supply.
B	One or two fans do not run	A. Both Paper Handler and Read Head Fans - F7 B. Paper Handler or Read Head Fans - not both Fan bad or wiring to fan bad C. Card Cage Fan - (1) Check F8 (2) Fan or wiring bad D. Power Supply Fan - Fan or wiring bad.

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOM	ACTION/REMEDY
C	No delay	A. Machine was not off long enough for Power Supply Fan to stop. B. Power Supply Wind Vane Micro Switch stuck on or contacts fused. C. Power Supply contactor stuck closed.
D	Power Supply contactor does not pull in	A. Power Supply Wind Vane Micro Switch stuck open. B. Fan blocked or not up to speed. C. Micro Switch contacts open. D. Power Supply contactor faulty - coil open or mechanically stuck.
E	Read Head A. Does not lock in place, remains free. B. Read Head drives quickly and uncontrollably to one side -	A. Never locks (1) Faulty Servo Fuses - F3 and F4. Observe DS2 and 3. (2) Faulty Servo Amplifier. (3) Faulty Servo Controller. B. Same as A.
	WARNING: Troublesheet with Servo Fuses (Fs and F4) removed.	

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOM	ACTION/REMEDY
	C. Drifts slowly to one side.	C. Horizontal Drift Adjustment Incorrect.
F	One LED (DS2-7) out	A. DS2 or 3 - LED faulty.
		B. DS4, 5, 6, 7 - Associated Power Supply or Fuse faulty.
		C. Power Supply has bad contactor.
G	LEDs do not show	A. Check that boards are plugged in.
	Null Null Null	B. Run Executive Macro Diagnostic.
H	Read Head Lamp, Page Feeder	A. All three are on - check Run Flop (1) 2C-5, 6.
	Motor, and Run Indicator are	B. Read Head Lamp on - others off.
	not all off.	(1) Check inverter (1) 2D-10.
		(2) Check Read Head Power Supply.
		C. Run indicator on - others off.
		(1) Check inverter (1) 2D-4.
		(2) Check control panel circuitry.
		D. Page Feeder Motor on - others off.
		(1) Check NAND Gate (1) U23-6.
		(2) Check transistor circuitry on control panel.
		(3) Check for seized Page Feeder relay in Page Feeder.

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Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOMS	ACTION/REMEDY
I	Feed Indicator is on	Check Instruction Decoder (1) 19T-3.
J	Paper Gate is pushed down	A. Check Inverter (1) 14R-6. B. Check Control Flop (1) 10L-8. C. Check transistor circuitry on control panel.
K	Paper Handler Rollers not stopped	A. Turn slowly - adjust Vertical Drift Pot to stop rollers. B. Turn fast - (1) Faulty Vertical Servo Amp. (2) Faulty Servo Controller. (3) Faulty Instruction Decoder.
L	Margins do not adjust properly	A. No margin values (1) Check two cables to core memory and all cables on cards in Card Cage. (2) Check that all cards are properly seated (with power off). B. All margins have same value and change if any one is changed. Cable on core memory upside down.

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOMS	ACTION/REMEDY
M	Read Head Lamp, Run Indicator, and Page Feeder Motor not all on	A. All three off (1) Check Control Flop (1) 2C-6. (2) Run Communications Diagnostic (see Test Set Manual). B. Read Head Lamp off, others on - check DS1. (1) DS1 off (a) Check inverter output (1) 2D-10. (b) Check Read Head Lamp Power Supply. (2) DS1 on - check for voltage on lamp leads. (a) No voltage - bad Read Head Flex cable or wiring. (b) Voltage OK - bad bulb. C. Motor off - others on (1) Check inverter (1) U23-6. (2) Check for open relay coil or open contacts. (3) Check transistor drive circuitry on control panel.

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Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOMS	ACTION/REMEDY
		D. Run indicator off - others on (1) Check inverter (1) 2D-4. (2) Check control panel circuitry.
N.	Page Feeding Belts moving whenever motor is on	Check transistor drive circuitry for brake on and clutch off.
P	Read Head A. Does not drive left. B. Drives left and does not stop at photocell. Drives against physical stop. WARNING: Troubleshoot with Servo Fuses pulled.	A. No drive left (1) All further operations cease - faulty Servo Controller. (2) This step bypassed - faulty left stop photocell circuit. (3) Mechanical bind in horizontal section. (4) Perform Mechanical Diagnostic. B. Does not stop at left photocell (1) Faulty photocell circuit. (2) Faulty Executive Macro test gate.

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOMS	ACTION/REMEDY
R	Read Head A. Does not drive right. B. Does not stop at center.	A. Does not drive right (1) Faulty right stop photocell. (2) Faulty Servo Controller. B. Does not stop at center (1) Faulty Horizontal Encoder output. (2) Faulty Horizontal UP/DN Pulse Generator. (3) Faulty Horizontal Position Counter. (4) Faulty Horizontal Adder. (5) Faulty LT/RT margin Test Gate.
S	No Feed Indicator and/or Page Feeding Belts are not driven.	A. No Indicator and no belt movement - check Feed Decoder (1) 19T-3. B. No Indicator, belts move - check control panel indicator and circuitry. C. No belt movement, Indicator lit (1) Check brake and clutch control voltages. (2) Check for mechanical bind.

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOMS	ACTION/REMEDY
T	Paper Gate A. Is not pushed down. B. Returns back up almost immediately.	A. Gate not pushed down (1) Return spring tension too great. (2) Faulty control voltages from control panel. (3) Open coil. (4) Faulty Decoder (1) 10L-8. B. Returns up (1) Micro Switch stuck. (2) Micro Switch stuck closed. (3) Faulty Executive Macro Test Gate.
U	Paper Handler Rollers A. Do not turn. B. Turn wrong way.	A. Do not turn (1) Faulty Vertical Position Mode Decoder (1) 20T-2. (2) Faulty Position Mode Circuitry. B. Turn wrong way - faulty Position Mode Circuitry.

Table 6-3

Troubleshooting with the Sequence of Events Flow Chart (continued)

FIG. 6-1	SYMPTOMS	ACTION/REMEDY
V	A. Paper does not reach gate. B. Gate never rises.	A. Does not reach gate (1) Check for blockage (2) Double page kickers pushing all pages back. B. Never rises - faulty Micro Switch or wiring
W	Several pages shoot through, Read Head never moves.	Paper present never detected A. Faulty circuitry. B. Faulty Flex cable. C. Faulty Executive Macro Test Gate.
X	Page does not stop at top margin.	A. Page shoots through, Read Head hangs up at left stop - faulty Vertical Servo Position Mode Circuitry. B. Page shoots through, Read Head tries to scan the moving page (1) Faulty Encoder output. (2) Faulty Vertical UP Pulse Generator.
Y	Read Head does not start scanning after paper stops.	Faulty Paper in Position Flop or Test Gate.

6-7. PROCEDURE FOR TROUBLESHOOTING MISRECOGNIZED CHARACTERS. - In order to utilize the procedures contained in this section, the Order of Events serve as a prerequisite. The Servo Control Circuitry must be working accordingly (refer to paragraph 6-1). If the ALPHA misrecognizes, use the Recognition Flow Chart, Figure 6-2 and Table 6-2 in conjunction with the following procedures to determine the cause of the malfunctions.

a. Procedure to Continuously Scan a Line of Text. -

(1) Disable SRECO via the Test Set.

(2) Disable the Vertical Servo Control by grounding the output of the Vertical Servo Pre-Amp, 30A-10 (Figure A-l, 2-Stage Amplifier).

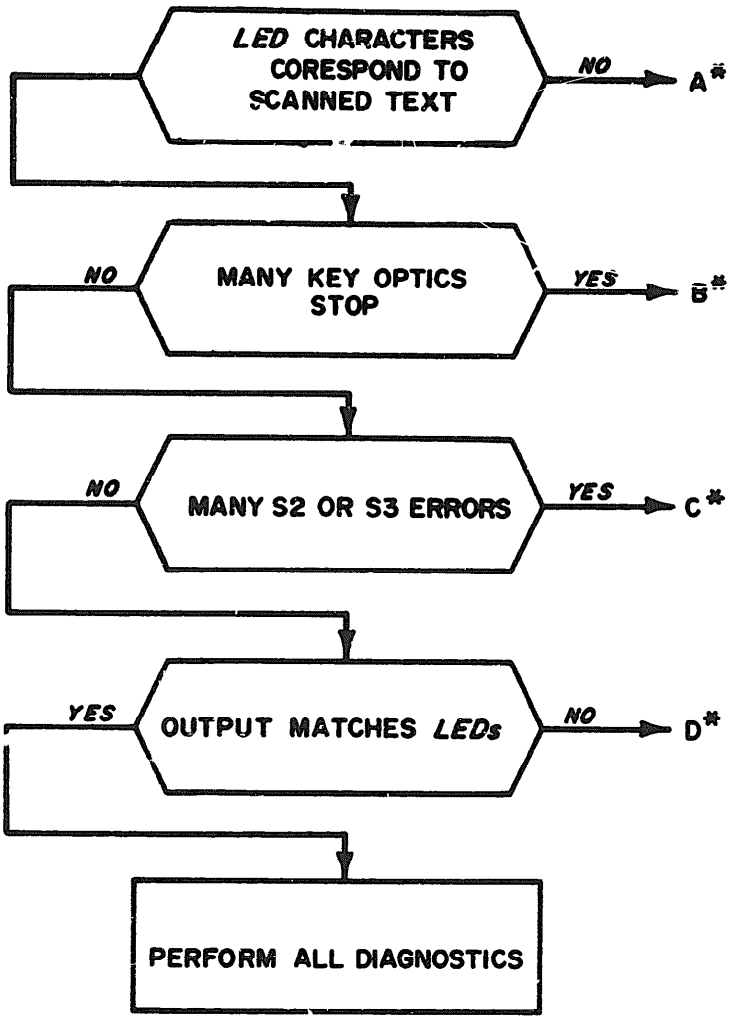
(3) Position a line of text (use the same character repeated at least 60 times on the line) under the Read Head.

(4) Press "START"; the Read Head will drive left and then right and position itself at the center of the carriage.

(5) Ground "Tpp" at connector P40, pin 32 (Figure A-31) for about a second; when ground is taken off, the Read Head should continuously scan the same line 128 times and then stop. At this point, ground "Tpp" again to get scanning started. This step may be repeated as desired.

(6) To slow down the speed of the Read Head for ease in scoping signals, place a resistor in parallel with the gain resistor (across pins 56 and 57) on the second stage of the horizontal Pre-Amp (30A). WARNING: A resistor of 1K or greater must be used or damage can result. By decreasing the value

*CAUTION: Exercise extreme caution when performing these procedures. (Use only when necessary.)



* Refer to Table 6-4

Figure 6-2. - Recognition Flow Chart

Table 6-4

Troubleshooting with Recognition Flow Chart

REF. FIG. 6-2	SYMPTOM	ACTION/REMEDY
A	LED characters do not match scanned copy	(1) Faulty Character Identification Circuitry Run Scan and Recognition Diagnostics. (2) Faulty LEDs - Run LED Diagnostics.
B	Many Copy Optics stops	(1) Check copy quality. (2) Check Read Head alignment. (3) Run Scan and Recognition Diagnostics.
C	Many S2 or S3 errors	(1) Disable SRECO with text box and if problems go away, SRECO Board is faulty. (2) Run Scan and Recognition Diagnostics.
D	Output faulty	(1) Reload header sheets. (2) Run Diagnostics including Memory Diagnostic. Caution: Reload header sheets after running Memory Diagnostics

of the gain resistor, the velocity of the Read Head is proportionally decreased.

b. Procedure to Scope "BID" ASCII Code for the Character Being Scanned. -

(1) Turn Key Optics OFF.

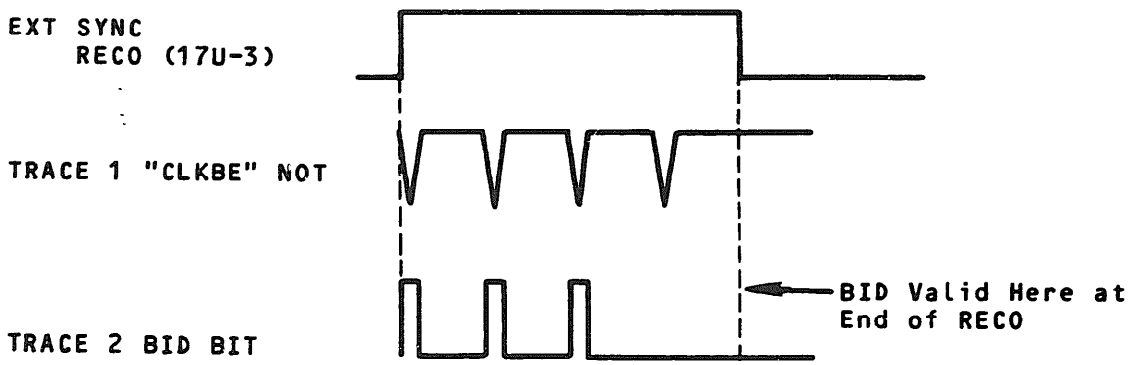
(2) Disable Early Abort by grounding 1X-13 (Figure A-14).

(3) Externally synchronize scope on RECO (17U-3, Figure A-11). Trigger on the positive slope.

(4) Scope out with trace 1 CLKBE(not) (8X-11, Figure A-14).

(5) Scope out with trace 2 the BID latches (4X and 5X, Figure A-14), BID bits 0-7, utilizing the accompanying timing diagram.

NOTE: The BID bits are valid at the training edge of RECO. If the "BID" ASCII code does not correlate with the scanned character, resort to Procedure "C". If "BID" is correct, the problem probably lies within the Line or Flag Buffer, or the core memory and related control circuitry (Memory and Output Control Circuitry), the Output Data Latch, or the Executive Macro's data paths.



c. Procedure to Troubleshoot Incorrect "BID" Bits. -

(1) Externally synchronize on RECO (17U-3, Figure Trigger scope on the positive slope.

(2) With trace 1 scope SHIFT XYSR(not) (31S-3, Figure A-12).

(3) With trace 2 scope the output of the X Shift Register (29Z-9, Figure A-12).

(4) The same procedure can be undertaken in scoping the Reference Characters by moving trace 2 to the output of the Y Shift Register (29Z-5, Figure A-12).

If the characters appear correct at the outputs of the X and Y Shift Registers, check the following as a possible cause for misrecognition:

(1) Character Parameter Memory (Figure A-7).

(2) Error Generators and Latches (Figures A-7 and A-13).

(3) Related Evaluation Circuitry (Figure A-14).

If the characters appear incorrect on the output of either Shift Register, further diagnosing will reveal whether or not the character has been successfully loaded into the Shift Registers. Restore to Procedure D.

d. Procedure to Troubleshoot Incorrect Characters at the Output of Either the X or Y Shift Register. - By monitoring LOADXYSR(not) (23T-6, Figure A-12) during recognition, each horizontal plane can be diagnosed as it is loaded into either Shift Register. It is obvious at this point that if the character is being loaded into the Shift Register correctly and

the output is incorrect, the problem lies within the Shift Register. If the unknown character appears incorrect at the input to the X Shift Register, the problem lies somewhere in the URAM or other front end circuitry. If this is the case, the following procedure will diagnose the URAM.

(1) Externally synchronize on "Just" (8U-5, Figure A-6).

(2) With trace 1, scope "Write Enable" (25N-2, Figure A-6).

(3) With Trace 2, scope the 24 inputs to the URAM (Figure A-6) during "Write Enable" time. This will determine if the URAM is being loaded properly,

If the character appears to be correct on the input to the URAM, then the malfunction is within the URAM. If the character appears incorrect at the input to the URAM, the problem is in the front end circuitry, video acquisition, or video processing.

Procedure to Troubleshoot the MMatrix Assembler (SR2). -

(1) Ground 15N-9 (Figure A-6) to force all ones in SR2; or Ground 25N-8 (Figure A-6) to force all zeroes in SR2.

(2) Externally synchronize on sample (10S-3). Trigger on the positive slope.

(3) With trace 1, scope "SCCLK" (1T-9, Figure A-6).

(4) With trace 2, scope the most significant stage of SR2 (Figure A-6). Either all ones or zeroes should be observed depending on Step 1.

If the data appears correct in SR2, it is obvious that SR2 is functioning correctly. The problem now has been narrowed

down to the Read Head Analog and Digital Circuits or the Matrix Analysis Circuits.

Refer to the Read Head alignment procedures contained in Chapter 5 for preventive maintenance in case Read Head is suspended. Refer to diagnostic program if the Matrix Analysis Circuit 5 are suspect.

If the data appears incorrect at the output of SR2, it is obvious that one or more of the 24 stages is incorrect.

6-8. PROGRAMMED OR AUTOMATIC TESTS. - Refer to the Programming Manual for all programmed, automatic, and other self-tests.

6-9. MAJOR PARTS REPLACEMENT. - Many of the parts that can be replaced are located on the interior of the paper handling assembly The procedures in paragraphs 6-9b through 6-9r describe in detail the removal and replacement of specific parts. Most of these procedures can be accomplished with the standard tools found in any repair shop. If a special tool or fixture is required, refer to Table 6-2 for specific information concerning the tool. In order to correctly remove and/or replace the parts described, the sequence provided must be strictly adhered to.

If the Control Console is raised until travel is stopped, it will not be possible to lower the upper platen. To access these parts, the upper platen must be released from the Console Assembly cover. Proceed as follows to remove or replace parts.

a. Access to Paper Handling Assembly. -

(1) Loosen the Page Feeder retaining screw (Figure A-34) and carefully pull the unit forward and off the cabinet.

(2) Loosen the two hand sc (Figure A-34) fastening the Control Console Assembly to the Lower cabinet base.

(3) Slowly tilt back the Control Console Assembly, (16, Figure A-41) until its travel is stopped (approximately 60 degree angle with the lower platen).

(4) Remove the two 1/4-20 socket head cap screws (3, Figure A-41), washers, lockwashers, and shims (if any) fastening the upper platen (4) to the Control Console cover (5). (Do not lose the washers of shims.)

(5) Separate the top cower from the upper platen by slowly moving the upper platen down. The cover will go back until it is stopped by the two brace bars.

(6) Firmly grasp the upper platen and push it down until it butts with the lower platen (6). DO NOT RELEASE FIRM PRESSURE.

(7) Engage the two hooks (7) on the lower platen with the small protruding studs (8) on the upper platen. Tighten the hooks in place with the pivoting screws. RELEASE PRESSURE on upper platen.

(8) After the replacement part is installed, apply a firm downward pressure on the upper platen while releasing the two restraining hooks.

CAUTION. - It is imperative to maintain a firm grasp on the upper platen when releasing it. This restraining action will prevent physical damage to the machine through platen overtravel caused by unrestrained spring tension.

(9) Allow the upper platen to move upward while maintaining downward pressure until it reaches the point where the springs stop further movement.

(10) Move the upper platen and console cover together until the tab (5) on the mirror and hole in the platen line up. Replace and tighten the 1/4-20 socket head cap screws (3) (with washer, lockwasher, and shims, if any).

(11) Slowly lower the Control Console Assembly to the cabinet and fasten in place with two knurled screws.

Note:- When the console cower is closed, two small studs (9) on the lower platen (6) align and close with washers (10) in the upper platen,

b. Read Head Assembly. - To remove the Read Head, proceed

(1) Access the upper assemblies as described in paragraph 6-9a, steps 1 through 7.

(2) Remove grill by removing the four round head screws that secure the grill in front of the Read Head.

(3) Remove front mirror by removing the four socket screws holding the front mirror brace,

(4) Remove the two wires connected to the Read Head lamp by gently pulling on connectors from the lamp. The connectors are banana plugs and may take some prying. Be careful as the lamp could be broken.

(5) Remove screw securing ribbon cable to Read Head and carefully disconnect cable from the board by prying up the COnneector.

(6) Loosen set screw (on front) (do not remove).

(7) Loosen the two thumb screws.

(8) Rotate the Read Head Assembly very slightly, pull up and remowe.

(9) Reverse the procedure to reassemble. If any adjustments have been affected, perform Read Head alignment.

c. Read Head Lamp. - To change the Read Head lamp, access the upper assembly as described in paragraph 6-9, steps 1 through 7.

(1) Pull wires off lamps.

(2) Remove the three round head screws and associated hardware that secure the lamp retaining ring.

(3) Lift the retaining ring over the lamp and remove the Camp.

(4) Insert new lamp exactly as original lamp was.

(5) Reverse procedure to reinstall. Be certain retaining ring is reinstalled as close to where it originally was,

(6) Check lamp voltage and set at about 17 volts,

(7) Check video at TP-2 on Read Head Analog Board. Lamp may have to be moved to get flat video wave on scope,

d. Removing Read Head Analog Card.- To remove the Read Head Analog Card, follow the procedures for removal of

the Read Head given in paragraph 6-9b. Refer to Figure 7-20, sheet 4. Numbers in parentheses are item numbers on this figure.

(1) Remove the screw (113) between US and C12 on top of the card.

(2) Remove the screw (113) located to the right of C23.

(3) Remove the screw (113) on the left side of the board near C4.

(4) Remove the screws (115) located at each end of U4.

(5) Carefully lift the board up,

(6) To reassemble, reverse the above procedure. Perform Read Head alignment.

e. Horizontal Drive Cables. - To remove and restring the horizontal drive cables, perform the following. Refer to figure 7-20, sheet 8. Numbers in parentheses are item numbers on this figure.

(1) Access the upper assemblies as described in paragraph 6-9a, steps 1 through 7.

(2) Remove the drive cables by loosening the hex nut (127) on the left side, located at lower left corner of fan. When removing the nut, make sure that the square fitting on the end of the cable is held firmly with pliers to prevent the cable from being twisted while the nut is being removed.

(3) Unstring and remove cable from the drum (305).

(4) Remove nut (127) from end of Cable Assembly (173) on right side and remove cable from drum,

(5) Remove spring (126) and spring housing (128) from cable.

(6) To string new cables, place Read Head carriage near left side.

(7) Insert ball end of first cable into drum (305) slot and loop around in counterclockwise direct ion 1/2 turn in rearmost groove of drum (see Figure 6-3).

(8) String cable over and under the right pulley (243).

(9) Bring over to and around counterclockwise the lower groove of the Read Head carriage pulley (250).

(10) Insert end of second cable through hole in right side of plate and take up on tension by pulling to move Read Head carriage to right limit.

(11) Place spring and spring housing over cable, then thread nut onto screw only to depth of nut,

(12) Move main drive drum clockwise to take up all slack in cable. Ensure that spring is centered in the hole.

(13) Insert ball end of other cable into drum slot and loop around clockwise.

(14) String cable over and under the left pulley (245).

(15) Bring over and loop around clockwise the upper groove of the Read Head carriage pulley.

(16) Maintaining tension with pliers on cable screw, insert screw end of cable through hole on left side and secure with nut. Tighten to depth of nut, ensuring that cable does not twist.

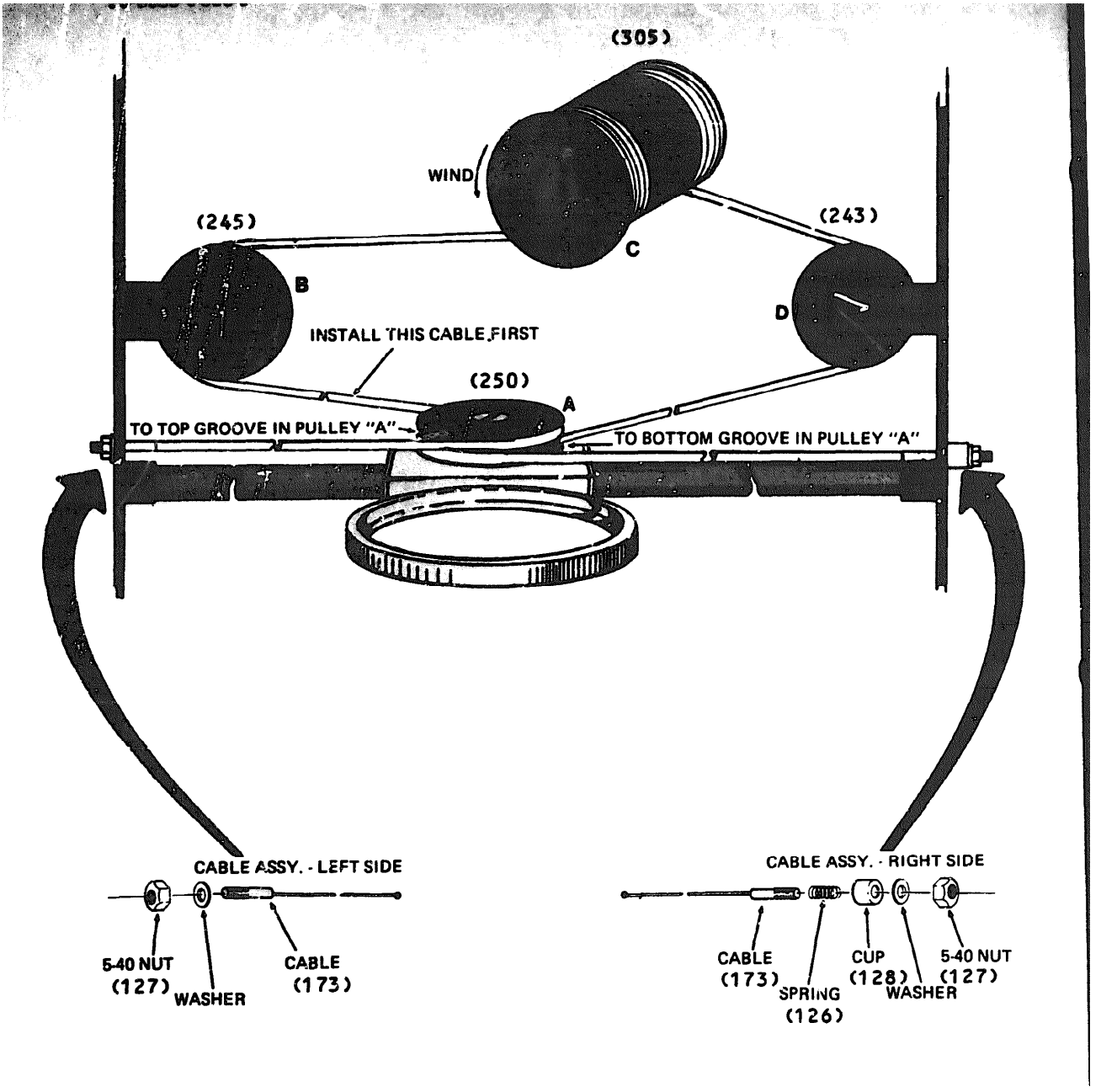


Figure 6-3. - Read Head Cable Drive Diagram

(17) Turn drum (305) by hand to move the Read Head carriage to the right and left stop, checking for smooth operation.

(18) Replace mirrors and grill.

f. Linear Ball Bearings. - To install new linear ball bearings into the carriage housing (188A), perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Follow procedures for access to the upper assemblies as described in paragraph 6-9a.

(2) Remove Read Head as described in paragraph 6-9b.

(3) Remove the horizontal drive cables as described in paragraph 6-9e.

(4) Loosen the cap screws on both roller lifting mechanisms and the set screw in the two collars (19) on the rear carriage rail (211); slide the rail out to either side. Now the carriage may be removed.

(5) Remove the two flat head screws (206) that mount the retainer plates (205) on both sides of the linear bearing bore.

(6) Note how the seals are positioned, because when new seals are installed, they must be installed into the bore in the identical position as the old seals.

(7) Locate the end of the carriage linear bearing bore over a larger than 5/8" diameter hole and use a 5/8" diameter tool that has a 3/8" diameter pilot to slowly press

out the bottom seal, but do not push all the way through. When the bottom seal has been released, turn the carriage upside down and press from the other side to remove the other seal. After removal of seals, the bearings and the spacer will slide freely out of the bore.

(8) Install new bearings and new seals by reversing the procedure described in step 7.

(9) To reassembly, reverse the procedure described in steps 1 through 5.

g. Flexible Cable. - To remove the flexible cable from the Read Head Lamp Assembly, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure. Also access assembly as in paragraph 6-9a.

(1) Remove leads from Read Lamp.

(2) Remove screw (228) to release the flexible cable from the Analog Read Head Board (Figure 7-22-1). Now pry connector up from pins on the Analog Board.

(3) Pull out P102 from connector. Remove three screws from the side plate (261), and the cable will now be free for removal by separating it from the velcro strip.

(4) To reassemble the flexible cable, reverse the procedure described in steps 1, 2, and 3.

h. Upper Rollers. - To remove or replace upper rollers, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure,

(1) Access the upper assemblies as described in paragraph 6-9a.

(2) Remove roller lifting mechanism (256) on both sides of system.

(3) Remove page hopper from back of the system.

(4) Remove the two screws that are holding the static eliminator. These screws are number 8, and you will need a 9/64 Allen wrench. These screws also lock into the back of the upper platen.

(5) Remove the three screws from bottom side of lower platen into vertical side of the fan.

(6) Loosen the three screws on the other side of the lower platen into the vertical side. These six screws are number 6 Allens. Use a 7/64 Allen wrench.

(7) You should now be able to remove the upper rollers.

(8) To remove the upper platen itself, you will have to first remove the two photo detectors mounted on top of the lower platen.

(9) Now remove the screw loosened in step 6.

(10) To reassemble put the six screws in the side plates in loosely.

(11) Insert the two screws removed in step 4 and screw them in tightly.

(12) Tighten the six screws from step IO.

(13) Replace roller lifters removed in step 2, photo detectors removed in step 8.

i. Lower Rollers and Platen. - Remove the lower rollers and platen in the following manner. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Raise upper assembly as described in paragraph 6-9a.

(2) Remove time belt (92) by loosening four cap screws and washers (86 and 87).

(3) Remove four socket head cap screws and remove the Lower Platen Assembly. There are two centering pins on each side. You may have to tap the platen from below with a small mallet.

Note:- The rollers and lower platen are replaced as one unit. This is because of gears having to be pinned to the roller shaft. This has to be done in the factory.

(4) Remove the guide pins either by pulling out or knocking into the frame. They will not be needed.

(5) Place the new lower platen in place and put in four socket screws removed in step 3. Make these snug but not tight.

(6) Bring down the upper platen slowly and lock it down. The guide pins in the lower platen wilt now fit into the guide holes of the upper platen and thereby align itself.

(7) Raise the upper platen.

(8) Now lock down tightly the four screws in the lower platen.

(9) Put timing belt back on gear. Push down on the lower pulley and tighten the four cap screws.

j. Torque Spring. - To replace torque springs between the upper and lower halves of the Paper Handler, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Remove the shoulder screw (346) and sleeve bearing (347A).

(2) Release tension springs (350) with the winding tool.

(3) Remove the pan head screw and washer (351 and 352).

CAUTION, - When winding or unwinding torque springs be extremely careful. If the springs are released, they may injure anyone close by.

(4) To reassemble, reverse the procedure described in steps 1 and 2.

k. Vertical Drive Encoder. - To exchange the paper drive encoder, perform the following. Refer to Figure 7-20.

(1) Note location of wires on TB105, then remove the five leads from encoder from TB105.

(2) Remove Encoder Assembly from Paper Handler base by removal of four screws and washers (66, 67, and 68).

(3) Take the anti-backlash gear clamp and mounting plate off the old encoder and install all of these on the new

encoder. Be sure to align the anti--backlash gear with the drive gear.

(4) To reassemble the Encoder Assembly onto the Paper Handler, reverse the procedure described in steps 1 and 2. Be sure that the anti-backlash gear is offset by two teeth prior to being mated with the pinion on the Lower Platen Assembly.

l. Vertical Drive Servo Motor. - To replace the Vertical Drive Servo Motor perform the following. Refer to Figure 7-20.

(1) Remove the output hopper.

(2) Remove the t o screws holding in the hopper support.

(3) Lift out the paper tray. W e now have access to the Servo Motor in the rear right.

(4) Remove the motor leads from top of TB-5. Make note of which color and size go to which pin.

(5) Remove the two screws (78) that mount the Servo Motor to bracket on the side wall. Take care to lift out the belt.

(6) Remove the pulley from the Servo Motor and install it on the new motor. Pin it in the proper position.

(7) Remove the mounting bracket from the old motor (four screws, item 71), and install it on the new motor.

(8) Reassemble by reversing steps 1 through 5.

Note:- Make sure to put the drive belt back on.

m. Horizontal Drive Assembly. - To remove the entire Horizontal Drive Assembly, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Remove the drive cables as described in paragraph 6-9e.

(2) Remove all wires connected to the horizontal encoder by removing the five flat head screws on the terminal board (323) TB104. Note the location of the wires.

(3) Remove the three wires connected to the rear of the horizontal servo.

(4) Remove the paper hopper (Figure 7-2, item 68).

(5) Remove the four socket head cap screws (293) on the underside of the lower platen,

(6) Remove the entire assembly.

(7) To replace, reverse the procedure described in steps 1 through 6.

n. Horizontal Drive Encoder- - To replace the encoder, perform the following, Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Remove wires of the horizontal encoder at TB104. Note the terminals the different colors come off of.

(2) Release two set screws (297) on the flexible coupling (296), remove four screws (321) which hold encoder support to the base, and slide encoder support with encoder out of the flex coupling, Note if there are any shims under the encoder bracket.

(3) Remove four screws on encoder to release the encoder from the braket.

(4) Install new encoder on the support bracket. Make sure it is centered on the center hole of the bracket.

(5) To reassemble, place the encoder mounting bracket in position and align the shaft of the encoder with the bore of the coupling. The shaft and bore must be aligned axially so the encoder bearings are not forced to take excessive radial forces.

o. Horizontal Drive Servo Motor. - To remove the Servo Motor, follow the procedure as given below. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Remove the white, black, and red wires that go from the rear of the Servo Motor to TB106 (116). Note the position of the wires on TB106.

(2) Remove the two socket cap head screws (309) that hold the servo L-bracket to the assembly base plate, This will release tension on the belt, Remove the belt.

(3) Remove the four socket head cap screws (299) that mount the servo to the bracket.

(4) To reassemble reverse the procedure described in steps 1 through 3.

p. Drum, Pulley, Bearings, and Shaft. - To replace these items on the Carriage Drive Assembly, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Remove drive cables as described in paragraph 6-9e. Remove the belt and encoder per paragraph 6-9n.

(2) Remove t o spiral pins (191). This will separate the drum and pulley from the shaft.

(3) Each part in the assembly may now be replaced.

(4) To reassemble, reverse the procedure described in steps 1 and 2. Pin the drum and/or pulley to the shaft selecting a radial spot other than the existing holes.

q. Timing Belt. - To change the timing belt on the Carriage Drive Assembly, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Loosen two screws (309) to release tension on the belt.

(2) Please set screw in flexible coupling (297).

(3) Remove four screws (321).

(4) Slide the Encoder Assembly back to provide clearance for the timing belt to pass through.

(5) Note if there are any shims under the encoder bracket; reinstall during reassembly.

(6) To reassemble, align the encoder shaft; then reverse the procedure described in steps through 5, being sure to replace and tighten the screws in step 3 before performing step 2.

Note:- Do not overtighten the timing belt during reassembly - timing belts do not require excessive tension to transmit motion.

r. Carriage Travel End Detectors (Left and Right Limit Switches). - To change the Carriage Travel End Detector, perform the following. Refer to Figure 7-20. Numbers in parentheses are item numbers on this figure.

(1) Remove two screws (149) that hold detector bracket (148) to platen.

(2) Remove Lugs from either TB108 (119) for left limit switch or TB109 (122) for right limit switch, noting which color ire goes to which pin.

(3) Install new Detector on bracket.

(4) Install new Detector Assembly, reversing the procedure given in steps 1 and 2.

(5) Check that when the carriage is pushed past the End Detector the shutter passes through the slot and does not touch the Detector at both locations; if necessary, readjust the shutter to achieve this free condition.

S. Vertical Servo Amplifier. -

(1) Remove paper hopper from the rear.

(2) Remove the hopper support by taking out the two screws.

(3) Remove the paper tray (blank cover).

(4) The Vertical Servo Amplifier mounted on the left side can be taken out by removing the four screws (16), one from each corner.

(5) Pull the Amplifier Assembly straight out as it has an octal tube-type connector.

(6) To replace, reverse steps 1 through 5.

t. Any Board in Power Supply. -

(1) Disconnect AC power plug to wall outlet

(2) Lift off front bottom panel.

(3) Open front door.

(4) Remove the cover of the power supply by removing the seven screws on top of it.

(5) Remove the wires and screws holding in the board now being changed.

(6) To reassemble, reverse steps 1 through 5.

u. Horizontal Servo Amplifier. -

(1) Follow procedure to access the Upper Assembly as described in Paragraph 6-9a.

(2) Remove the four screws (111B) and washers (111C) from its corners.

(3) Pull up on Servo Amplifier, as the connector is an octal tube socket. It is keyed.

(4) To replace, reverse steps 2 and 3.

v. Control Panel. - Refer to Figure 7-14. Numbers in parentheses are item numbers on this figure.

(1) Release the two knurled head screws and raise the Control Console,

(2) Remove the ribbon cables on both ends of the board.

(3) Remove the twisted ire connector to the center of the board.

(4) Remove the two screws (9) that hold the speaker (1) in place on two standoffs (12).

(5) Remove the large standoff S.

(6) The board should now drop out.

(7) To reassemble, place the board in position and reverse steps 2 through 5.

6-10. PAGE FEEDER. - To remove the cover of the Page Feeder remove the four screws in the rear bottom of the cover and four screws in the bottom corners. The cover can now be lifted up. The following paragraphs outline the procedure to be followed for replacement of parts. Refer to Figure 7-13. The numbers in parentheses are item numbers on this figure.

a. Brake and Clutch Assembly. - To remove the Brake and Clutch Assembly, perform the following.

(1) Disconnect the plastic connector (188).

(2) Remove the two belts between the large pulley and the motor pulley.

(3) Remove the two long belts from the lower pulley on the Brake and Clutch Assembly to the rear pulley of the Page Feeder.

(4) Remove the three screws (182) which pass through the left side plate into the back of the Brake and Clutch Assembly.

(5) To reinstall, reverse the procedure described in steps 1 through 4.

b. Bearings, Clutch, and Pulley Assembly. - To replace bearings in the Clutch and Pulley Assembly, do the following. Refer to Figure 7-13.

(1) Remove Clutch and Brake Assembly as described in paragraph 6-10a, steps 1 through 4.

(2) Remove the two pulleys on the outside of the brackets (front plate) by loosening the set screws.

(3) Remove the four screws that hold the left hand bracket (front plate) in place.

(4) Remove spacer on clutch shaft.

(5) Gently pry bracket off the shafts. Bearings will come up with bracket.

(6) Remove belts from pulleys.

(7) Remove nylon washer from clutch shaft.

(8) Remove pulley and clutch.

(9) Remove snap ring from brake pulley.

(10) Remove shim from brake shafts.

(11) Remove brake pulley and belts together.

(12) Pull idler pulley and shaft out (has nylon washers on each end).

(13) Remove "E" ring from clutch and nylon washer.

(14) Loosen screws on collar.

(15) Pull shaft through,

(16) Press bearing out.

(17) Note if bracket, bearing support on the end of clutch coil is removed, then alignment has to be set.

(18) To reassemble the clutch and pulley, reverse the steps of 2 through 16. hen mounting the clutch pulley on the outside of the side bracket, push it in snugly, then lock it. If it is too loose you will get a noise from the Clutch Assembly.

c. Bearings, Brake Pulley Assembly. - To replace bearings in the Brake and Pulley Assembly (Figure 7-13) perform the following.

(1) Remove the two belts between the large pulley and the motor pulley.

(2) Remove the t o long belts from the lower pulley on the Brake and Clutch Assembly to the rear pulley of the Page Feeder.

(3) Remove the two pulleys on the outside of the bracket.

(4) Remove the four screws that hold the left hand bracket in place.

(5) Remove spacer on clutch shaft.

(6) Gently pry out bracket off the shafts. Bearings will come off with the bracket.

(7) Slide belts off of clutch pulley.

(8) Slide brake pulley off of shaft.

(9) Bearings are in pulley.

(10) To reassemble, reverse steps 1 through 8. When mounting the clutch pulley on the outside of the side bracket, push it in snugly, then lock it in. If it is too loose you will get a noise from the Clutch Assembly.

d. "O" Rings and Drive Belts. - To replace these items, remove the front plate as described in 6-10b, 2 through 6, then

install new "O" rings or belts as required. Reverse the procedure to reassemble.

e. Clutch Bearing Support. - To replace the bearing in the Clutch Bearing Support (Figure 7-13, item 210) perform the following.

(1) Remove the four nuts (214), lock washers (213), and flat washers (212) from the Bearing Support.

f. Electromagnet. - To replace the electromagnet portion of the Clutch and Pulley Assembly, do the following. Refer to Figure 7-13.

(1) Remove Clutch and Brake Assembly as described in 6-10a, 1 through 4.

(2) Remove front plate pulleys and clutch as described in 6-10b, 2 through 8.

(3) Remove four nuts (214) and lock washers (213), Clutch Bearing Support (210), and four screws (211).

(4) Unsolder leads (red) from bottom terminal strip.

(5) Install new electromagnet portion of the Clutch and Pulley Subassembly using four screws, and Clutch Bearing Support (210).

(6) Insert clutch alignment tool pin 101907, add washer and lock washer, tighten nuts, and then remove aligning tool.

(7) Solder on new leads to terminal strip.

(8) To reassemble, reverse the steps of 6-10b, 2 through 8.

(9) To remount hole assembly, reverse steps taken in 6-1Oa, 1 through 4.

g. Blower Assembly. - The following procedure is used to remove the Blower Assembly.

(1) Remove the wires from the Blower Assembly by pulling off the push-on terminals from the clips on the motor coil.

(2) Remove the top two screws (173D) on the blower bracket support (Figure 7-13, item 84).

(3) On the right side of the Blower Assembly, remove the two vertical screws (109), nuts (112), and washers (110 and 111) that are holding the blower down. When the screws come out, there is a metal guide support plate (108) that is now lying loose on the Blower Assembly. Remove it and save to reinstall.

(4) You can now lift the Blower Assembly straight up.

(5) To reassemble onto feeder, reverse steps 1 through 5 above.

h. Paper Drive Belts. - To replace the six paper drive belts, perform the following. Refer to Figure 7-13. Numbers in parentheses are item numbers on this figure.

(1) Remove the Blower Assembly as described in paragraph 6-10g.

(2) Scribe a thin line down the left side of the belt shaft support plate (115) located on the right side of the feeder. This is done to make it easier to properly realign the support plate during the reassembly.

(3) Remove the two long belts (30) from the pulleys.

(4) Remove the lower plastic gear (26).

(5) Remove the two belts between the kicker shaft pulley and the pulley on the shaft from which we just removed the plastic gear (item 4 above).

(6) Remove the pulley from the shaft that the plastic gear as taken off of (item 4 above). Also remove all washers from shaft.

(7) Remove "E" ring from outside of left side plate on the front shaft-

(8) Remove two number 8-32 x 1/4 screws (116). Then, while holding the t o shaft supports (against the tension of the belts), carefully remove the support plate. The two shafts must be held apart in order not to damage the bearings in the side plate; if this is not done then the bearings may be damaged due to excessive axial twist applied by the belt tension, It is recommended that a set of spacers be made to eliminate the problem of having to hold the shafts manually apart.

(9) Remove and replace the paper drive belts.

(10) To reassemble the shafts and belts, install the support plate (115) onto the two shafts and line up the edge of the support plate with the scribed line while the screws (116) are being tightened.

(11) Reverse steps 3-7 above and step 1 above.

i. Stripper Pulley (Kickers) "O" Rings. - To service the "O" rings of the stripper pulley on the Stripper Shaft Assembly perform the following. Refer to Figure 7-13. Numbers in parentheses are item numbers on this figure.

(1) Remove Blower Assembly per step 6-10g.

(2) Remove the two long belts from the pulleys.

(3) Remove the lower plastic gear (done for convenience).

(4) Remove the two belts between the stripper pulley and the pulley behind the lower gear.

(5) Remove the pulley on the stripper shaft.

(6) Loosen the set screws in both strippers (kickers) and the cam spacer, so that they rotate freely.

(7) Remove the “E” ring located on the stripper shaft, just inside the left side plate.

(8) Carefully pull the shaft out the left side of the Page Feeder, sliding the cams and spacer off the shaft as it is removed. Be careful not to flex the shaft as any axial twist in the shaft motion can damage the bearing, thereby causing the stripper to malfunction.

(9) Retrieve strippers and replace the “O” ring on the cams.

(10) To reassemble reverse steps 1 through 8.

(11) Note, when locking the strippers in place (step 6 above) the cams must be aligned with the belts and the cams must be aligned with each other. (The cams are both high or low at the same time.)

Note: - Removal of the stripper shaft may be avoided if one is able to shift the "O" rings (137) on the pulleys (135) so that the section of the "O" ring that rests on the roll pins is shifted to a position in between the pins.

Front Idler Roller and Pressure Roller Drive. - To replace the front idler roller and pressure roller drive,, perform the following. Refer to Figure 7-13. Numbers inparentheses are item numbers on this figure.

(1) Remove two number 8-32 screws and remove shaft (140).

(2) Remove four number 8-32 screws (247), remove two number 6-32 screws from Paper Stop Assembly (246), remove two number 4-40 screws from align support (50) remove screws and stand-off, remove two number 4-40 screws from upper paper spacer (36) and remove one number 8-32 screw. Now disengage springs from solenoid. Remove epoxy from between right side plate (127) and upper paper spacer (36) and then remove the right side plate (127). Remove retaining (E) ring from roller drive (32), remove spacers and retainers and remove roller shaft.

(3) To reassemble, reverse the procedure described in steps 1 and 2, using a jig to align the roller and pressure shaft:,

k. Double Page Detector. - To remove the Photo Paper detector, perform the following. Refer to Figure 7-13. Numbers in parentheses are item numbers on this figure.

(1) Remove the epoxy from both the IR detector and the IR source.

(2) Remove the bottom mounting plate (290A) by removing the six number 8-32 screws (290B). Remove the exit alignment plate (3) by removing four number 8-32 screws (4).

(3) Disconnect leads from terminal board on right side.

(4) Install new emitter and detector. Tighten detector onto the mounting plate. Leave the emitter Loose.

(5) Replace the Page Feeder in the machine. This will have to be done with care as the base plate is off. Boxes might have to be put under feeder so connector can be plugged in. Be careful as voltage leads are exposed. Turn the machine on. With a voltmeter connected to the detector terminals, obtain the lowest voltage reading when the emitter is rotated into position. When the lowest possible reading is obtained, tighten the nut on top of the emitter.

(6) Shut power off and disconnect feeder from system.

(7) Epoxy emitter.

(8) To reassemble, reverse the procedure described in steps 1 and 2.

6-11. MAJOR ADJUSTMENTS. - The following paragraphs contain procedures for major adjustments.

a. Cable Tension Adjustment. - To adjust the Carriage Drive cable tension, attach an adapter onto the threaded end of the Cable Assembly. Attach a scale and note that the scale registers a force of 10 and 11 pounds at the time when the other end of

the Cable Assembly starts moving. Note that the adapter has a number 5-40 thread.

b. Paper Gate Solenoid. - To align the Paper Gate Solenoid, remove all springs and check that the linkage arm (Figure 7-13, item 273) falls in the center of the paper stop (Figure 7-13, item 262) hole. Loosen and tighten two screws to adjust to the above requirement.

c. Paper Sensing Switch. - For adjustment of the Paper Sensing Micro Switch, loosen two screws (Figure 7-13, item 166), move switch assembly down until activator arm touches ramp deflector (128), move switch up until it just clears and is centered in the slot, then tighten screws (266). Loosen screws (251), move switch so that when the activator arm moves toward the end of the slot it clicks 1/32" away from the end of the slot, then tighten screws (251).

d. Paper Stop Gate. - To adjust the Paper Stop, loosen four number 6-32 screws (247), lift Paper Gate until it touches jig and move assembly untie it touches jig evenly; tighten screws.

e. Roller Alignment. - To align the upper and Lower rollers, perform the following:

(1) Access the upper assemblies as described in paragraph 6-9a.

(2) The upper and lower rollers are to be aligned

(2) The upper and lower rollers are to be aligned with a small square (tool makers square). The rollers must be aligned axially and tangentially to each other.

(3) The paper gap (the gap between the upper and lower platen) may not be less than 0.015 and not greater than 0.045. To adjust this, add or subtract spacers between the upper platen and guide plate for the bullet type dowels in the lower platen.

f. Timing Belt Adjustment. - The timing belt in all locations on the Paper Handling Assembly must be sufficiently taut so as not to have excessive backlash but must not be over-tightened, One may recognize if a timing belt is too tight by rotating the pulley with finger tips, and if one feels that the belt is cogging over the teeth then it is too tight. If this condition exists, tension should be released until the cogging just disappears.

g. Read Head Adjustment. - There are three objectives to be considered when adjusting the Read Head: magnification, flatness of illumination, and depth of focus. Adjusting any one of the three affects the other two. Proceed as follows:

(1) Turn off power. Remove servo fuses (F3 and F4) inside rear door.

(2) To open top half of machine; loosen the two knurled screws at front corners, and raise cover.

(3) To remove the stack feeder; loosen the knurled screw under center of hopper.

(4) Remove the t o 1/4-20 Allen cap screws, one on each corner of upper platen (near ends of upper rollers), On the front of the lower s e c t i o n a r e two ("Z" clips held by one screw each. Loosen screws so clip may rotate, Hold the two upper sections together and Lower them. When they are down, hold the paper handler section down and raise the top cover off of it. Use the two "Z" clips to hold upper section down. Tighten "Z" clip screws. Use extreme caution as there are heavy torsion springs on handler.

(5) Remove the white grill and the front key optics mirror.

(6) Connect scope channel 1 to TP7 on the Read Head Digital Board (board in J40). Connect channel 2 to TP2 on Read Head Analog Board. (On Read Head) ground probe to TP1 on the Analog Board,

(7) Move Head out of left stop, turn power on, toggle "RESET" and "START". Read Lamp should go on.

(8) Synchronize scope on channel 1 negative going. Get two pulses on channel 1 (20 Usec/Div). With Head viewing white paper only, count the peaks on channel 2 between pulses on channel 1. There MUST be 128. (See Figure 6-4.)

(9) If Head has been disassembled put the Analog Board in the center of slots and focus adjustment in the center of its range of adjustment.

(10) Adjust if necessary potentiometer R9. Check that the brightest horizontal. Line on channel 2 is 0 volts, If not adjust it. (Use 0.5 V/Div.)

(11) Next adjust for flatness of illumination by adjusting the Lamp position. The lamp is held in place by a retainer (Figure 7-20, item 192). Loosen screws to move lamp. If rotation of lamp is necessary be careful to end up with the connections in a safe place, so wires do not rub or hit right side wall. Flatness can also be adjusted by moving the Analog Board. Board should be level, be sure that the fiber light pipe is not blocking the lens. If the fiber light pipe has been removed or damaged, it may have to be rotated to get light beam parallel to the reticon chip. The average amplitude should be about 2.8 volts. Maximum variation between peaks is .5 volts. Adjust the 2.8 volt peaks by adjusting supply (top rear pot from front of machine). DO NOT allow the diodes to saturate, indicated by flattening of diode peaks. Voltage across lamp leads should be 17 to 19 volts, and must not exceed 20 volts.

(12) Once the flatness has been achieved the next adjustment is for magnification. However, when adjusting magnification you must also keep in mind the flatness and focus. Move the Head and test pattern so that the low bits fall in the center of the 128 bits on channel 2. A preliminary check on focus can be made at this time. The low bits should be no more than 1/2 of the high bits. If not, adjust the focus to

get this. See step 13. Move Head so that reticon chip is viewing section "B" (Figure 6-4) of pattern. Using the delay time base move the channel 2 scan so that you can display the last 24 bits of one scan and the first 24 bits of the next scan sample. There should be 15 ± 1 peaks not counting the lowest. If there are more than 16 high bits, the Analog Board is too high and must be lowered. To do this, loosen the three screws (item 3, Figure 1) and move the board down toward the paper, again maintaining the flatness of illumination. Tighten screws and recheck magnification.

(13) Loosen the lens locking hex nut and then loosen the Allen set screw in the center of the hex nut. (The Head will have to be removed to loosen the back screw. Follow the procedure outlined in step 15.) Use a 1/4 inch open end wrench and adjust the focus by turning the focus adjustment screw (item 186, Figure 7-20) to get maximum depth of the valley or low bits on video on channel 2. After making focus adjustment, recheck the magnification and flatness. You may have to make these adjustments several times to get them balanced.

(14) Tighten all adjustment screws and nuts, being extremely careful not to move the original adjustment setting.

(15) To remove ALPHA Read Head and cable:

(a) Remove the Read Head cable from the Read Head by removing the nut and bolt securing the end of the cable. Remove the two slide clips on the Read Head Lamp. Lift cable up off of the Read Head Analog Board.

(b) Loosen the rotation index set screw, located to the left of the two screws that hold the key optics pointers on.

(c) Loosen two thumb screws (item 185, Figure 7-20)

(d) Lift Head up and out of transverse carriage.

(e) When replacing Head,. reverse the above procedure but be sure that the rotation index set screw is in the detent made for it. Also be sure Head is seated properly in the transverse carriage.

(16) Threshold Adjustment. - When all adjustments have been made, place Head viewing customer's white paper. TP3 on the Read Head Analog Board should be approximately 2.5 volts. Set TP4 by adjusting R17 on Analog Board to approximately 60% of TP3.

Note:- A11 adjustments must be made with a scan program in the ALPHA.

(17) Turn system power off.

(18) Replace fuses removed back in step 1.

6-12. MINOR ADJUSTMENTS. - Minor adjustments of roller drift should be made as required.

a. Double Page Detector. - The Double Page Detector Circuit compensates for variations in paper densities. The setting made at the factory should be adequate for most papers; however, if the unit does not sound a warning tone and/or the error message P2 is not indicated on the display on the Control Console when

a double-page feed occurs, an adjustment of the Detector Circuit is required. To adjust, proceed as follows:

(1) Toggle the RESET position of the RESET-STOP switch located on the Control Panel.

(2) Loosen the two Control Console hand screws and raise the Control Console (Figure A-34).

(3) Set the multimeter to the 10 VDC scale. Carefully connect the common lead to Double Page Detector (Figure A-38) test point TPL (GND) and the positive lead to TP2 (Figure 6-5).

Note:- Insert a piece of paper between leads for safety.

(4) Without paper being present in the stack feeder, the multimeter should indicate approximately 0 VDC; if not, adjust the potentiometer. (It should be as close to 0 as possible but no more than 0. SVDC.)

(5) Insert a single sheet of paper in the stack feeder; the multimeter should indicate approximately 2 VDC. If not, adjust the potentiometer. This may vary the sorting of item 4.

(6) Insert two sheets of paper in the stack feeder. The multimeter should read approximately 4 VDC; if not, adjust the potentiometer. Recheck 4 and 5.

CAUTION: Be extremely careful that the two connections do not short.

(7) Turn system power off; carefully remove the test leads, and lower the Control Console.

b. Read Head and Roller Drift. - The Read Head and Paper Roller Servo Drift are adjusted to zero at the factory. However, after extended use of the unit, some drift is possible. The drift is noticeable as a movement of the rollers and/or movement of chattering of the Scan Head after ALPHA has been RESET. To correct for Read Head and Roller Drift, proceed as follows:

(1) Open rear access door (Figure A-35) to gain access to rear of the Main Wire Wrap Assembly (Figure A-39).

(2) Allow the machine to warm up for approximately five minutes before making any adjustments.

Note:- Although this drift adjustment can be accomplished by one person, the adjustment can be performed more quickly by two people; one to adjust the trimpots, the other to observe the movement of the Read Head and rollers.

(3) Toggle the RESET position of the RESET-STOP switch Located on the Control Panel,

(4) Using a small screwdriver, with a minimum of pressure, adjust the vertical adjustment trimpot on the Main Wire Wrap Assembly (Figure 6-6) for zero movement of the rollers; adjust the horizontal adjustment trimpot for zero movement of the Read Head. These trimpots are located in the lower left hand corner of Wire Wrap Board.

(5) Close the rear access door.

6-13. **FUSE REPLACEMENT, - ALPHA contains nine fuses** located **at the rear of the unit, As depicted in Figure A-40, the main AC power fuse (F9) and the convenience outlet fuse (F8) are mounted on the** rear **connector panel and** are readily accessible. **The remainder** are accessible **through the rear access door. Six fuses (F1 through F6) are mounted on the fuse panel, five active and one spare, An additional fuse (F7) is found to the right of and adjacent to the Data Save Card. The following paragraphs describe the procedure for locating and changing fuses.**

To gain access **to the internal fuses, remove the scanned text hopper (Figure A-35) at the rear of the unit by sliding it upward and** out **of the hopper supports. Depress the rear door lock and open the rear access door; unlock the inner hinged circuit panel and swing it to the left.**

The Data Save **Card (Figure A-40) contains seven red indicators (LEDs) which glow during normal ALPHA operation. The first LED at the left, DS1 (RH LAMP), indicates that power is applied to the Read Head Lamp. This indicator is off when the Read Head Lamp is off during normal operation. When any of the other LEDs (DS2 through DS7) are off, the power supply associated with the LED circuit has been interrupted,**

Table 6-5 lists all ALPHA fuses along with their type, circuit, and applicable Data Save Card Indicator. If a defective fuse is suspected, refer to the table and check to see if one or more Data Save Card Indicator(s) are off,

Table 6-5

Fuse Replacement

Reference Designation	Fuse Type	Circuit	Data Save Card Indicator
F1	Spare		
F2	10A	- Supply	DS4 (-12V), DS5 (-9V)
F3	10A	+ Servo	DS2
F4	10A	- Servo	DS3
F5	5A	8 VAC	
F6	15A	+ Supply	DS6 (+5V), DS7 (+12V)
F7	3 ASB	Test Box and Tape Punch	
F8	3 ASB	Convenience Outlet	
F9	10 ASB	AC Input	

Note:- All fuses are fast blow unless otherwise indicated.

WARNING

Before attempting to remove any fuse or examine any components of the unit, remove the main power plug.

replace associated fuse(s). The Indicator on the Data Save Panel that is associated with the defective fuse should go on after replacement, indicating a restored power supply.

6-14. MEASURING POWER SUPPLY VOLTAGES. -

a. Place ALPHA in off-line status.

b. Turn POWER switch to ON.

c. Remove any paper from stack feeder.

d. Remove lower front panel and open rear door.

e. Allow unit to warm up for approximately five minutes.

f. Release the latch on the mother beard and swing it open.

g. Measure the -12 V.D.C., +12 V.D.C., and the -9 V.D.C. power supplies on the data save card.

h. Insure all voltages are within ± .1%.

(1) If voltages are out of tolerance adjust the appropriate pot on the power supply.

i. Open the door containing the external memory assembly.

j. Measure the +5 V.D.C. at the bottom terminal of P371 as it enters the interface card on the external memory assembly, GND is the next terminal up.

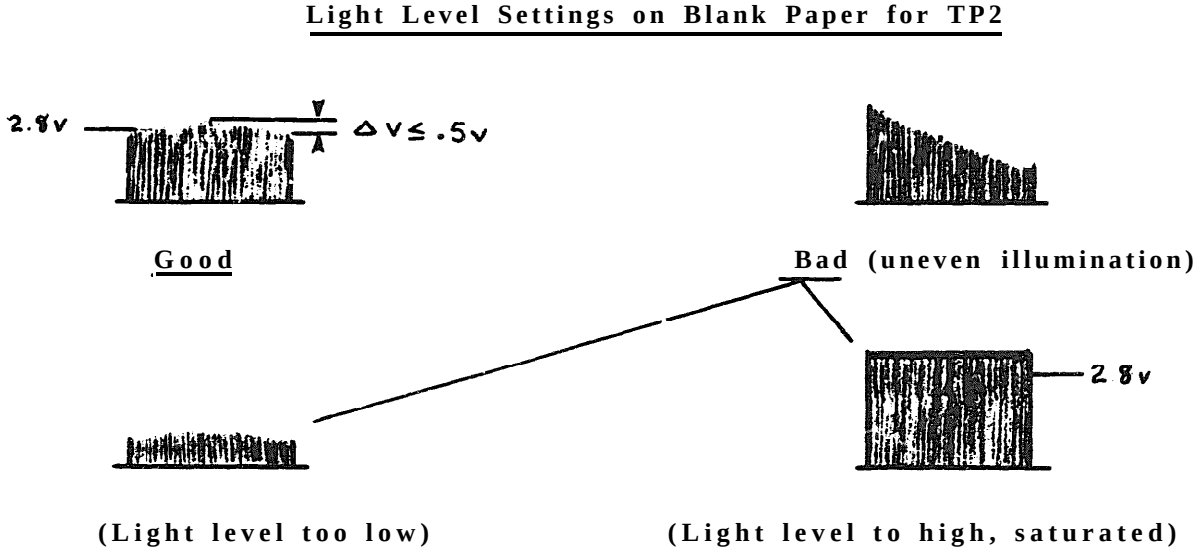
(1) Insure the voltage is 5 V.D.C. ± .1%; if not, adjust the 5V adjustment pot on the power supply.

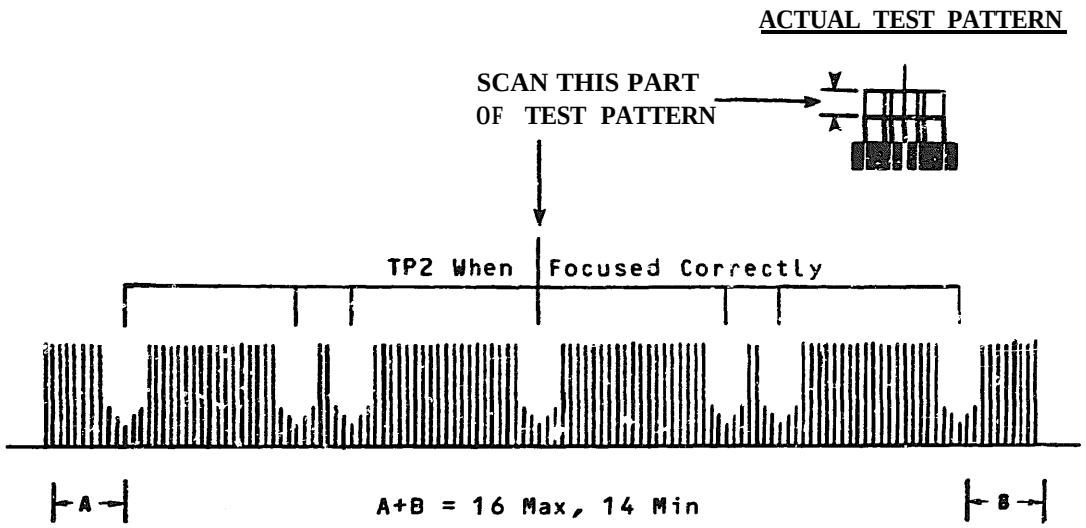
(2) Disconnect the meter.

(3) Close and secure the external memory assembly door.

k. Turn POWER switch to OFF.

6-15. MNEMONIC LISTING. - Table 6-6 contains an alphabetical listing in tabular form of every signal name used in the preceding text and on the schematic diagrams. The component, pin number, figure number, and location for each signal is listed along with the definition of the mnemonic. A summary of the scanned text flow through the ALPHA is provided in Table 6-7.





CAUTION: If light level is set too high, the valleys will not dip low enough and no data will be read from copy.

Figure 6-4. - Read Head Alignment Pattern

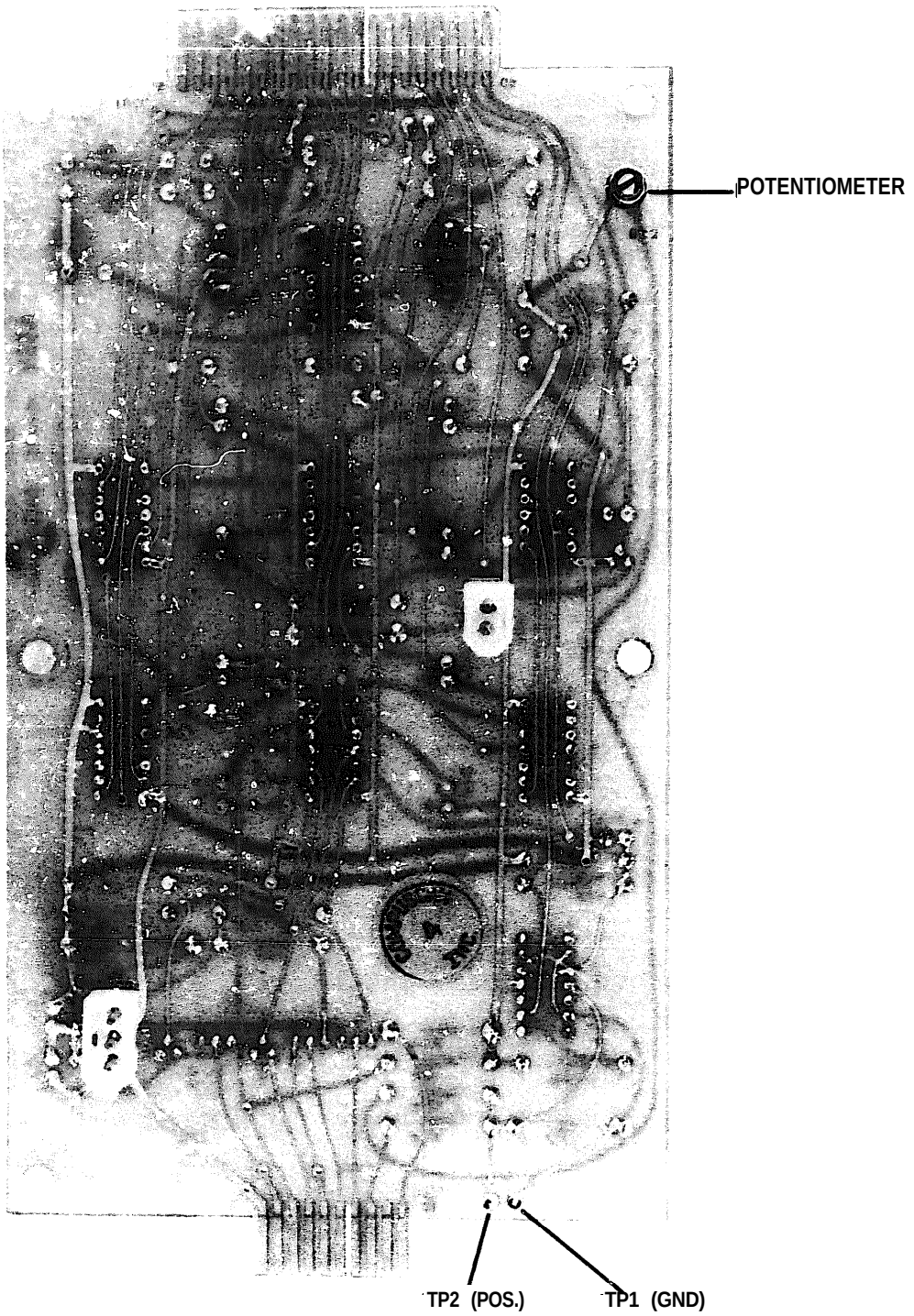


Figure 6-5. - Double Page Detector Test Points

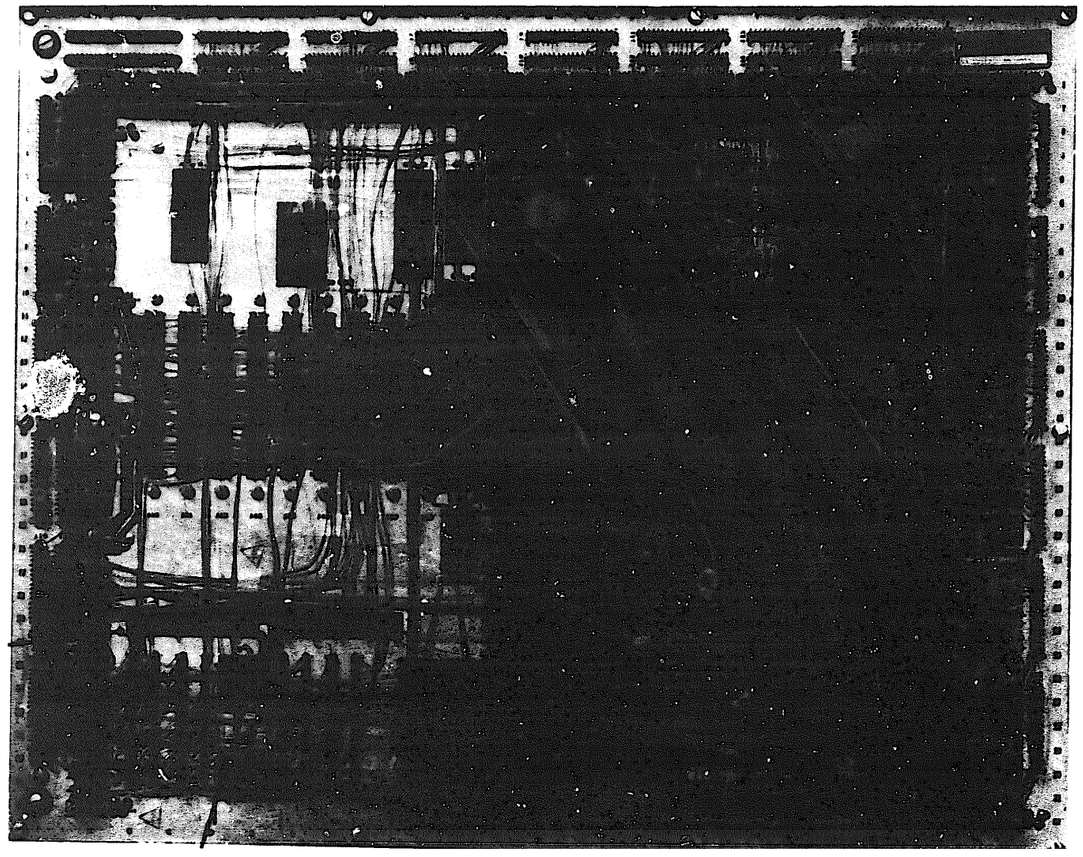


Figure 6-6. - Drift Adjustment Potentiometers

Table 6-6

Mnemonic Signal Listing

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
A	U1	3	17	A TIME
ABORT	1X	9	14	ABORT
$\overline{\text{ABORT}}$	1X	8	14	ABORT NOT
ABORT CYCLE	7Z	8	14	ABORT CYCLE
$\overline{\text{ABORT CYCLE}}$	7Z	9	14	ABORT CYCLE NOT
ACC 0	U14	3	17	ACCUMULATOR BIT 0
ACC 1	U14	2	17	ACCUMULATOR BIT 1
ACC 2	U14	6	17	ACCUMULATOR BIT 2
ACC 3	U14	7	17	ACCUMULATOR BIT 3
ACC 4	U15	3	17	ACCUMULATOR BIT 4
ACC 5	U15	2	17	ACCUMULATOR BIT 5
ACC 6	U15	6	17	ACCUMULATOR BIT 6
ACC 7	U15	7	17	ACCUMULATOR BIT 7
ALARM	13W	12	18	ALARM
ALPHABET $\overline{1/2}$	S2	2	24	ALPHABET 1/2 NOT
ALPHABET $\overline{1/2}$	22A	12	7	ALPHABET 1 NOT/2
ARITH	U4	8	17	ARITHMETIC INSTRUCTION
$\overline{\text{ARITH}}$	U3	5	17	ARITHMETIC INSTRUCTION NOT
ARO JUMP	15R	8	11	ARITHMETIC OVERFLOW JUMP
$\overline{\text{ARO 2}}$	23M	12	1	ARITHMETIC OVERFLOW # 2 NOT
$\overline{\text{ARO 3}}$	32L	12	2	ARITHMETIC OVERFLOW # 3 NOT
$\overline{\text{ARO 4}}$	U2	8	24	ARITHMETIC OVERFLOW # 4 NOT
B	U1	4	17	B TIME
B0	8P	15	6	BOTTOM BIT 0
B1	8P	13	6	BOTTOM BIT 1
B2	8P	12	6	BOTTOM BIT 2
B3	8P	11	6	BOTTOM BIT 3
B4	8R	15	6	BOTTOM BIT 4
B5	8R	13	6	BOTTOM BIT 5
B6	8R	12	6	BOTTOM BIT 6
B7	8R	11	6	BOTTOM BIT 7
$\overline{\text{BBS}}$	1P	2	6	BAD BOTTOM SPACE NOT
BE0	8X	7	14	BEST ERROR BIT Cl
BE1	8X		14	BEST ERROR BIT 1
BE2	8X	2	14	BEST ERROR BIT 2
BE3	8X	3	14	BEST ERROR BIT 3
BE4	8Z	5	14	BEST ERROR BIT 4
BE5	8Z	9	14	BEST ERROR BIT 5
BHTL	6P	7	6	BIT HEIGHT LOW (BTS)

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
BID 0	5X	7		BEST ID BIT 0
BID 1	5X		14	BEST ID BIT 1
BID 2	5X	2		BEST ID BIT 2
BID 3	5X	3	14	BEST ID BIT 3
BID 4	4X		14	BEST ID BIT 4
BID 5	4X	6	14	BEST ID BIT 5
BID 6	4X	2	14	BEST ID BIT 6
BID 7	4X	3	14	BEST ID BIT 7
BKNF	2R		6	BROKEN FLOP
$\overline{\text{BKNF}}$	2R	8	6	BROKEN FLOP NOT
BOT MARGIN	16P	15	18	BOTTOM MARGIN
BRAKE			23	BRAKE NOT
BRKPT	10M	8	18	BREAKPOINT
BSO	M	3	15	BUFFER STROBE BIT 0
BS1	17M	2	15	BUFFER STROBE BIT 1
BSZF	2N	9	6	BOTTOM SPACE ZERO FLAG
C	U1		17	C TIME
$\overline{\text{C}}$	U28	8	17	C TIME NOT
$\overline{\text{CEF}}$	25N	6		CHARACTER END FLAG NOT
$\overline{\text{CJMP}}$	U16	5	17	CONDITIONAL JUMP NOT
CK	U1	4	5	VIDEO CLOCK NOT
$\overline{\text{CLEAR STATE}}$	24S	17	11	CLEAR STATE NOT
$\overline{\text{CLEAR XY SR}}$	24S	2		CLEAR X Y SHIFT REGISTERS NOT
$\overline{\text{CLK BE}}$	13Z		11	CLOCK BEST ERROR
$\overline{\text{CLK BE}}$	18X	6	11	CLOCK BEST ERROR NOT
$\overline{\text{CLK BE MX}}$	18X	7	11	CLOCK BEST ERROR MULTIPLEXER NOT
CLRNDBO	U26	11	10	NOT USED
$\overline{\text{CLRURM}}$	22T	2	7	CLEAR UNKNOWN RAM ADDRESS NOT
$\overline{\text{CLSFLG}}$	14S	3		CLEAR SCAN FLAGS NOT
CLURA	16W	8	11	CLEAR UNKNOWN RAM ADDRESS
$\overline{\text{CLUTCH}}$	Q2		23	CLUTCH NOT
$\overline{\text{CMP}}$	U3	6	17	COMPARE INSTRUCTION NOT
$\overline{\text{CMP MX}}$	13N	1	18	COMPARE MULTIPLEXER INSTRUCTION NOT
$\overline{\text{CNT PULSE}}$	U23	6	17	COUNT PULSE NOT
CONTINUE	16L	15	18	CONTINUE
CPM 0	4U	4	7	CHARACTER PARAMETER MEMORY BIT 0
CPM 1	4U	2	7	CHARACTER PARAMETER MEMORY BIT 1

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
CPM 2	5U	12	7	CHARACTER PARAMETER MEMORY BIT 2
CPM 3	5U	10	7	CHARACTER PARAMETER MEMORY BIT 3
CPM 4	5U	8	7	CHARACTER PARAMETER MEMORY BIT 4
CPM 5	5U	6	7	CHARACTER PARAMETER MEMORY BIT 5
CPM 6	5U	4	7	CHARACTER PARAMETER MEMORY BIT 6
CPM 7	5U	2	7	CHARACTER PARAMETER MEMORY BIT 7
CPM 8	6U	8	7	CHARACTER PARAMETER MEMORY BIT 8
CPM 9	6U	6	7	CHARACTER PARAMETER MEMORY BIT 9
CPM 10	6U	4	7	CHARACTER PARAMETER MEMORY BIT 10
CPM 11	6U	2	7	CHARACTER PARAMETER MEMORY BIT 11
CPM 12	4U	12	7	CHARACTER PARAMETER MEMORY BIT 12
CPM 13	4U	10	7	CHARACTER PARAMETER MEMORY BIT 13
CPM 14	4U	8	7	CHARACTER PARAMETER MEMORY BIT 14
CPM 15	4U	6	7	CHARACTER PARAMETER MEMORY BIT 15
CTTF	11U	7	6	CHARACTER TOO TALL FLAG
CW 2	5V	2	14	CHARACTER WIDTH BIT 2
CW 4	5V	5	14	CHARACTER WIDTH BIT 4
CW 8	5V	7	14	CHARACTER WIDTH BIT 8
CW 16	5V	10	14	CHARACTER WIDTH BIT 16
D	U1	6	17	D TIME
$\overline{D}$	U26	4	17	D TIME NOT
$\overline{DO}$	U15	6	10	RECO RAM DATA NOT
$\overline{DO1}$	U3	8	10	SRECO RAM DATA NOT
$\overline{DO\ MUX}$	U37	9	10	RAM DATA SELECT NOT
$\overline{DATA\ 8}$	U24	6	20	DATA BIT 8 NOT
$\overline{DATA\ 9}$	U24	5	20	DATA BIT 9 NOT
$\overline{DATA\ 10}$	U24	4	20	DATA BIT 10 NOT
$\overline{DATA\ 11}$	U24	3	20	DATA BIT 11 NOT

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
DATA 12	U28	6	20	DATA BIT 12 NOT
DATA 13	U28	5	20	DATA BIT 13 NOT
DATA 14	U28	4	20	DATA BIT 14 NOT
DATA 15	U28	3	20	DATA BIT 15 NOT
DATA AVAIL	U38	6	20	DATA AVAILABLE
DATA RDY	U43	6	20	DATA READY NOT
DEC CTRS	13W	4	11	DECREMENT COUNTERS
DEC CTRS	24S	7	11	DECREMENT COUNTERS NOT
DEC FF	18P	9	18	DECREMENT FLIP FLOP
DEC RCTR	13W	2	11	DECREMENT REFERENCE ALPHABET ADDRESS
DEC VERT	11N	6	18	DECREMENT VERTICAL REGISTER NOT
D LEFT	28M			DRIVE LEFT
D LEFT	20S	4	2	DRIVE LEFT NOT
DOUBLE DISABLE	M	12	18	NOT USED
DOUBLE PAGE	10N	3	18	DOUBLE PAGE NOT
D RIGHT	28M	10		DRIVE RIGHT
D RIGHT	20S	3	2	DRIVE RIGHT NOT
DRIVE RIGHT MUX	10W	4	11	DRIVE RIGHT SELECT NOT
D UP	20T	4	1	DRIVE UP NOT
E		10		E TIME
EO	19W	5	14	ERROR BIT 0
E1	19x		14	ERROR BIT 1
E2	19Y	5	14	ERROR BIT 2
E3	20W	5		ERROR BIT 3
E4	20X		14	ERROR BIT 4
E5	20Y	5	15	ERROR BIT 5
E<BE	9Y	7	14	ERROR LESS THAN BEST ERROR
E>BE	9Y	5	14	ERROR GREATER THAN BEST ERRO
ECLK	3x	4	14	EVALUATION CLOCK
ECT1	11Z	3	14	ERROR SELECT COUNT 1
ECT2	11Z	2	14	ERROR SELECT COUNT 2
ECT4	11Z	6	14	ERROR SELECT COUNT 4
E CYCLE	1Y	8	14	ERROR CYCLE NOT
EMAB0	U9	3	17	EXECUTIVE MACRO ADDRESS BIT 0
EMAB1	U9	2	17	EXECUTIVE MACRO ADDRESS BIT 1
EMAB2	U9	6	17	EXECUTIVE MACRO ADDRESS BIT 2
EMAB3	U9	7	17	EXECUTIVE MACRO ADDRESS BIT 3
EMAB4	U10	3	17	EXECUTIVE MACRO ADDRESS BIT 4

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
EMAB5	U10	2	17	EXECUTIVE MACRO ADDRESS BIT 5
EMAB6	U10	6	17	EXECUTIVE MACRO ADDRESS BIT 6
EMAB7	U10	7	17	EXECUTIVE MACRO ADDRESS BIT 7
EMAB8	U11	3	17	EXECUTIVE MACRO ADDRESS BIT 8
EMAB9	U11	2	17	EXECUTIVE MACRO ADDRESS BIT 9
EMAB10	U11	6	17	EXECUTIVE MACRO ADDRESS BIT IO
EMAB11	U11	7	17	EXECUTIVE MACRO ADDRESS BIT 11
EM GRP	15N	6	18	NOT USED
EM HSMP	18W	6	2	EXECUTIVE MACRO HORIZONTAL SAMPLE NOT
EMOBO - 15	PROMS		19	EXECUTIVE MEMORY OUTPUT BITS
EM SAMP RESET	15P	3	18	EXECUTIVE MACRO SAMPLE RESET NOT
EMSPLF	5R	3	6	EXECUTIVE MACRO SAMPLE FLAG
EMV SMP	18W	8	1	EXECUTIVE MACRO VERTICAL SAMPLE NOT
ENABL	U39	10	20	ENABLE
ENABLE ECTR	1Y	6	14	ENABLE ERROR COUNTERS NOT
ENABLE KEYBOARD	15M	4	18	ENABLE KEYBOARD NOT
ENCODER SAMPLE	22T	8	2	ENCODER SAMPLE
END JUST	15U	6	11	END OF JUSTIFICATION NOT
END OF CYCLE	1Y	11	14	END OF CYCLE NOT
EQUL	12M	5	18	CMP MX EQUAL TO ACC
ERROR 1	29V		12	ERROR # 1
ERROR 2	29V	8	12	ERROR # 2
ERROR 3	29W	12		ERROR # 3
ERROR 4	29W	6	12	ERROR # 4
ERROR 5	29W	8	12	ERROR # 5
ERROR 6	29X	12	12	ERROR # 6
ERROR 7	29X	6	12	ERROR # 7
ERROR 8	29X	8	12	ERROR # 8
ESCN	12S	10	6	END SCAN
EV1	U21	4	5	VIDEO ENVELOPE 1
EV2	U21	3	5	VIDEO ENVELOPE 2

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
EXT BRKT	10M		18	EXTERNAL BREAK POINT
EXT INC URM	22T	5	7	EXTERNAL INCREMENT URAM ADDRESS NOT
EXT INST	FROM TEST SET			EXTERNAL INSTRUCTION
F	U1	11	17	F TIME
F1	U6	9	10	FAILURE MODE 1
F2	U6	10	10	FAILURE MODE 2
F3	U6	1	10	FAILURE MODE 3
F4	U6	13	10	FAILURE MODE 4
FAIL 1	U6	8	10	FAIL 1
FAIL 2	U6	12	10	FAIL 2
FBI	5P	3	6	FOUND BIT I
FB2	SN	5	6	FOUND BIT 2
FC	22N		6	FOUND BIT CORRELATED
FEED	19T	3		FEED
FEED HOLE	U12		20	NOT USED
FORMAT	10N	13	18	NOT USED
G	U1	12	17	G TIME
GENERAL RESET	15S			GENERAL RESET NOT
GRATR	12M	9	18	CMP MX GREATER THAN ACC
GR CJMP	14P	8	18	GROUP CONDITIONAL JUMP
GR0 CJUMP	13P			GROUP 0 CONDITIONAL JUMP NOT
GR1 CJUMP	12N	6	18	GROUP 1 CONDITIONAL JUMP NOT
GR2 CJUMP	16N	6	18	GROUP 2 CONDITIONAL JUMP NOT
GR3 CJUMP	16L	6	18	GROUP 3 CONDITIONAL JUMP NOT
GR4 CJUMP	16M	6	18	GROUP 4 CONDITIONAL JUMP NOT
GR5 CJUMP	16P	6	18	GROUP 5 CONDITIONAL JUMP NOT
GR0 TEST	U32	1	17	GROUP 0 TEST NOT
GR1 TEST	U32	2		GROUP 1 TEST NOT
GR2 TEST	U32		17	GROUP 2 TEST NOT
GR3 TEST	U32	4	17	GROUP 3 TEST NOT
GROUP CLK 1	8V	12	14	GROUP CLOCK ONE
GROUP CLK 1	8V	13	14	GROUP CLOCK ONE NOT
GROUP CLK 2	W		14	GROUP CLOCK TWO NOT
H	U1	13	17	H TIME
H	U29	12	17	H TIME NOT
HALT			18	HALT NOT
HDA1	28I	3	2	HORIZONTAL DIGITAL TO ANALOG BIT 1
HDA2	28I	6	2	HORIZONTAL DIGITAL TO ANALOG BIT 2
HDA3	28I	8	2	HORIZONTAL DIGITAL TO ANALOG BIT 3

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
HDA4	28I	II	2	HORIZONTAL DIGITAL TO ANALOG BIT 4
HDAS	29I	3	2	HORIZONTAL DIGITAL TO ANALOG BIT S
HDA6	29I	6	2	HORIZONTAL DIGITAL TO ANALOG BIT 6
HDA7	29I	8	2	HORIZONTAL DIGITAL TO ANALOG BIT 7
HDA8	29I	11	2	HORIZONTAL DIGITAL TO ANALOG BIT 8
HEAD IN MOTION	18L	13	2	HEAD IN MOTION
HEN 1	2K	5	2	HORIZONTAL ENCODER PHASE 1
HEN 1	2K	6	2	HORIZONTAL ENCODER PHASE 1 NOT
HEN 1B	4A	6	2	HORIZONTAL ENCODER PHASE 1 BUFFERED
HEN 2	2K	9	2	HORIZONTAL ENCODER PHASE 2
HEN 2	2K	8	2	HORIZONTAL ENCODER PHASE 2 NOT
HEN 2B	4A	8	2	HORIZONTAL ENCODER PHASE 2 BUFFERED
HOLD	2OU	5	II	HOLD
HOR DN	1K	11	2	HORIZONTAL DOWN PULSE NOT
HOR UP	4A	10	2	HORIZONTAL UP PULSE NOT
HP CL INH	19S	2	2	HORIZONTAL CLEAR INHIBIT
H POS	20S	2	2	HORIZONTAL POSITION NOT
HSA±	32A	10	2	HORIZONTAL SERVO AMPLIFIED VOLTAGE ±
H STOP	20S	1	2	HORIZONTAL STOP NOT
HT 1	N	9	6	HEIGHT BIT 1
HT 2	7N	6	6	HEIGHT BIT 2
HT 4	7N			HEIGHT BIT 4
HT 8	7N	15	6	HEIGHT BIT 8
HT 16	6N	9	6	HEIGHT BIT 16
HT 32	6N	6	6	HEIGHT BIT 32
HT 64	6N	2	6	HEIGHT BIT 64
HT 128	6N	15	6	HEIGHT BIT 128
HTC±	31A	10		HORIZONTAL TACH ±
HTZ	11X	4	11	HEIGHT OF ZERO
IEMAB0	U12	4	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 0
IEMAB1	U12	7	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 1

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
IEMAB2	U12	12	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 2
IEMAB3	U12	9	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 3
IEMAB4	U13	4	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 4
IEMAB5	U13	7	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 5
IEMAB6	U13	12	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 6
IEMAB7	U13	9	17	INPUT EXECUTIVE MACRO ACCUMULATOR BIT 7
INC B MAR	11N	7		INCREMENT BOTTOM MARGIN NOT
INC CH 1	15L	5	18	INCREMENT LED CHARACTER 1 NOT
INC CH 2	15L	6	18	INCREMENT LED CHARACTER 2 NOT
INC CH 3	15L	7	18	INCREMENT LED CHARACTER 3 NOT
INC CPM CTR 1	24S	5	11	INCREMENT CPM COUNTER PULSE ONE NOT
INC CPM CTR 2	24S	15	11	INCREMENT CPM COUNTER PULSE TWO NOT
INC FF	18P	5	18	INCREMENT FLIP FLOP
INC HORZ	11N	4	18	INCREMENT HORIZONTAL REGISTER NOT
INC KYBD	15N	7	18	INCREMENT KEYBOARD NOT
INCL	11N		18	SHIFT COMPARE LATCH LEFT NOT
INCPA	21T	12		INCREMENT CPM ADDRESS COUNTER
INCR	11N	2	18	SHIFT COMPARE LATCH RIGHT NOT
INCRNDA	U2	3	10	INCREMENT REFERENCE START ADDRESS COUNTER
INC URCTR	16V	3	11	INCREMENT URAM ADDRESS COUNTER NOT
INCR INST	U34	5	20	INCREMENT INSTRUCTION
INCR XADD	U43	11	20	INCREMENT DATA ADDRESS COUNTER NOT
INC VERT	11N	3	18	INCREMENT VERTICAL REGISTER NOT
I/O ADD 0	U26	3	20	INPUT/OUTPUT ADDRESS 0
I/O ADD 1	U26	2		INPUT/OUTPUT ADDRESS 1
I/O ADD 2	U26	6	20	INPUT/OUTPUT ADDRESS 2
I/O ADD 3	U26	7	20	INPUT/OUTPUT ADDRESS 3

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
I/O ADD 4	U22	3	20	INPUT/OUTPUT ADDRESS 4
I/O ADD 5	U22	2	20	INPUT/OUTPUT ADDRESS 5
I/O ADD 6	U22		20	INPUT/OUTPUT ADDRESS 6
I/O ADD 7	U22	7	20	INPUT/OUTPUT ADDRESS 7
I/O ADD 8	U18	3		INPUT/OUTPUT ADDRESS 8
I/O ADD 9	U18	2	20	INPUT/OUTPUT ADDRESS 9
I/O ADD 10	U18	6	20	INPUT/OUTPUT ADDRESS 10
I/O ADD 11	U18	7	20	INPUT/OUTPUT ADDRESS 11
IOBFR 0	1A	4	15	LINE BUFFER INPUT BIT 0
IOBFR 1	1A		15	LINE BUFFER INPUT BIT 1
IOBFR 2	1A	12	15	LINE BUFFER INPUT BIT 2
IOBFR 3	1A	9	15	LINE BUFFER INPUT BIT 3
IOBFR 4	2A	4	15	LINE BUFFER INPUT BIT 4
IOBFR 5	2A	7	15	LINE BUFFER INPUT BIT 5
IOBFR 6	2A	12	15	LINE BUFFER INPUT BIT 6
IOBFR 7	2A	9	15	LINE BUFFER INPUT BIT 7
$\overline{\text{I/O CYCLE}}$	U35	9	20	INPUT/OUTPUT CYCLE NOT
I/O CYCLE DONE	U31	9	20	INPUT/OUTPUT CYCLE DONE
I/O REQ	U31	5	20	INPUT/OUTPUT CYCLE REQUEST
I/O STRT	U43	a	20	INPUT/OUTPUT CYCLE START NOT
IR	P320	7	32	DOUBLE DETECT EMITTER
IR 0	U34	2	19	INSTRUCTION REGISTER BIT 0
IR 1	U34	5	19	INSTRUCTION REGISTER BIT 1
IR 2	U34			INSTRUCTION REGISTER BIT 2
IR 3	U34	10	19	INSTRUCTION REGISTER BIT 3
IR 4	U34	12	19	INSTRUCTION REGISTER BIT 4
IR 5	U34	15	19	INSTRUCTION REGISTER BIT 5
IR 6	U35	2	19	INSTRUCTION REGISTER BIT 6
IR 7	U35	5	19	INSTRUCTION REGISTER BIT 7
IR 8	U35		19	INSTRUCTION REGISTER BIT 8
IR 9	U35	10	19	INSTRUCTION REGISTER BIT 9
IR 10	U35		19	INSTRUCTION REGISTER BIT 10
IR 11	U35	15	19	INSTRUCTION REGISTER BIT 11
IR 12	U36	2	19	INSTRUCTION REGISTER BIT 12
IR 13	U36	5	19	INSTRUCTION REGISTER BIT 13
IR 14	U36	7	19	INSTRUCTION REGISTER BIT 14
IR 15	U36	10	19	INSTRUCTION REGISTER BIT 15
$\overline{\text{IR 3}}$	U28	2	17	INSTRUCTION REGISTER BIT 3 NOT
$\overline{\text{IR 8}}$	18R	4	18	INSTRUCTION REGISTER BIT, 8 NOT
$\overline{\text{IR 9}}$	18R	8	18	INSTRUCTION REGISTER BIT 9 NOT

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
$\overline{\text{IR 10}}$	18R	12	18	INSTRUCTION REGISTER BIT 10 NOT
$\overline{\text{IR 11}}$	18R	6	18	INSTRUCTION REGISTER BIT 11 NOT
$\overline{\text{IR 12}}$	18R	10	18	INSTRUCTION REGISTER BIT 12 NOT
$\overline{\text{IR 13}}$	18T	2	18	INSTRUCTION REGISTER BIT 13 NOT
$\overline{\text{IR 14}}$	18T	4	18	INSTRUCTION REGISTER BIT 14 NOT
$\overline{\text{IR 15}}$	18T	8	18	INSTRUCTION REGISTER BIT 15 NOT
IR 4B	U24	8	17	INSTRUCTION REGISTER BIT 4 BUFFERED
IR 5B	U24	4	17	INSTRUCTION REGISTER BIT 5 BUFFERED
IR 6B	U24	10	17	INSTRUCTION REGISTER BIT 6 BUFFERED
IR 7B	U25	4	17	INSTRUCTION REGISTER BIT 7 BUFFERED
IR 12B	18S	3	18	INSTRUCTION REGISTER BIT 12 BUFFERED
IR 13B	18S	6	18	INSTRUCTION REGISTER BIT 13 BUFFERED
IR 14B	18S	8	18	INSTRUCTION REGISTER BIT 14 BUFFERED
IR 15B	18S	11	18	INSTRUCTION REGISTER BIT 15 BUFFERED
IRNDA 0	U27	3	10	REF START ADDRESS 0
IRNDA 1	U27	2	10	REF START ADDRESS 1
IRNDA 2	U27	6	10	REF START ADDRESS 2
IRNDA 3	U27	7		REF START ADDRESS 3
IRNDA 4	U28	3	10	REF START ADDRESS 4
IRNDA 5	U28	2	10	REF START ADDRESS 5
$\overline{\text{JMP}}$	U3	1	17	JUMP INSTRUCTION NOT
JUST	8U	5		JUSTIFICATION
JUST	8U	6	6	JUSTIFICATION NOT
KB 0	KEYBOARD			KEYBOARD BIT 0
KB 1	KEYBOARD			KEYBOARD BIT 1
KB 2	KEYBOARD			KEYBOARD BIT 2
KB 3	KEYBOARD			KEYBOARD BIT 3
KB 4	KEYBOARD			KEYBOARD BIT 4

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
KB 5	KEYBOARD			KEYBOARD BIT 5
KB 6	KEYBOARD			KEYBOARD BIT 6
KB 7	KEYBOARD			KEYBOARD BIT 7
KBD 0			15	KEYBOARD DATA BIT 0
KBD 1	1B	2	15	KEYBOARD DATA BIT 1
KBD 2	1B	6	15	KEYBOARD DATA BIT 2
KBD 3				KEYBOARD DATA BIT 3
KBD 4	2B	3	15	KEYBOARD DATA BIT 4
KBD 5	2B	2	15	KEYBOARD DATA BIT 5
KBD 6	2B	6	15	KEYBOARD DATA BIT 6
KBD 7	2B	7	15	KEYBOARD DATA BIT 7
KBSTB	KEYBOARD			KEYBOARD STROBE
KEY LAMP DRIVER	2D	6		KEY LAMP DRIVER
KEY OPTICS	16M	2	18	KEY OPTICS
KYBD	20	9	15	KEY BOARD
KYBD ENTRY	16M	2	18	KEYBOARD ENTRY
LAST PLANE	2OU	9	11	LAST PLANE
LAST SHIFT	21U	5	11	LAST PLANE SHIFT
LBLF	2R	5		LOAD BOTTOM LATCH FLAG
LDBS	15S	2	18	LOAD BOTTOM SPACE NOT
LDBWL	15N	2	18	LOAD BOTTOM WINDOW LATCH NOT
LDCW	15N			LOAD CHARACTER WIDTH NOT
LD FLGS	13N	3	18	LOAD FLAGS NOT
LD MX HT	13N		18	LOAD MAXIMUM HEIGHT NOT
LD OAR	U2	11	17	LOAD ACCUMULATOR AND EXECUTIVE MACRO RAM NOT
LDTSC	15S	3	18	LOAD TOP SPACE CRITERIA NOT
LDTWL	15N	3	18	LOAD TOP WINDOW LATCH NOT
LDWNDO	12S		6	LOAD WINDOW NOT
LIR	R/F	9	2	LEFT PHOTOCELL EMITTER
LINE SPACING	16M	3	18	LINE SPACING
L JUST	IOU	10	6	LEFT JUSTIFICATION MODE (FINISHED)
L JUST	6U	12	6	LEFT JUSTIFICATION MODE (FINISHED? NOT
LLS	19N	4		LOAD HORIZONTAL LEFT SPEED
LOAD	U4	6	17	LOAD INSTRUCTION
LOAD	U3	4	17	LOAD INSTRUCTION NOT
L O A D	13N	7		LOAD INSTRUCTION # 6 NOT
LOAD 7	13N	9	18	LOAD INSTRUCTION # 7 NOT
LOAD ACC	U22	3	17	LOAD ACCUMULATOR NOT

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN FIGURE A-		DEFINITION
LOAD IBFR	U30	8	20	LOAD INPUT BUFFER NOT
LOAD I/O	13N	6	18	LOAD INPUT/OUTPUT NOT
LOAD I/O ADD HI	U41	14	20	LOAD I/O ADDRESS HIGH ORDER BITS NOT
LOAD I/O ADD LO	U41	13	20	LOAD I/O ADDRESS LOW ORDER BITS NOT
LOAD IR	U26	10		LOAD INSTRUCTION REGISTER
LOAD IR	U6	9	17	LOAD INSTRUCTION REGISTER NOT
LOAD IRB	U26	8	17	LOAD INSTRUCTION REGISTER BUFFERED
LOAD LATCHES	1Y	3	14	LOAD LATCHES NOT
LOAD MECH	18R	2	18	LOAD MECHANICAL INSTRUCTION LATCH
LOAD MECH	13N	5	18	LOAD MECHANICAL INSTRUCTION LATCH NOT
LOAD STATE	14Y	8	11	LOAD STATE NOT
LOAD SWITCH	15N	9	18	LOAD SWITCHES NOT
LOAD XADD HI	U33	15	20	LOAD DATA ADDRESS HIGH ORDER BITS NOT
LOAD XADD LO	U33	14	20	LOAD DATA ADDRESS LOW ORDER BITS NOT
LOAD XY1	24S	6	11	LOAD X Y SHIFT REGISTERS SIGNAL 1 NOT
LOAD XY2	24S	13	11	LOAD X Y SHIFT REGISTERS SIGNAL 2 NOT
LOAD XYSR	23T	6		LOAD X Y SHIFT REGISTERS NOT
LOW 2	2W	5	14	LOW 2
LOW TAPE	16M	15	18	NOT USED
LPC	R/F	11	2	LEFT PHOTO CELL
LRS	19N	2	2	LOAD HORIZONTAL RIGHT SPEED
L STOP	22S	10	2	LEFT STOP
L-STOP	20L		2	LEFT STOP NOT
LTLF	1R	10	6	LOAD TOP LATCH FLAG
LT/RT MARG	32K	14	2	LEFT OR RIGHT MARGIN
LUS	19N	6	1	LOAD UP SPEED
MASK OUT	17X	8	11	MASK OUT NOT
MEM ADD 0	U23	4	20	EXTERNAL MEMORY ADDRESS BIT 0
MEM ADD 1	U23	7	20	EXTERNAL MEMORY ADDRESS BIT 1
MEM ADD 2	U23	9	20	EXTERNAL MEMORY ADDRESS BIT 2

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
MEM ADD 3	U23	12	20	EXTERNAL MEMORY ADDRESS BIT 3
MEM ADD 4	U19	4	20	EXTERNAL MEMORY ADDRESS BIT 4
MEM ADD 5	U19	7	20	EXTERNAL MEMORY ADDRESS BIT 5
MEM ADD 6	U19	9	20	EXTERNAL MEMORY ADDRESS BIT 6
MEM ADD 7	U19	12	20	EXTERNAL MEMORY ADDRESS BIT 7
MEM ADD 8	U15	4	20	EXTERNAL MEMORY ADDRESS BIT 8
MEM ADD 9	U15	7	20	EXTERNAL MEMORY ADDRESS BIT 9
MEM ADD 10	U15	9	20	EXTERNAL MEMORY ADDRESS BIT 10
MEM ADD 11	U15	12	20	EXTERNAL MEMORY ADDRESS BIT 11
MEM DELAY	U42	2	20	MEMORY DELAY
MEM INST	U37	8	20	MEMORY INSTRUCTION
MEM RESET	U32	6	20	NOT USED
MX 0	11L	7	18	COMPARE MULTIPLEXER BIT 0
MX 1	11L	9	18	COMPARE MULTIPLEXER BIT 1
MX 2	12L		18	COMPARE MULTIPLEXER BIT 2
MX 3	12L	9	18	COMPARE MULTIPLEXER BIT 3
MX 4	13L		18	COMPARE MULTIPLEXER BIT 4
MX 5	13L	9	18	COMPARE MULTIPLEXER BIT 5
MX 6	14L	7	18	COMPARE MULTIPLEXER BIT 6
MX 7	14L	9	18	COMPARE MULTIPLEXER BIT 7
NARROW UNK	3V	5	14	NARROW UNKNOWN
NO COMPARE	17Y		11	NO COMPARE
NO COMPARE	18U	8	11	NO COMPARE NOT
NBS 4	4Y	7	14	NOMINAL BOTTOM SPACE BIT 4
NBS 8	4Y	9	14	NOMINAL BOTTOM SPACE BIT 8
NBS 16	5Y	7	14	NOMINAL BOTTOM SPACE BIT 16
NBS 32	5Y		14	NOMINAL BOTTOM SPACE BIT 32
OBFR 0	1s	5	16	LINE BUFFER OUTPUT BIT 0
OBFR 1	1s	12	16	LINE BUFFER OUTPUT BIT 1
OBFR 2	2s		16	LINE BUFFER OUTPUT BIT 2
OBFR 3	2s	12	16	LINE BUFFER OUTPUT BIT 3
OBFR 4	4s	5	16	LINE BUFFER OUTPUT BIT 4
OBFR 5	4s	12	16	LINE BUFFER OUTPUT BIT 5

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN FIGURE A-		DEFINITION
OBFR 6	5S	5	16	LINE BUFFER OUTPUT BIT 6
OBFR 7	5S	12	16	LINE BUFFER OUTPUT BIT 7
0BFR 10	18N	12	15	LINE BUFFER OUTPUT BIT 10
0BFR 11	18N	9	15	LINE BUFFER OUTPUT BIT 11
0N LINE	U39	5	20	ON LINE
OUTPUT	16M	14	18	OUTPUT
OUTPUT BSY	U30	5	20	OUTPUT BUSY
OUTPUT STROBE	15N	4	18	OUTPUT STROBE NOT
OVER FLOW	U16	8	17	OVER FLOW NOT
PAP IN POS	18L	12	1	PAPER IN POSITION
PAPER PRESENT --	2E	3	1	PAPER PRESENT
PAPER SENSE SWITCH	P320	14	32	PAPER SENSE SWITCH
PARTIAL 1	6Z	5	14	PARTIAL 1 NOT
PARTIAL 2	6Z	8	14	PARTIAL 2
PARTIAL 2	6Z	9	14	PARTIAL 2 NOT
PARTIAL 1 HI	2X		14	PARTIAL 1 HIGH
PARTIAL 1 LO	W	5	14	PARTIAL 1 LOW
PARTIAL 2 HI	2X	9	14	PARTIAL 2 HIGH
PARTIAL 2 LO	5W		14	PARTIAL 2 LOW
PC COM	P320	15	32	PHOTOCELL GROUND
PC DOUBLE DOCUMENT	P320	8	32	DOUBLE DOCUMENT PHOTOCELL
PF MOTOR (RELAY)	Q3	C	23	PAGE FEEDER MOTOR ON NOT (RELAY)
PF MOTOR ON	23U	6	1	PAGE FEEDER MOTOR ON NOT
PGS DOWN	Q4		23	PAPER GATE SOLENOID NOT
PGS DOWN/UP	14R	6	1	PAPER GATE DOWN
PITCH (10/12)	16P	2	18	PITCH
PLB 3	16S	4	18	PULSE B INSTRUCTION # 3 NOT
PLB 4	16S	5	18	PULSE B INSTRUCTION # 4 NOT
PLB 6	16S	7	18	PULSE B INSTRUCTION # 6 NOT
PLB 7	16S		18	PULSE B INSTRUCTION # 7 NOT
PMF	5P	6	6	POSITION MODE FLAG
PMF SYNC	19U	8	6	POSITION MODE FLAG SYNC NOT
POPF	2N		6	POPULATION FLAG
PRESET 48	10Y	6	14	PRESET 48 NOT
PULSE	U4		17	PULSE INSTRUCTION
-PULSE	U3	2	17	PULSE INSTRUCTION NOT
PWR ON RESET	14S	8	18	POWER ON RESET NOT
RAM 0	U25	12	17	EXECUTIVE MACRO RAM OUTPUT BIT 0
RAM 1	U25	6	17	EXECUTIVE MACRO RAM OUTPUT BIT 1

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
RAM 2	U25	10	17	EXECUTIVE MACRO RAM OUTPUT BIT 2
RAM 3	U25	8	17	EXECUTIVE MACRO RAM OUTPUT BIT 3
RAM 4	U27	6	17	EXECUTIVE MACRO RAM OUTPUT BIT 4
RAM 5	U27	4	17	EXECUTIVE MACRO RAM OUTPUT BIT 5
RAM 6	U27	2	17	EXECUTIVE MACRO RAM OUTPUT BIT 6
RAM 7	U27	12	17	EXECUTIVE MACRO RAM OUTPUT BIT 7
RAM SELECT 0-15	16S	2	18	SELECT RAM 0-15
RAM SELECT 16-31	16S	3	18	SELECT RAM 16-31
RD XD HI	U33	11	20	READ TRANSMIT DATA HIGH ORDER BITS NOT
RD XD LO	U33	10	20	READ TRANSMIT DATA LOW ORDER BITS NOT
READ DATA	2G	11	16	READ DATA NOT
READ DATA B	U43	3	20	READ DATA BUFFERED NOT
READ SWITCHES	11N	5	18	READ SWITCHES NOT
RECIRC BFRS	1C	8	15	RECIRCULATE BUFFERS
RECO 4	14Z	3	11	START OF RECOGNITION AND END OF ALPHABET OVERFLOW PULSE
RECO 4	14Z	4	11	START OF RECOGNITION AND END OF ALPHABET OVERFLOW PULSE NOT
RECOG	24U	8	11	RECOGNITION
RECOG	17U	2	11	RECOGNITION NOT
RECOG B	U15	3	10	RECOGNITION BUFFERED
RECO MX	18Y	8		RECOGNITION MULTIPLEXER
RECO MX	18X	9	11	RECOGNITION MULTIPLEXER NOT
RECRF	IOU	5		RECIRCULATE FLAG
REQ SRVC	16M	1	18	REQUEST FOR SERVICE
RESET	U1	2	5	RESET VIDEO
RESET ERROR CTRS	10Z	8	14	RESET ERROR COUNTERS NOT
RESET INC/DEC	15P	2	18	RESET INCREMENT/DECREMENT FLIP FLOPS NOT
RESET SWITCH	15P	7	18	RESET SWITCHES NOT
RESET V/H	U8	12	5	RESET VIDEO HOLD NOT
RFA0	13A	3	11	REFERENCE ALPHABET ADDRESS BIT 0
RFA1	13A	6	11	REFERENCE ALPHABET ADDRESS BIT 1

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
RFA2	13A	8	11	REFERENCE ALPHABET ADDRESS BIT 2
RFA3	13A	11	11	REFERENCE ALPHABET ADDRESS BIT 3
RFA 4	17A	3	11	REFERENCE ALPHABET ADDRESS BIT 4
RFA5	17A	6	11	REFERENCE ALPHABET ADDRESS BIT 5
RFA6	17A	8	11	REFERENCE ALPHABET ADDRESS BIT 6
RFA7	17A	11	11	REFERENCE ALPHABET ADDRESS BIT 7
RFA8	22A	2	11	REFERENCE ALPHABET ADDRESS BIT 8
RFA9	22A	4	11	REFERENCE ALPHABET ADDRESS BIT 9
$\overline{\text{RFA9}}$	U22	8	9	REFERENCE ALPHABET ADDRESS BIT 9 NOT
RFA10	22A	6	11	REFERENCE ALPHABET ADDRESS BIT 10
RFA11	22A	8	11	REFERENCE ALPHABET ADDRESS BIT 11
RFB 1	U16	9	9	REFERENCE ALPHABET BIT 1
RFB 2	U16	10	9	REFERENCE ALPHABET BIT 2
RFB 3	U16	11	9	REFERENCE ALPHABET BIT 3
RFB 4	U16	13	9	REFERENCE ALPHABET BIT 4
RFB 5	U16	14	9	REFERENCE ALPHABET BIT 5
RFB 6	U16	15	9	REFERENCE ALPHABET BIT 6
RFB 7	U16	16	9	REFERENCE ALPHABET BIT 7
RFB 8	U16	17	9	REFERENCE ALPHABET BIT 8
RFB 9	U17	9	9	REFERENCE ALPHABET BIT 9
RFB 10	U17	10	9	REFERENCE ALPHABET BIT 10
RFB 11	U17	11	9	REFERENCE ALPHABET BIT 11
RFB 12	U17	13	9	REFERENCE ALPHABET BIT 12
RFB 13	U17	14	9	REFERENCE ALPHABET BIT 13
RFB 14	U17	15	9	REFERENCE ALPHABET BIT 14
RFB 15	U17	16	9	REFERENCE ALPHABET BIT 15
RFB 16	U17	17	9	REFERENCE ALPHABET BIT 16
RFB 17	U18	9	9	REFERENCE ALPHABET BIT 17
RFB 18	U18	10	9	REFERENCE ALPHABET BIT 18
RFB 19	U18	11	9	REFERENCE ALPHABET BIT 19
RFB 20	U18	13	9	REFERENCE ALPHABET BIT 20
RFB 21	U18	14	9	REFERENCE ALPHABET BIT 21

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
RFB 22	U18	15	9	REFERENCE ALPHABET BIT 22
RFB 23	U18	16	9	REFERENCE ALPHABET BIT 23
RFB 24	U18	17	9	REFERENCE ALPHABET BIT 24
RFCS0	19A	11	11	REFERENCE ALPHABET CHIP SELECT BIT 0 NOT
RFCS1	19A	10	11	REFERENCE ALPHABET CHIP SELECT BIT 1 NOT
RFCS2	19A	9	11	REFERENCE ALPHABET CHIP SELECT BIT 2 NOT
RFCS3	19A	7	11	REFERENCE ALPHABET CHIP SELECT BIT 3 NOT
RFCS4	19A	6	11	REFERENCE ALPHABET CHIP SELECT BIT 4 NOT
RFCS5	19A	5	11	REFERENCE ALPHABET CHIP SELECT BIT 5 NOT
RFCS6	19A	4	11	REFERENCE ALPHABET CHIP SELECT BIT 6 NOT
RFCS7	19A	3	11	REFERENCE ALPHABET CHIP SELECT BIT 7 NOT
RFCS8	19A	2	11	REFERENCE ALPHABET CHIP SELECT BIT 8 NOT
RFCS9	19A	1	11	REFERENCE ALPHABET CHIP SELECT BIT 9 NOT
RH COMP	13W	8	11	REFERENCE HEIGHT COMPLETE
RH COMP	14U	5	11	REFERENCE HEIGHT COMPLETE NOT
RH LAMP	2D	4	1	READ HEAD LAMP
RH VIDEO	U24	11	5	READ HEAD VIDEO NOT
RIR	R/F	5	2	RIGHT PHOTOCELL EMITTER
RNDA 0	U39	4	10	REFERENCE START ADDRESS 0
RNDA 1	U39	5	10	REFERENCE START ADDRESS 1
RNDA 2	U39	6	10	REFERENCE START ADDRESS 2
RNDA 3	U39	7	10	REFERENCE START ADDRESS 3
RNDA 4	U39	8	10	REFERENCE START ADDRESS 4
RNDA 5	U39	9	10	REFERENCE START ADDRESS 5
RNDA 6	U39	10	10	REFERENCE START ADDRESS 6
RNDA 7	U39	11	10	REFERENCE START ADDRESS 7
RNDA 8	U38	4	10	REFERENCE START ADDRESS 8
RNDA 9	U38	5	10	REFERENCE START ADDRESS 9
RNDA 10	U38	6	10	REFERENCE START ADDRESS 10
RNDA 11	U38	7	10	REFERENCE START ADDRESS 11
ROV	U21	8	10	END OF ALPHABET COUNTER OVERFLOW

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN FIGURE A-		DEFINITION
ROW	U21	9	10	END OF ALPHABET COUNTER OVERFLOW NOT
RPC	R/F	7	2	RIGHT PHOTOCELL
RROV	U21	3	10	END OF ALPHABET COUNTER OVERFLOW DURING RECOGNITION
RROV	U21	4	10	END OF ALPHABET COUNTER OVERFLOW DURING RECOGNITION NOT
RSTART	U1	6	5	VIDEO STROBE NOT
RST CHAR DISP	15P	5	18	RESET LED CHARACTER DISPLAY NOT
RST KEYBD REG	15P	4	18	RESET KEYBOARD REGISTER NOT
R STOP	22S	8	2	RIGHT STOP
R STOP	2OL	2	2	RIGHT STOP NOT
RSTOP + LSTOP	21N	10	2	RIGHT STOP NOT OR LEFT STOP NOT
RST VERT POS	15P	6	18	RESET VERTICAL POSITION COUNTER NOT
RUN LAMP	2D	10	1	RUN LAMP ON
S0	24S	1	11	RECOGNITION SEQUENCER STATE 0 NOT
S2	24S	3	11	RECOGNITION SEQUENCER STATE 2 NOT
S 8	24S	9	11	RECOGNITION SEQUENCER STATE 8 NOT
S 1 0	24S	11	11	RECOGNITION SEQUENCER STATE 10 NOT
S 1 2	24S	14	11	RECOGNITION SEQUENCER STATE 12 NOT
S14	24S	16	11	RECOGNITION SEQUENCER STATE 14 NOT
SAMPLE	10S	3	6	SAMPLE
SAMPLE	12S	4	6	SAMPLE NOT
SBRTN	U7	8	17	SUBROUTINE NOT
SCAN SYNC	7W	3	6	SCAN SYNC
SCCF	10S	5	6	SCAN COUNTER CLOCKING FLAG
SCCLK	12R	6	6	SCAN COUNTER CLOCK
SCCLK	1T	8	6	SCAN COUNTER CLOCK NOT
SEL 0	13Y	9	11	NOT USED
SEL 1	13Y	5	11	NOT USED
SELECT KYBD	1D	6	15	SELECT KEYBOARD NOT
SET CH DISP1	15M	6	18	SET LED CHARACTER # 1 DISPLAY NOT

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
SET CH DISP2	15M	7	18	SET LED CHARACTER # 2 DISPLAY NOT
SET CH DISP3	15M	9	18	SET LED CHARACTER # 3 DISPLAY NOT
SET CPU STATUS	15L	4	18	SET CPU STATUS NOT
SET DEC	15M	3	18	SET DECREMENT FLIP FLOP NOT
SET INC	15M	2	18	SET INCREMENT FLIP FLOP NOT
SET MASK	24S	4	11	SET MASK NOT
SET REQ FOR SERV CPU	15M	5	18	SET REQUEST FOR SERVICE CPU NOT
SHFT BFRS	1C	11	15	SHIFT BUFFERS NOT
SHIFT OUT BUF	15L	2	18	SERIALLY SHIFT OUT BUFFERS NOT
SHIFT XYSR	24U	4	11	SHIFT XY SHIFT REGISTER
SHIFT XYSR	24U	6	11	SHIFT XY SHIFT REGISTERS NOT
SHORT UNK	6W	5	14	SHORT UNKNOWN CHARACTER
SHSR2	15S	7	18	SHIFT SHIFT REGISTER 2 NOT
SIMV	11X	5	18	SIMULATED VIDEO (TEST SET) NOT
SINGLE CYCLE	11V	9	11	SINGLE CYCLE NOT (DIAGNOSTIC)
S JUST	9U	6	6	BOTTOM JUSTIFICATION MODE NOT
SPACE SELECT	14X	4	15	SPACE SELECT
SPACE SELECT	14X	3	15	SPACE SELECT NOT
SPEC IOP	U39	15	20	SPECIAL INPUT/OUTPUT PULSE
SPP	21Z	10	11	SPACE CIRCUIT GATE
SRADD 23	14Z	6	7	SIMULATED CHARACTER HEIGHT
SR DATA	25N	8	6	SHIFT REGISTER DATA
SR DATA	25N	9	6	SHIFT REGISTER DATA NOT
SRECO	14Z	2	11	SIMULATED RECOGNITION
SRECO	14Z	1	11	SIMULATED RECOGNITION NOT
SRECO PROM TEST	11W	12	7	SIMULATED CHARACTER TEST
SSHTS	15L	3	18	STAGE SHIFTS (BY PROGRAM) NOT
STAND	14S	11	11	STANDARD
STAND	14S	12	11	STANDARD NOT
START	U2	8	23	START
START RECOG	14Z	11	11	START RECOGNITION
START RECOG	14Z	10	11	START RECOGNITION NOT
START RECO MX	10W	9	11	START RECOGNITION MULTIPLEXER NOT
STB 0	18M	1	15	STROBE 0 NOT

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
STB 1	18M	2	15	STROBE 1 NOT
STB 2	18M	3	15	STROBE 2 NOT
STB 3	18M	4	15	STROBE 3 NOT
STB 11	15S	4	18	STROBE 11 NOT
STBF	3U	8	6	SPACE TOO BIG FLAG NOT
STEP DN	10X	5	14	STEP WINDOW DOWN
STEP UP	10X	9	14	STEP WINDOW UP
STOP	U2	6	23	STOP
STPMF	9U	2	6	START POSITION MODE FLAG NOT
STPMS	4R	8	6	SET POSITION MODE START NOT
STROBE 7	15L	9	18	PULSE STROBE INSTRUCTION 7 NOT
SUHT COMP	22Z	6	7	SIMULATED CHARACTER HEIGHT COMPLETE
SWNDO	5N	8	6	SCAN WINDOW NOT
SYS RESET	19N	10	1	SYSTEM RESET
SYS RESET	14S	6	18	SYSTEM RESET NOT
SYS RESET B	19N	10	1	SYSTEM RESET NOT BUFFERED
TALL UNK	6W	9	14	TALL UNKNOWN
TBS	1P	6	6	TOP BIT STROBE NOT
TCHF (BUF)	18N	7	15	TOUCHING CHARACTER FLAG BUFFERED
TCSF	10U	2	6	TENTATIVE CHARACTER START FLAG
TENT PAPER PRES	U2	11	5	TENTATIVE PAPER PRESENT
TEST	U19	5	5	TEST
TEST	U3	3	17	TEST INSTRUCTION NOT
TOUCHING CHARACTER	5V	12	14	TOUCHING CHARACTER
TOUCHING CHARACTER	9Z	10	14	TOUCHING CHARACTER NOT
TPPR	2D	12	1	GATED PAPER PRESENT
TSZF	3R	5		TOP SPACE ZERO FLAG
TWNDO	4M	6	6	TOP OF SCAN WINDOW
UB 1	32N	1		UNKNOWN RAM INPUT BIT 1
UB 2	32N	4	6	UNKNOWN RAM INPUT BIT 2
UB 3	32N	7	6	UNKNOWN RAM INPUT BIT 3
UB 4	32N	13		UNKNOWN RAM INPUT BIT 4
UB 5	31N	1	6	UNKNOWN RAM INPUT BIT 5
UB 6	31N	4	6	UNKNOWN RAM INPUT BIT 6
UB 7	31N	7		UNKNOWN RAM INPUT BIT 7
UB 8	31N	13	6	UNKNOWN RAM INPUT BIT 8
UB 9	30N	1	6	UNKNOWN RAM INPUT BIT 9
UB 10	30N	4		UNKNOWN RAM INPUT BIT 10
UB 11	30N	7	6	UNKNOWN RAM INPUT BIT 11
UB 12	30N	13	6	UNKNOWN RAM INPUT BIT 12

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
I 13	29N	1	6	UNKNOWN RAM INPUT BIT 13
I 14	29N	4	6	UNKNOWN RAM INPUT BIT 14
I 15	29N	7		UNKNOWN RAM INPUT BIT 15
I 16	29N	13	6	UNKNOWN RAM INPUT BIT 16
I 17	28N	1	6	UNKNOWN RAM INPUT BIT 17
I 18	28N	4	6	UNKNOWN RAM INPUT BIT 18
I 19	28N	7	6	UNKNOWN RAM INPUT BIT 19
I 20	28N	13	6	UNKNOWN RAM INPUT BIT 20
I 21	27N	1	6	UNKNOWN RAM INPUT BIT 21
I 22	27N	4		UNKNOWN RAM INPUT BIT 22
I 23	27N	7	6	UNKNOWN RAM INPUT BIT 23
I 24	27N	13	6	UNKNOWN RAM INPUT BIT 24
COMP	13W	6	11	UNKNOWN HEIGHT COMPLETE
$\overline{\text{COMP}}$	14U	9	11	UNKNOWN HEIGHT COMPLETE NOT
LIM	14T	8	11	UNKNOWN HEIGHT LIMIT NOT
REC FLG	7Z	5		UNRECOGNIZED FLAG
$\overline{\text{REC FLG}}$	7Z	6	14	UNRECOGNIZED FLAG NOT
REC FLG BUF	18N	4	15	UNRECOGNIZED FLAG BUFFERED
B 1	29R	2	7	UNKNOWN RAM OUTPUT BIT 1
B 2	29	4	7	UNKNOWN RAM OUTPUT BIT 2
B 3	29R	12	7	UNKNOWN RAM OUTPUT BIT 3
B 4	29R	10		UNKNOWN RAM OUTPUT BIT 4
B 5	29R	8	7	UNKNOWN RAM OUTPUT BIT 5
B 6	29R	6	7	UNKNOWN RAM OUTPUT BIT 6
B 7	29P	2	7	UNKNOWN RAM OUTPUT BIT 7
B 8	29P	12	7	UNKNOWN RAM OUTPUT BIT 8
B 9	29P	4	7	UNKNOWN RAM OUTPUT BIT 9
B 10	29P	6	7	UNKNOWN RAM OUTPUT BIT 10
B 11	29P	8	7	UNKNOWN RAM OUTPUT BIT 11
B 12	29P	10	7	UNKNOWN RAM OUTPUT BIT 12
B 13	27R	2	7	UNKNOWN RAM OUTPUT BIT 13
B 14	27R	4	7	UNKNOWN RAM OUTPUT BIT 14
B 15	27R	12		UNKNOWN RAM OUTPUT BIT 15
B 16	27R	10	7	UNKNOWN RAM OUTPUT BIT 16
B 17	27R	6	7	UNKNOWN RAM OUTPUT BIT 17
B 18	27R	8	7	UNKNOWN RAM OUTPUT BIT 18
B 19	27P	2	7	UNKNOWN RAM OUTPUT BIT 19
B 20	27P	12	7	UNKNOWN RAM OUTPUT BIT 20
B 21	27P	4	7	UNKNOWN RAM OUTPUT BIT 21
B 22	27P	6	7	UNKNOWN RAM OUTPUT BIT 22
B 23	27P	8	7	UNKNOWN RAM OUTPUT BIT 23
B 24	27P	10	7	UNKNOWN RAM OUTPUT BIT 24

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
URMA 1	23R	3	7	UNKNOWN RAM ADDRESS BIT 1
URMA 2	23R	2	7	UNKNOWN RAM ADDRESS BIT 2
URMA 3	23R	6	7	UNKNOWN RAM ADDRESS BIT 3
URMA 4	23R	7	7	UNKNOWN RAM ADDRESS BIT 4
URMA 5	23P	3	7	UNKNOWN RAM ADDRESS BIT 5
URMA 6	23P	2	7	UNKNOWN RAM ADDRESS BIT 6
VA0	2M	9		VIDEO ADDRESS 0
VA1	2M	10	6	VIDEO ADDRESS 1
VA2	2M	14	6	VIDEO ADDRESS 2
VA3	2M	1	6	VIDEO ADDRESS 3
VA4	4M	9	6	VIDEO ADDRESS 4
VA5	4M	10	6	VIDEO ADDRESS 5
VA6	4M	14		VIDEO ADDRESS 6
VA7	4M	1	6	VIDEO ADDRESS 7
VDA 1	28L	3	1	VERTICAL DIGITAL TO ANALOG BIT 1
VDA 2	28L	6	1	VERTICAL DIGITAL TO ANALOG BIT 2
VDA 3	28L	8	1	VERTICAL DIGITAL TO ANALOG BIT 3
VDA 4	28L	11	1	VERTICAL DIGITAL TO ANALOG BIT 4
VDA 5	28K	3	1	VERTICAL DIGITAL TO ANALOG BIT 5
VDA 6	28K	6	1	VERTICAL DIGITAL TO ANALOG BIT 6
VDA 7	28K	8	1	VERTICAL DIGITAL TO ANALOG BIT 7
VDA 8	28K	11	1	VERTICAL DIGITAL TO ANALOG BIT 8
VEN 1	2K	1		VERTICAL ENCONDER PHASE 1
$\overline{\text{VEN 1}}$	2K	2	1	VERTICAL ENCODER PHASE 1 NOT
VEN 1B	4A	2	1	VERTICAL ENCODER PHASE 1 BUFFERED
VEN 2	2K	3	1	VERTICAL ENCODER PHASE 2
$\overline{\text{VEN 2}}$	2K	4	1	VERTICAL ENCODER PHASE 2 NOT
VEN 2B	4A	4	1	VERTICAL ENCODER PHASE 2 BUFFERED
$\overline{\text{VER DN}}$	1K	6	1	VERTICAL DOWN PULSE NOT
$\overline{\text{VER UP}}$	1K	3	1	VERTICAL UP PULSE NOT
VMF1	1N	3	6	VERTICALLY MISALIGNED SIGNAL 1

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
VMF2	1N	6	6	VERTICALLY MISALIGNED SIGNAL 2
VP CL INH	19N	8	1	VERTICAL POSITION COUNTER CLEAR INHIBIT NOT
V POS	20T	2	1	VERTICAL POSITION NOT
VSA±	30A	10	1	VERTICAL SERVO AMPLIFIED VOLTAGE ±
V STOP	20T	1	1	VERTICAL STOP NOT
VTC±	29A	10	1	VERTICAL TACH ±
WE	U37	14	10	WRITE RECO RAMS NOT
WIDE UNK	3V	9	14	WIDE UNKNOWN
WRITE ENB	U5	6	5	WRITE ENABLE
WRITE ENABLE (URAM)	25N	2	6	UNKNOWN RAM WRITE ENABLE NOT
WRITE READ 1	U26	9	5	WRITE FRAME BUFFER 2 READ 1 NOT
WRITE READ 2	U26	4	5	WRITE FRAME BUFFER 1 READ 2 NOT
WRIT XD HI	U33	13	20	WRITE EXTERNAL DATA HIGH ORDER NOT
WRIT XD LO	U33	12	20	WRITE EXTERNAL DATA LOW ORDER NOT
X1	29U	9	12	X SHIFT REGISTER SAMPLE POINT 1
X2	27V	5	12	X SHIFT REGISTER SAMPLE POINT 2
X3	27V	9	12	X SHIFT REGISTER SAMPLE POINT 3
X4	27X	9	12	X SHIFT REGISTER SAMPLE POINT 4
X5	28X	5	12	X SHIFT REGISTER SAMPLE POINT 5
X7	27Z	9	12	X SHIFT REGISTER SAMPLE POINT 7
X9	28Z	9	12	X SHIFT REGISTER SAMPLE POINT 9
X11	28V	9	12	X SHIFT REGISTER SAMPLE POINT 11
X1	29U	7	12	X SHIFT REGISTER SAMPLE POINT 1 NOT
X2	27V	6	12	X SHIFT REGISTER SAMPLE POINT 2 NOT

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
$\overline{X3}$	27V	8	12	X SHIFT REGISTER SAMPLE POINT 3 NOT
$\overline{X4}$	27X	7	12	X SHIFT REGISTER SAMPLE POINT 4 NOT
$\overline{X5}$	28X	6	12	X SHIFT REGISTER SAMPLE POINT 5 NOT
$\overline{X6}$	28X	8	12	X SHIFT REGISTER SAMPLE POINT 6 NOT
$\overline{X7}$	27Z	7	12	X SHIFT REGISTER SAMPLE POINT 7 NOT
$\overline{X8}$	28Z	6	12	X SHIFT REGISTER SAMPLE POINT 8 NOT
$\overline{X9}$	28Z	8	12	X SHIFT REGISTER SAMPLE POINT 9 NOT
$\overline{X10}$	28V	6	12	X SHIFT REGISTER SAMPLE POINT 10 NOT
$\overline{X11}$	28V	8	12	X SHIFT REGISTER SAMPLE POINT 11 NOT
$\overline{X12}$	29Z	6	12	X SHIFT REGISTER SAMPLE POINT 12 NOT
XADD 0	U25	3	20	DATA ADDRESS BIT 0
XADD 1	U25	2	20	DATA ADDRESS BIT 1
XADD 2	U25	6	20	DATA ADDRESS BIT 2
XADD 3	U25	7	20	DATA ADDRESS BIT 3
XADD 4	U21	3	20	DATA ADDRESS BIT 4
XADD 5	U21	2	20	DATA ADDRESS BIT 5
XADD 6	U21	6	20	DATA ADDRESS BIT 6
XADD 7	U21	7	20	DATA ADDRESS BIT 7
XADD 8	U17	3	20	DATA ADDRESS BIT 8
XADD 9	U17	2	20	DATA ADDRESS BIT 9
XADD 10	U17	6	20	DATA ADDRESS BIT 10
XADD 11	U17	7	20	DATA ADDRESS BIT 11
XDO 0	U11	3	20	DATA OUT BIT 0
XDO 1	U11	4	20	DATA OUT BIT 1
XDO 2	U11	5	20	DATA OUT BIT 2
XDO 3	U11	6	20	DATA OUT BIT 3
XDO 4	U7	3	20	DATA OUT BIT 4
XDO 5	U7	4	20	DATA OUT BIT 5
XDO 6	U7	5	20	DATA OUT BIT 6
XDO 7	U7	6	20	DATA OUT BIT 7
XDO 8	U1	3	20	DATA OUT BIT 8
XDO 9	U1	4	20	DATA OUT BIT 9
XDO 10	U1	5	20	DATA OUT BIT 10

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
$\overline{Y7}$	32Y	7	12	Y SHIFT REGISTER SAMPLE POINT 7 NOT
$\overline{Y8}$	32Z	6	12	Y SHIFT REGISTER SAMPLE POINT 8 NOT
$\overline{Y9}$	32Z	8	12	Y SHIFT REGISTER SAMPLE POINT 9 NOT
$\overline{Y10}$	31U	6	12	Y SHIFT REGISTER SAMPLE POINT 10 NOT
$\overline{Y11}$	31U	8	12	Y SHIFT REGISTER SAMPLE POINT 11 NOT
$\overline{Y12}$	29Z	8	12	Y SHIFT REGISTER SAMPLE POINT 12 NOT
ZA0	U34	3	10	CLEAR RAM ADDRESS BIT 0
ZA1	U34	2	10	CLEAR RAM ADDRESS BIT 1
ZA2	U34	6	10	CLEAR RAM ADDRESS BIT 2
ZA3	U34	7	10	CLEAR RAM ADDRESS BIT 3
ZA4	U35	3	10	CLEAR RAM ADDRESS BIT 4
ZA5	U35	2	10	CLEAR RAM ADDRESS BIT 5
1E 0	21V	2	13	ERROR COUNTER ONE BIT 0
1E 1	21V	5	13	ERROR COUNTER ONE BIT 1
1E 2	21V	7	13	ERROR COUNTER ONE BIT 2
1E 3	21V	10	13	ERROR COUNTER ONE BIT 3
1E 4	21V	12	13	ERROR COUNTER ONE BIT 4
1E 5	21V	15	13	ERROR COUNTER ONE BIT 5
$\overline{1\ SRSHT}$	24N	8	6	ONE SHIFT REGISTER SHIFT NOT
2E 0	21W	2	13	ERROR COUNTER TWO BIT 0
2E 1	21W	5	13	ERROR COUNTER TWO BIT 1
2E 2	21W	7	13	ERROR COUNTER TWO BIT 2
2E 3	21W	10	13	ERROR COUNTER TWO BIT 3
2E 4	21W	12	13	ERROR COUNTER TWO BIT 4

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
2E 5	21W	15	13	ERROR COUNTER TWO BIT 5
3E 0	21X	2	13	ERROR COUNTER THREE BIT 0
3E 1	21X	5	13	ERROR COUNTER THREE BIT 1
3E 2	21X	7	13	ERROR COUNTER THREE BIT 2
3E 3	21X	10	13	ERROR COUNTER THREE BIT 3
3E 4	21X	12	13	ERROR COUNTER THREE BIT 4
3E 5	21X	15	13	ERROR COUNTER THREE BIT 5
4E 0	21Y	2	13	ERROR COUNTER FOUR BIT 0
4E 1	21Y	5	13	ERROR COUNTER FOUR BIT 1
4E 2	21Y	7	13	ERROR COUNTER FOUR BIT 2
4E 3	21Y	10	13	ERROR COUNTER FOUR BIT 3
4E 4	21Y	12	13	ERROR COUNTER FOUR BIT 4
4E 5	21Y	15	13	ERROR COUNTER FOUR BIT 5
5E 0	22V	2	13	ERROR COUNTER FIVE BIT 0
5E 1	22V	5	13	ERROR COUNTER FIVE BIT 1
5E 2	22V	7	13	ERROR COUNTER FIVE BIT 2
5E 3	22V	10	13	ERROR COUNTER FIVE BIT 3
5E 4	22V	12	13	ERROR COUNTER FIVE BIT 4
5E 5	22V	15	13	ERROR COUNTER FIVE BIT 5
6E 0	22W	2	13	ERROR COUNTER SIX BIT 0
6E 1	22W	5	13	ERROR COUNTER SIX BIT 1
6E 2	22W	7	13	ERROR COUNTER SIX BIT 2
6E 3	22W	10	13	ERROR COUNTER SIX BIT 3

Table 6-6

Mnemonic Signal Listing (continued)

SIGNAL	COMP	PIN	FIGURE A-	DEFINITION
6E 4	22W	12	13	ERROR COUNTER SIX BIT 4
6E 5	22W	15	13	ERROR COUNTER SIX BIT 5
7E 0	22X	2	13	ERROR COUNTER SEVEN BIT 0
7E 1	22X	5	13	ERROR COUNTER SEVEN BIT 1
7E 2	22X	7	13	ERROR COUNTER SEVEN BIT 2
7E 3	22X	10	13	ERROR COUNTER SEVEN BIT 3
7E 4	22X	12	13	ERROR COUNTER SEVEN BIT 4
7E 5	22X	15	13	ERROR COUNTER SEVEN BIT 5
8E 0	22Y	2	13	ERROR COUNTER EIGHT BIT 0
8E 1	22Y	5	13	ERROR COUNTER EIGHT BIT 1
8E 2	22Y	7	13	ERROR COUNTER EIGHT BIT 2
8E 3	22Y	10	13	ERROR COUNTER EIGHT BIT 3
8E 4	22Y	12	13	ERROR COUNTER EIGHT BIT 4
8E 5	22Y	15	13	ERROR COUNTER EIGHT BIT 5

SUMMARY OF SCANNED TEXT FLOW THROUGH O.C.R.

Item	Subject	Schem. Diag.
(1)	Analog Video	(A-4)
(2)	Digitized Video	(A-5)
(3)	Windowed Video	(A-5,6)
(4)	Matrix Assembled and Analyzed	(A-6)
(5)	Stored in URAM	(A-7)
(6)	Compared Against the Reference Alphabet in the X-Y Shift Registers	(A-12)
(7)	Errors Generated	(A-12)
(8)	Lowest Error Stored	(A-13)
(9)	Best Identified Character ASCII Code Latched	(A-14)
(10)	B.I.D. put into the Line Buffer	(A-15,16)
(11)	B.I.D. goes to Executive Macro Compare MUX	(A-17,18)
(12)	Executive Macro Accumulator	(A-17,18)
(13)	Executive Macro RAMs	(A-17,18)
(14)	Core Memory (Code Converted)	(A-20)
(15)	External Data Output Latch	(A-20)
(16)	Interface Electronics	(A-16)
(17)	External Devide (MOD 40 TTY)	

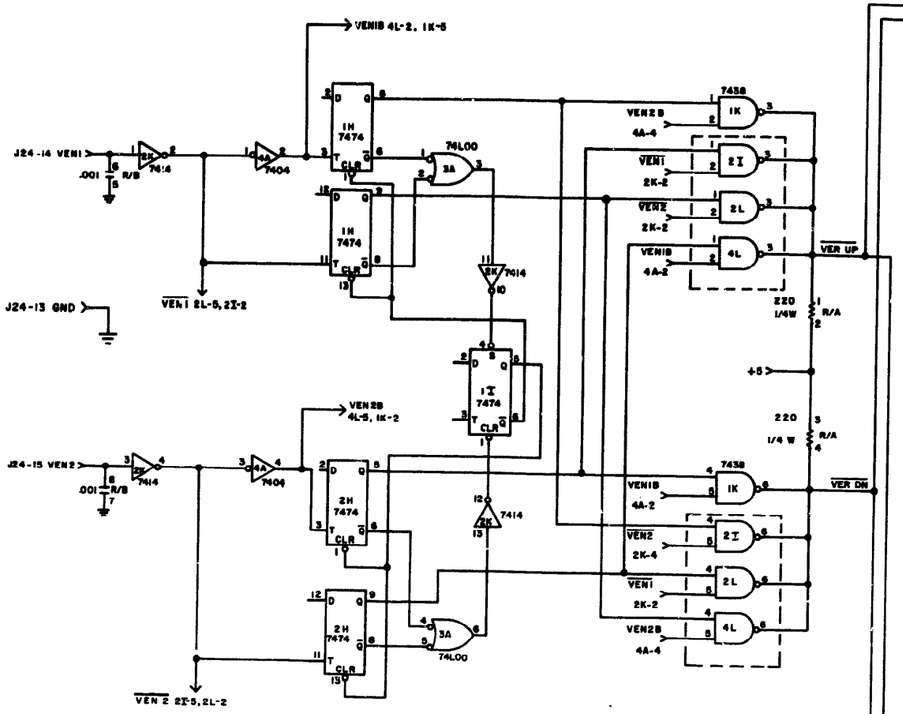
APPENDIX A

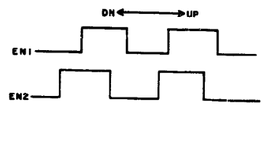
Logic Schematic Diagrams

Wiring Diagrams

Reference Photographs

VERTICAL ENCODER UP & DOWN PULSE GENERATOR

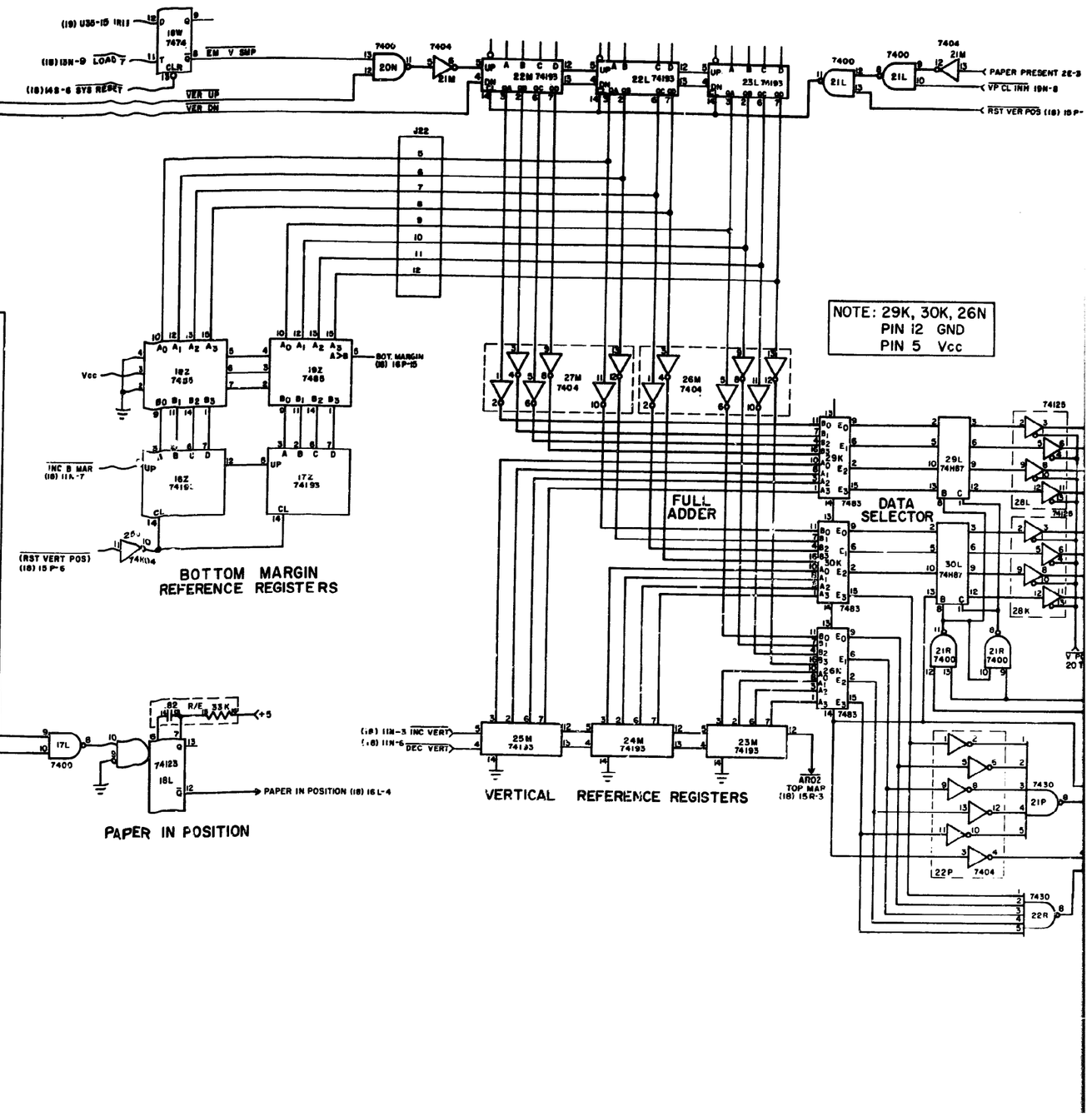




UP	
EN1	EN2
0	↑
↑	1
1	↓
↓	0

DN	
EN1	EN2
↓	1
0	↓
↑	0
1	↑

VERTICAL POSITION COUNTER



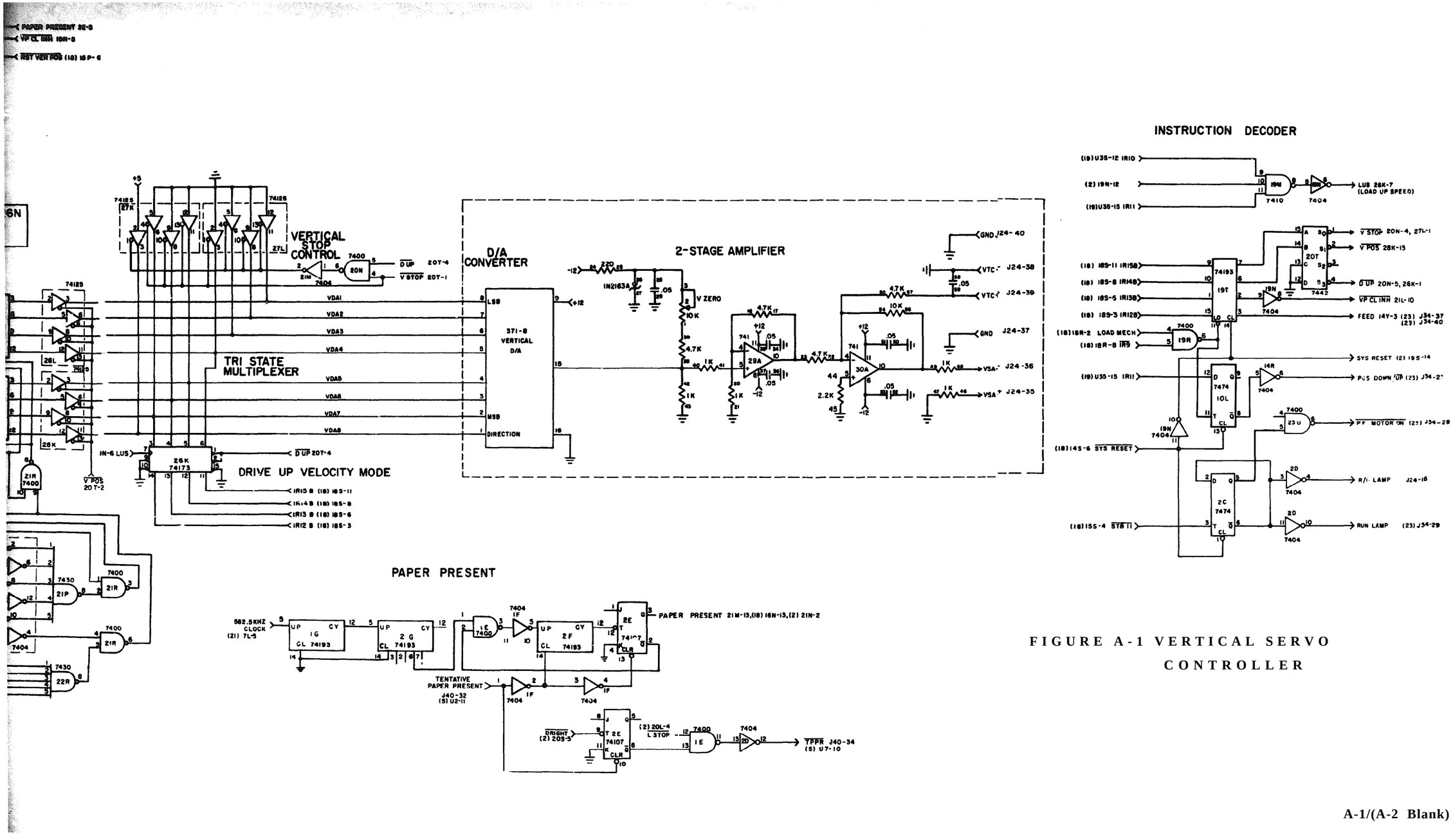


FIGURE A-1 VERTICAL SERVO CONTROLLER

HORIZONTAL ENCODER UP & DOWN PULSE GENERATOR

HENI J24-5 .001 R/B
HENI 4L-10, 1K-15
HENI 2L-10, 2L-13
J24-4 GND
HEN2 J24-6 .001 R/B
HEN2B 3L-3, 4L-13, 1K-10
HEN2 2L-13, 2L-10
HENIB 4A-6
HENI 2K-6
HEN2 2K-6
HEN2B 4A-6
HENIB 4A-6
HEN2 2K-6
HENT 2K-6
HEN2B 4A-6
220 1/4W R/A
+5V
HOR. DN.
HOR. UP
(19) U35-7 IR8
(18) 13N-9 LOAD 7
(18) 14S-6 SYS RESET
EM HSMP
J03-9 (TEST)
ENCODER SAMPLE
12U-9(6) 3Y-10 (6)
562.5KHz 7L-5 (21)
82 R/E 33K
HEAD IN MCTION 16L-3(18)
(18) 11N-4 INC HORZ
ARO 3 (18) 15R-4
(18) 16N-15 LT/RT MARG
THE 8 OUTPUTS GO TO J21
FULL ADDER
DATA SELECTOR
HORIZONTAL REFERENCE REGISTER
HEAD IN MOTION

UP

ENI	EN2
0	↑
↑	1
1	↓
↓	0

DN

ENI	EN2
↓	1
0	↓
↑	0
1	↑

INSTRUCTION DECODERS

(18) 18R-2 LOAD MECH
(19) U35-7 IR8
(19) U35-10 IR9
(1) 19M-10
(18) 18R-12 IRIO
(19) U35-15 IR11
LRS 31K-7
(19) U35-12 IRIO
(18) 18R-6 IRII
LLS 31L-7
(18) 18S-11 IR15B
(18) 18S-8 IR14B
(18) 18S-6 IR13B
(18) 18S-3 IR12B
(18) 18R-2 LOAD MECH
(18) 18R-4 IR8
(1) 19N-10 SYS RESET

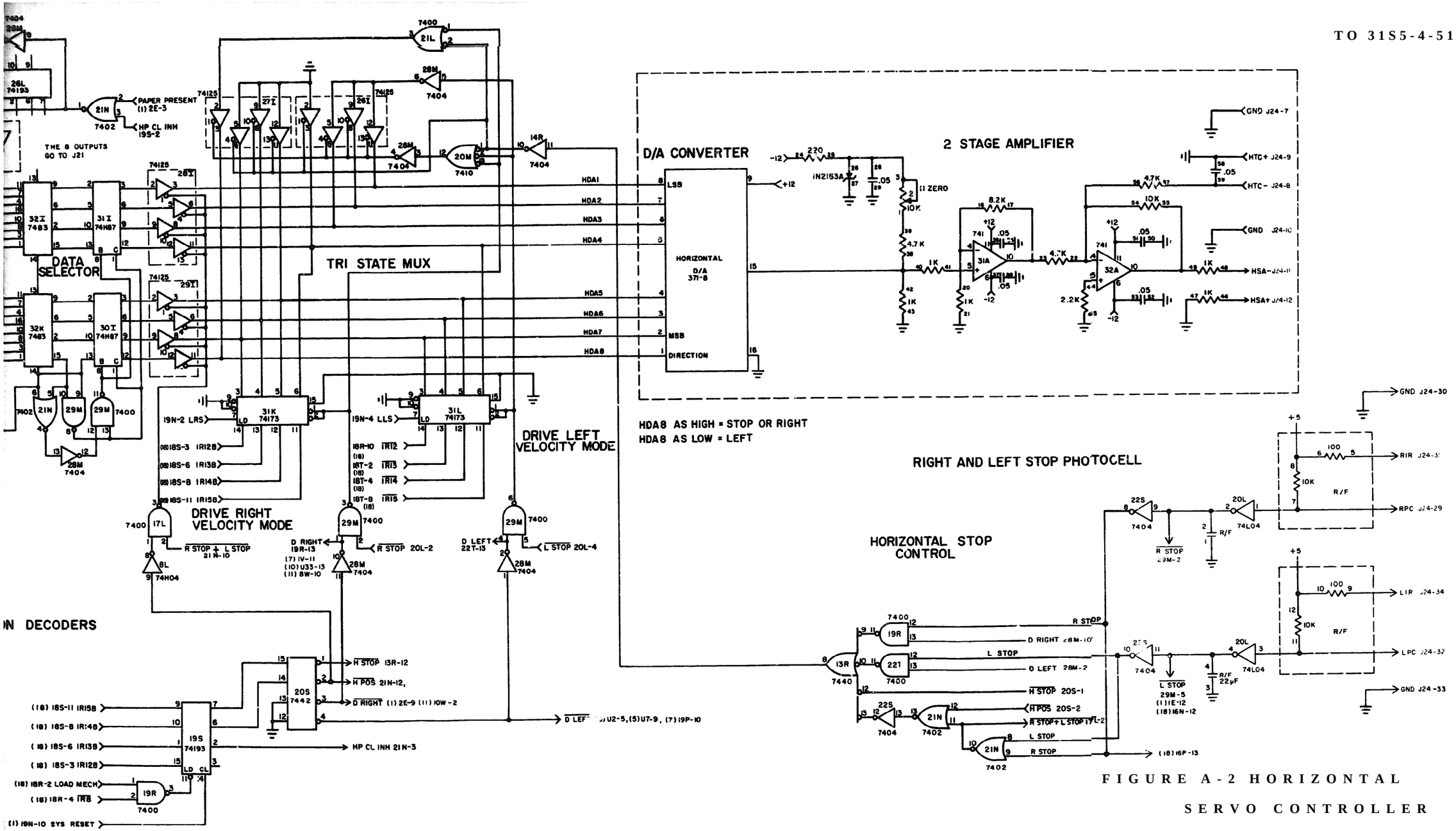
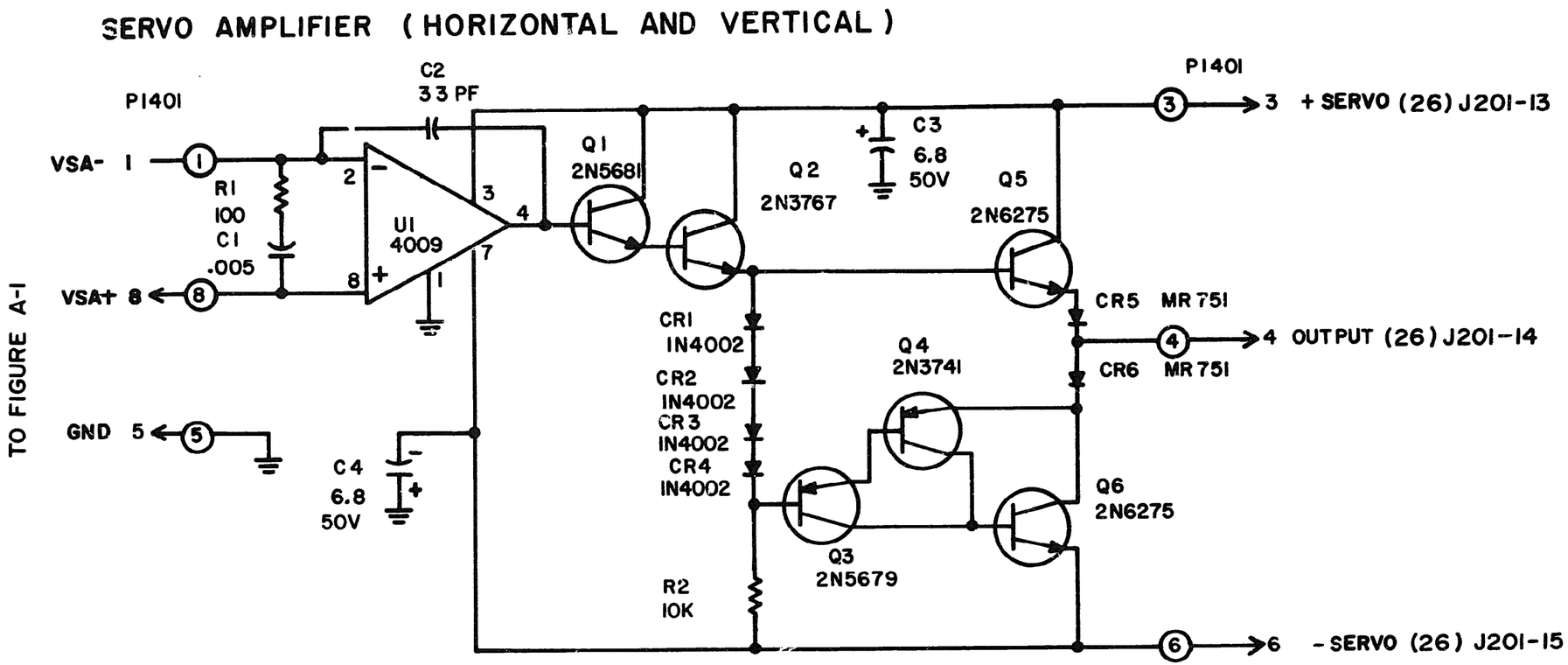


FIGURE A-2 HORIZONTAL SERVO CONTROLLER



NOTES

1. RESISTORS ARE OHMS, 1/4W. CAPACITORS ARE UF.
2. PARTIAL REF. DESIG. ARE SHOWN FOR COMPLETE DESIG. PREFIX WITH 1450 (EXAMPLE R1=R1451)

FIGURE A-3

SERVO POWER AMPLIFIER

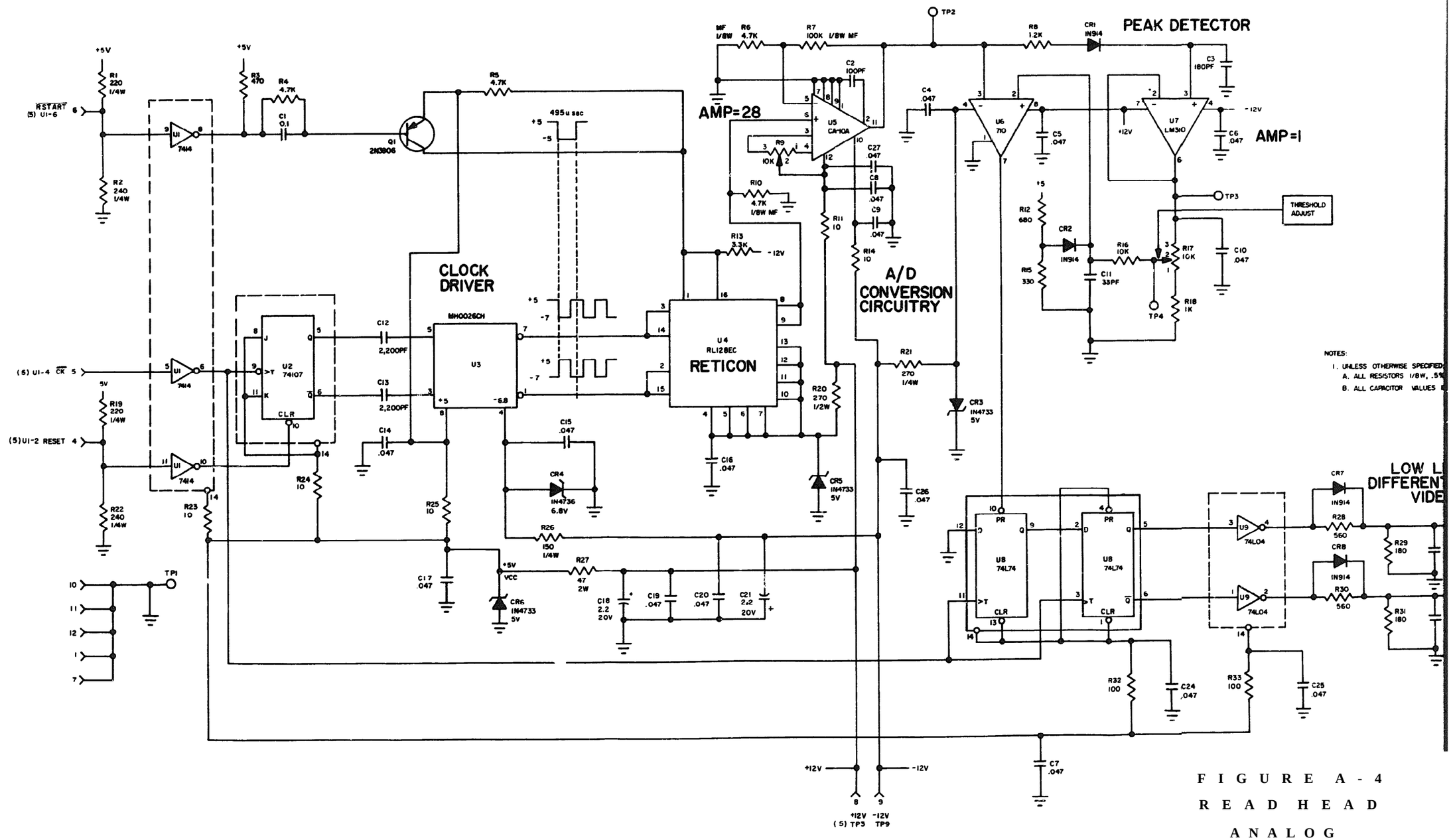
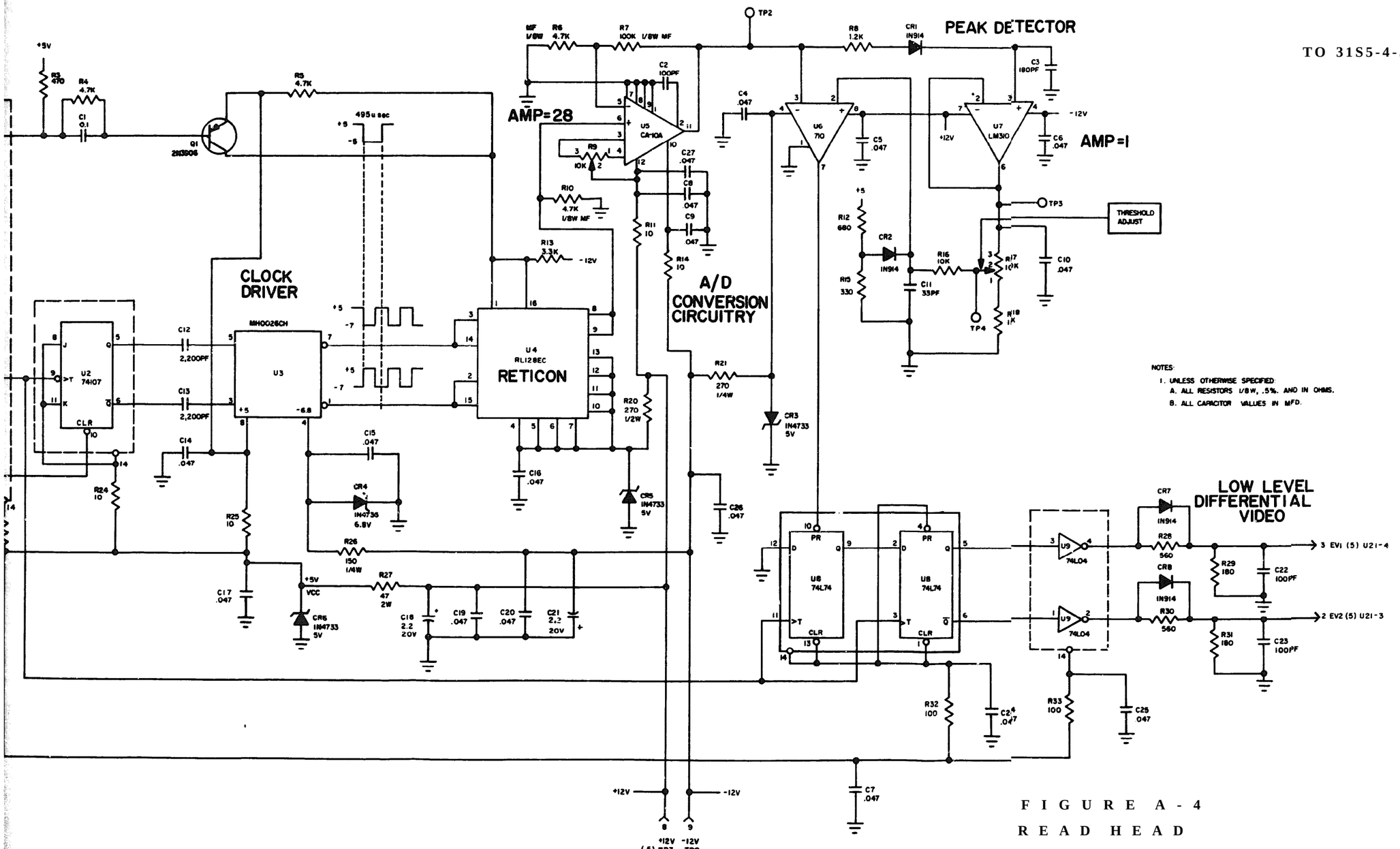


FIGURE A-4

READ HEAD

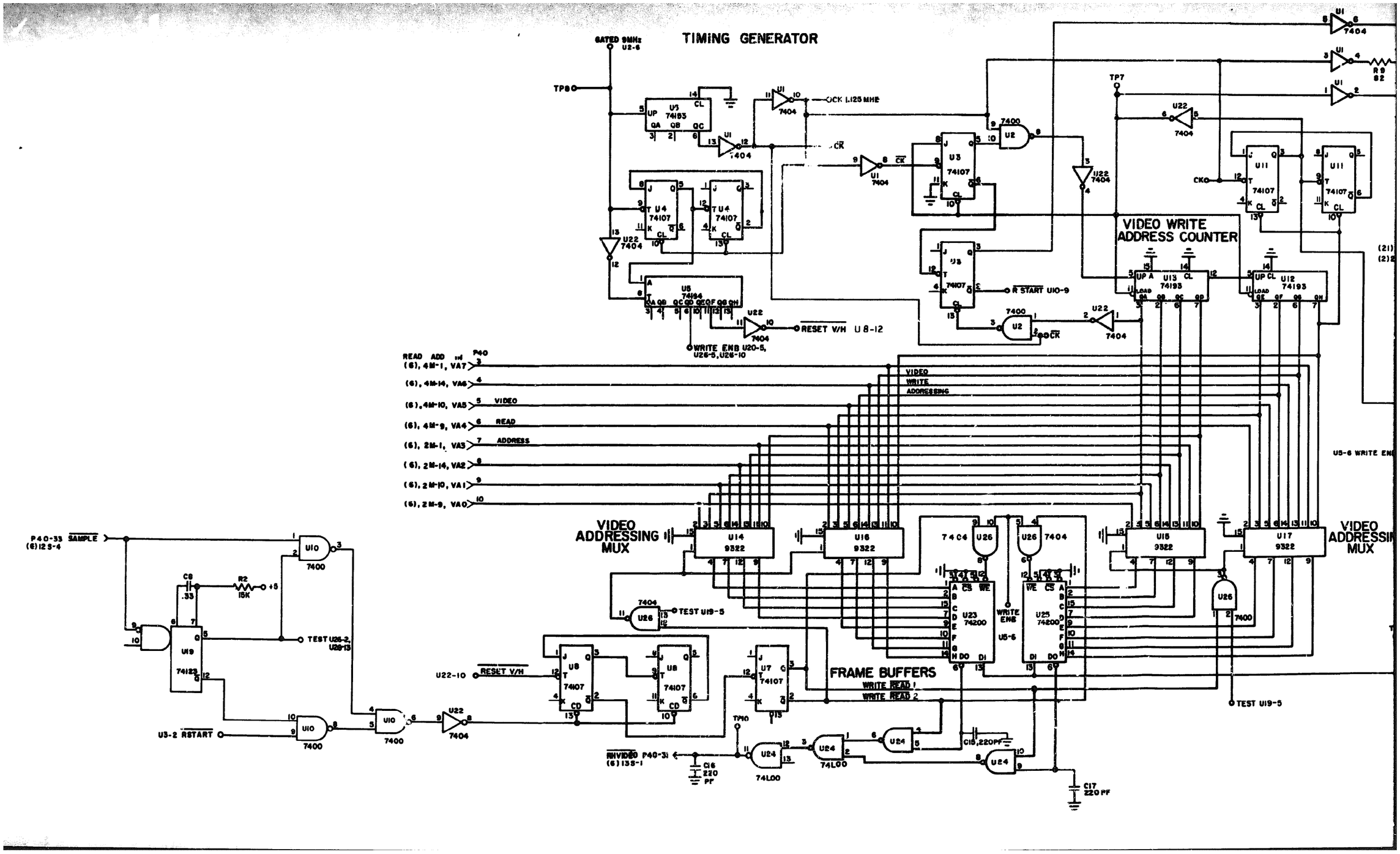
ANALOG

TO 31S5-4-516-1



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS 1/8W, .5%, AND IN OHMS.
   B. ALL CAPACITOR VALUES IN MFD.

FIGURE A-4
READ HEAD
ANALOG


TIMING GENERATOR
GATED 9MHz U2-6
TP8
U3 74193
UP QA QB QC
CL
7404
CK 1.125 MHz
CK
7400
U2
U4 74107
U22 7404
U5 74164
WRITE ENB U20-5, U26-5, U26-10
RESET V/H U 8-12
U3 74107
R START U10-9
VIDEO WRITE ADDRESS COUNTER
TP7
CK0
U11 74107
U13 74193
U12 74193
(21)
(2)2
READ ADD ml (6), 4M-1, VA7
(6), 4M-14, VA6
(6), 4M-10, VA5
(6), 4M-9, VA4
(6), 2M-1, VA3
(6), 2M-14, VA2
(6), 2M-10, VA1
(6), 2M-9, VA0
VIDEO
READ
ADDRESS
VIDEO WRITE ADDRESSING
U5-6 WRITE EN
VIDEO ADDRESSING MUX
U14 9322
U16 9322
U18 9322
U17 9322
U26 7404
U23 74200
U25 74200
WRITE ENB U5-6
TEST U19-5
FRAME BUFFERS
WRITE READ 1
WRITE READ 2
P40-33 SAMPLE (6)125-4
U10 7400
U19 74123
C8 .33
R2 15K
+5
TEST U26-2, U29-13
U3-2 RSTART
U22-10 RESET V/H
U8 74107
U7 74107
TP10
RHVIDEO P40-31 (6)135-1
C16 220 PF
U24 74L00
C15, 220PF
C17 220 PF

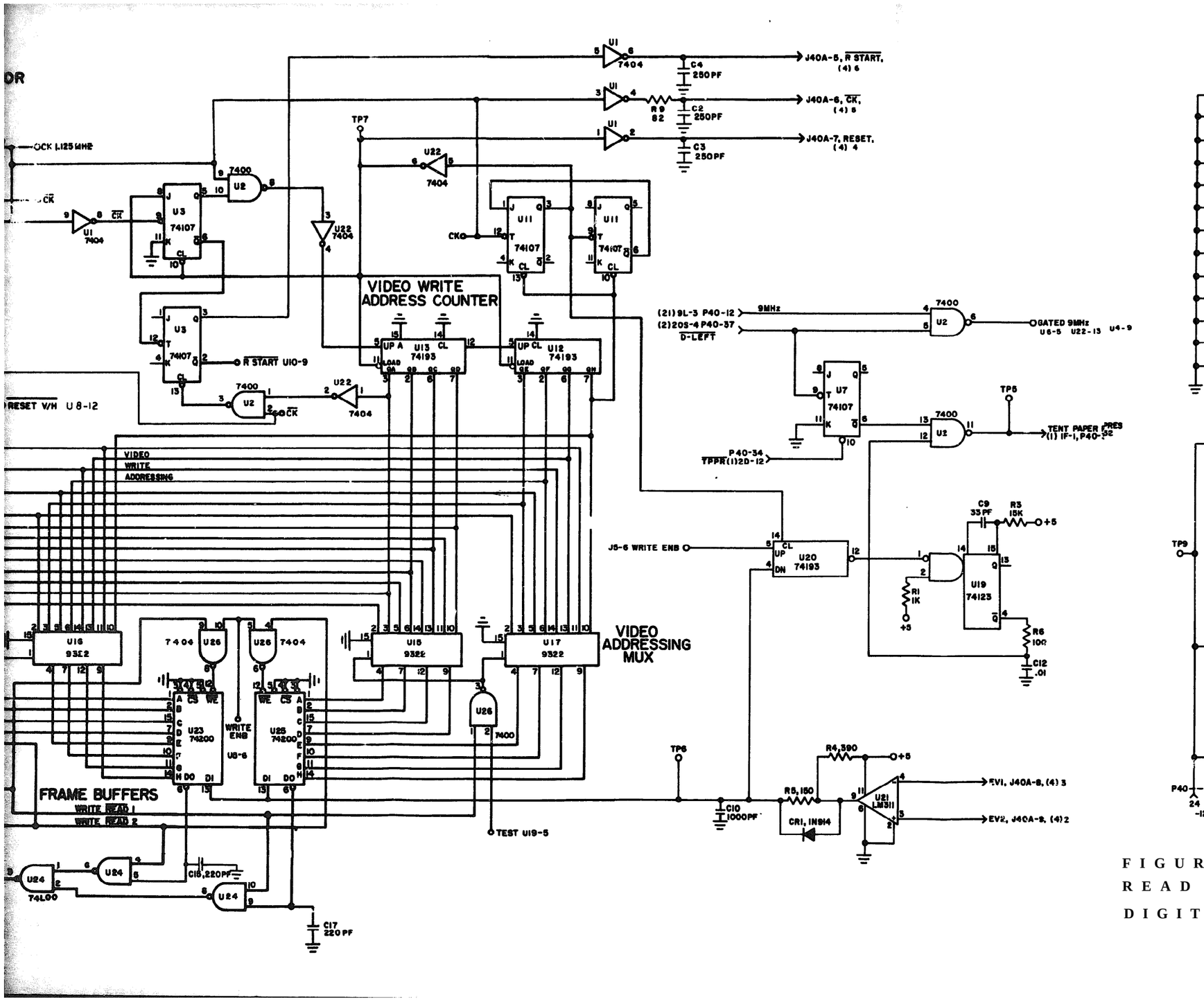
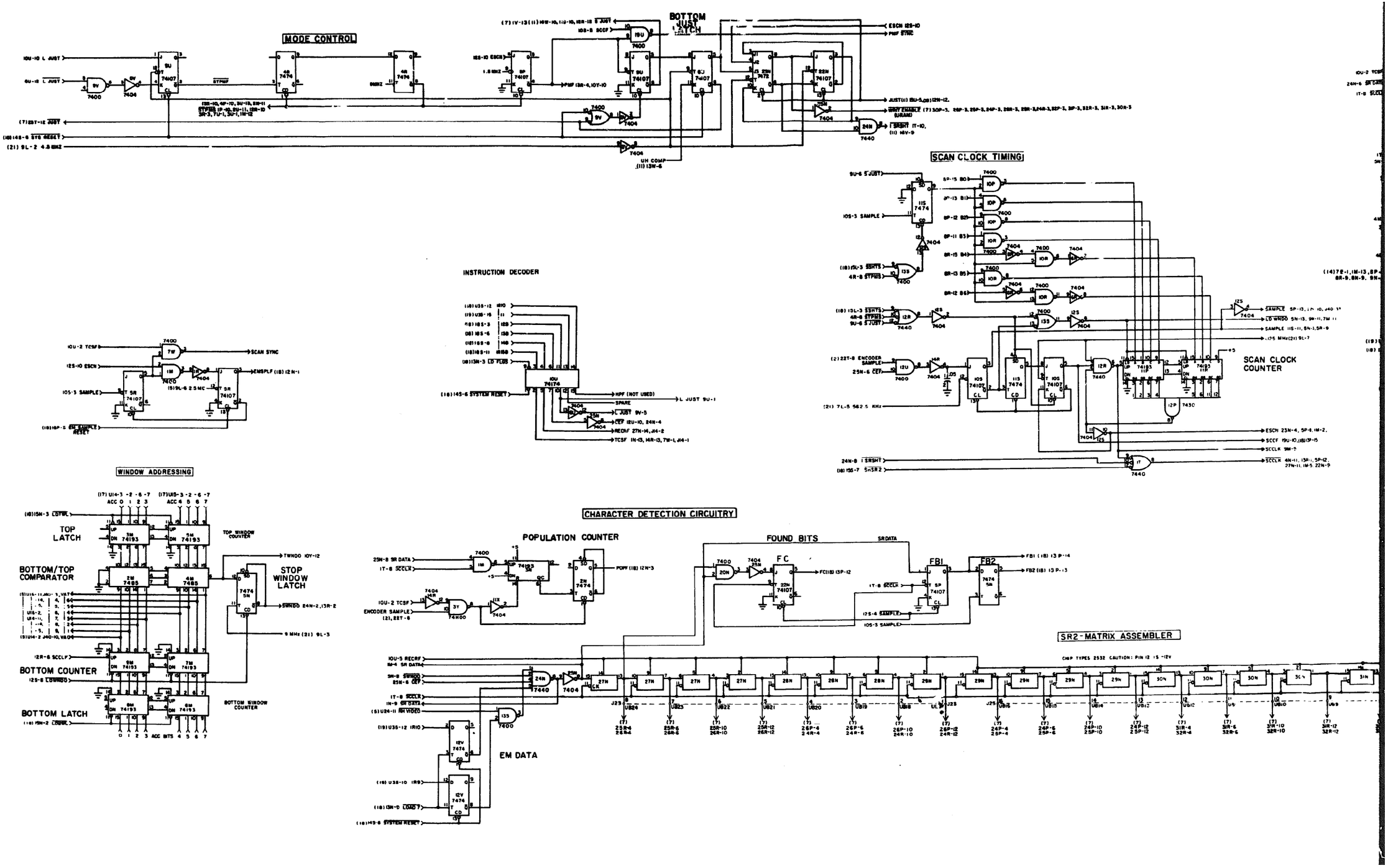


FIGURE A-5
READ HEAD
DIGITAL


MODE CONTROL
BOTTOM JUST LATCH
SCAN CLOCK TIMING
SCAN CLOCK COUNTER
INSTRUCTION DECODER
WINDOW ADDRESSING
TOP LATCH
BOTTOM/TOP COMPARATOR
BOTTOM COUNTER
BOTTOM LATCH
TOP WINDOW COUNTER
BOTTOM WINDOW COUNTER
STOP WINDOW LATCH
CHARACTER DETECTION CIRCUITRY
POPULATION COUNTER
FOUND BITS
SR2-MATRIX ASSEMBLER
EM DATA

POSITION MODE LOGIC (MATRIX ANALYSIS)

SCAN CLOCK TIMING

SCAN CLOCK COUNTER

SR1

O/I DETECT

I/O DETECT

VERTICAL SPACE LATCH

POSITION MODE COUNTER

SR2 - MATRIX ASSEMBLER

MAX HEIGHT LATCH

HEIGHT CALCULATOR ADDER

BIT HEIGHT TOO LOW LATCH

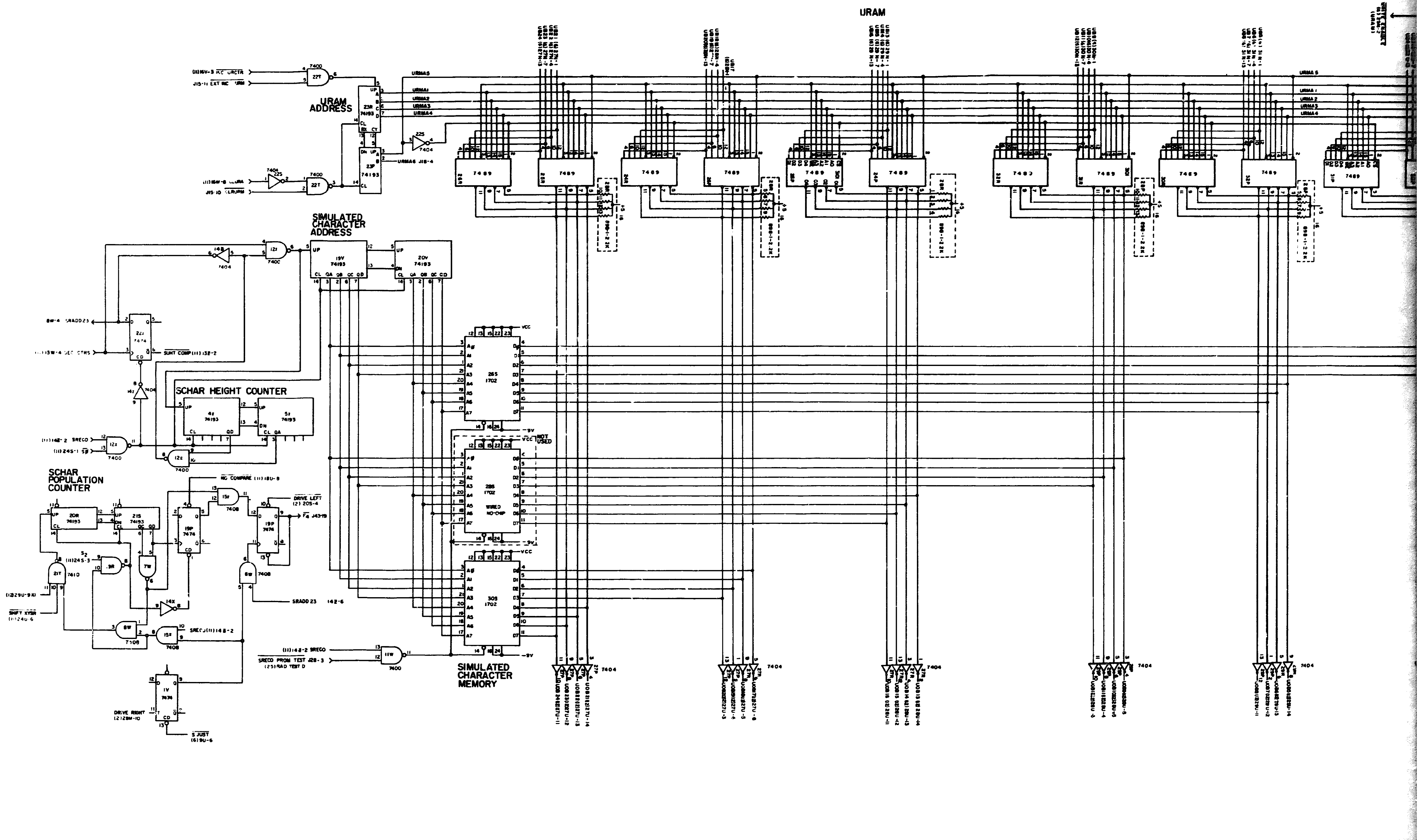
SR DATA

FB1

FB2

IR BITS

FIGURE A-6
VIDEO PROCESSOR


URAM
URAM ADDRESS
SIMULATED CHARACTER ADDRESS
SCHAR HEIGHT COUNTER
SCHAR POPULATION COUNTER
SIMULATED CHARACTER MEMORY
NOT USED
WIRED NO-CHIP

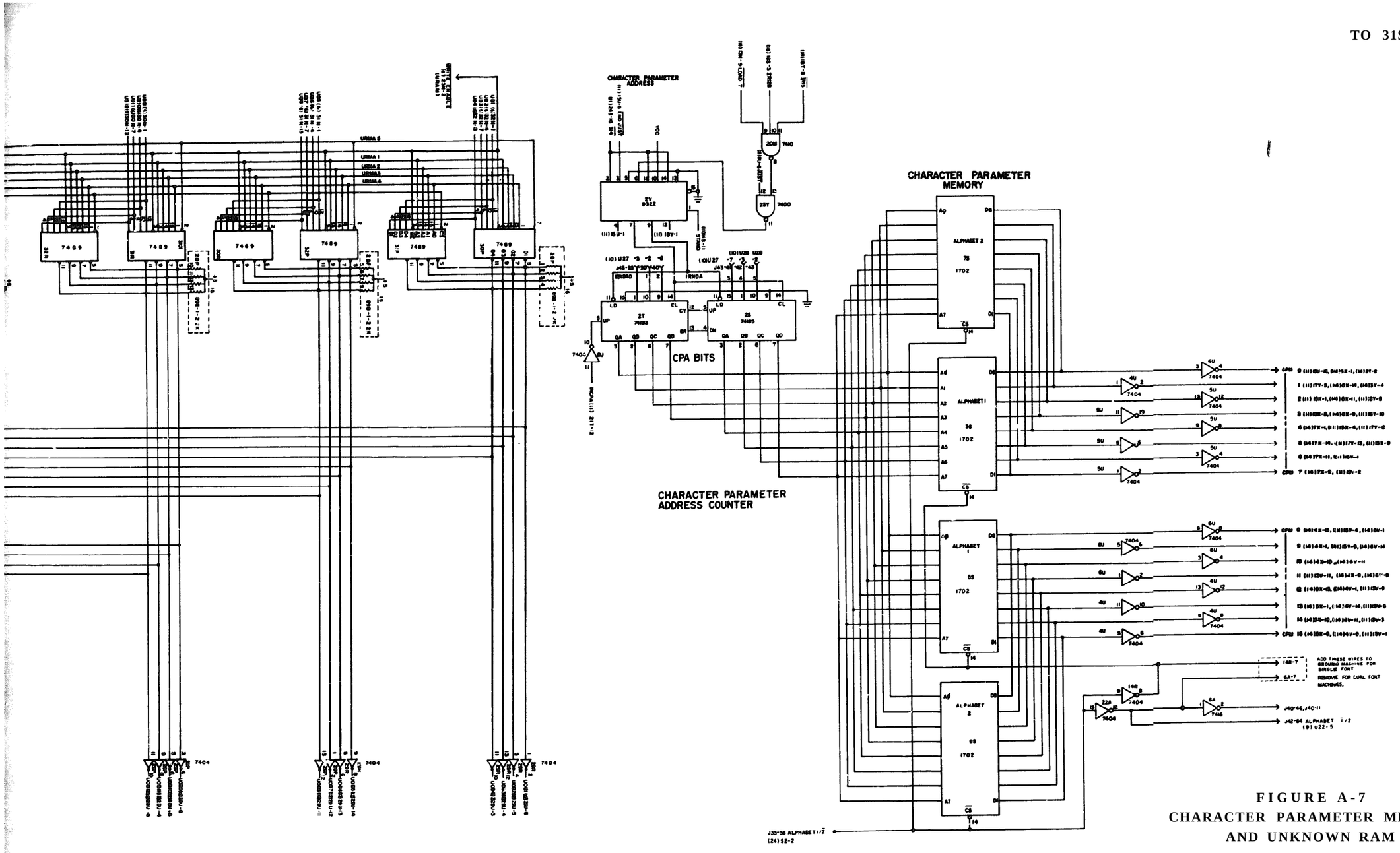
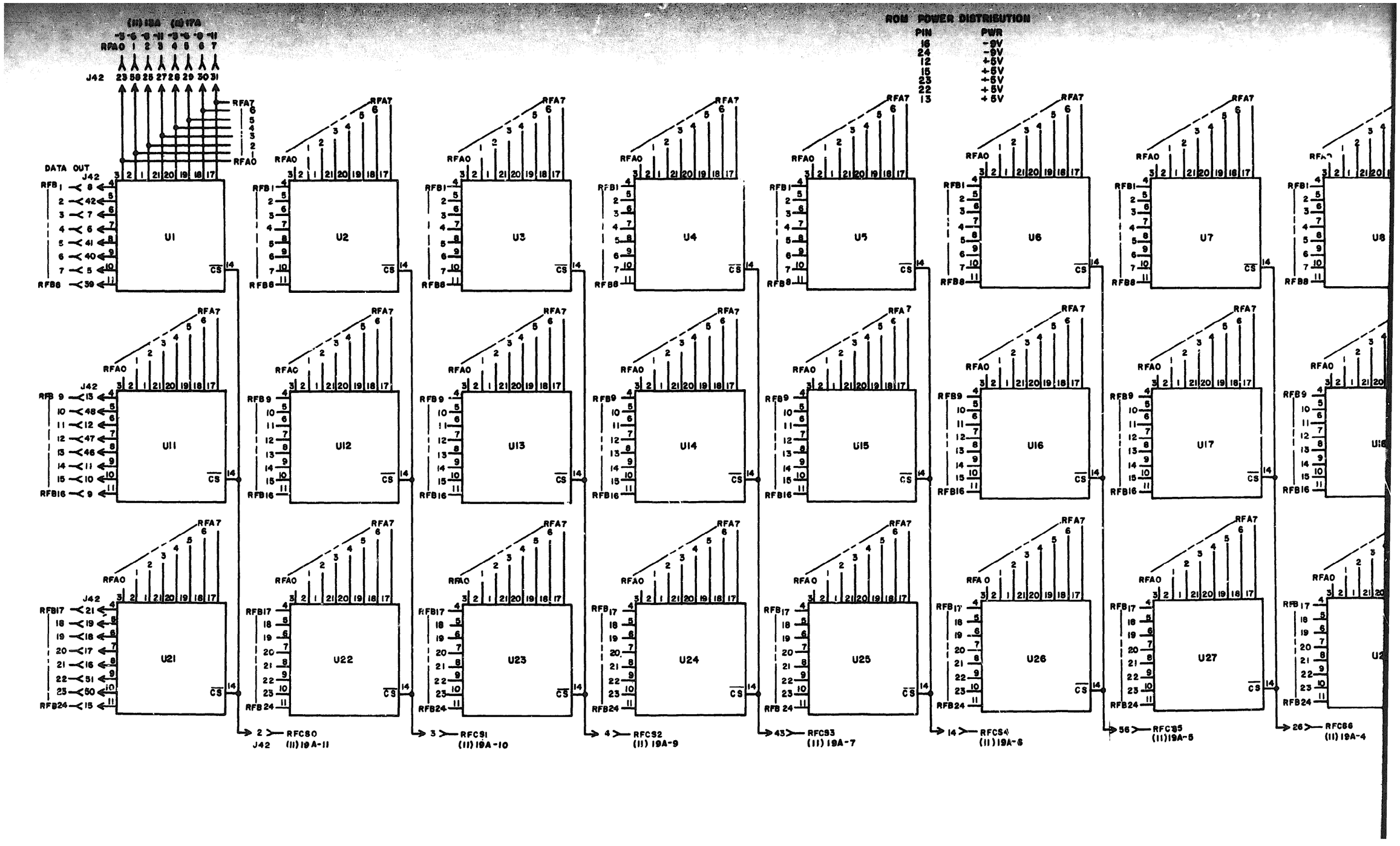


FIGURE A-7
CHARACTER PARAMETER MEMORY
AND UNKNOWN RAM


ROM POWER DISTRIBUTION
PIN PWR
16 -9V
24 -9V
12 +5V
15 +5V
23 +5V
22 +5V
13 +5V
(11) 18A (10) 17A
RFA0 RFA7
J42
DATA OUT
RFB1 RFB8 RFB9 RFB16 RFB17 RFB24
U1 U2 U3 U4 U5 U6 U7 U8
U11 U12 U13 U14 U15 U16 U17
U21 U22 U23 U24 U25 U26 U27
CS
2 RFCS0 J42 (11) 19A-11
3 RFCS1 (11) 19A-10
4 RFCS2 (11) 19A-9
43 RFCS3 (11) 19A-7
14 RFCS4 (11) 19A-6
56 RFCS5 (11) 19A-5
26 RFCS6 (11) 19A-4

ROM POWER DISTRIBUTION

PIN	PWR
16	-9V
24	-9V
12	+5V
15	+5V
23	+5V
22	+5V
13	+5V

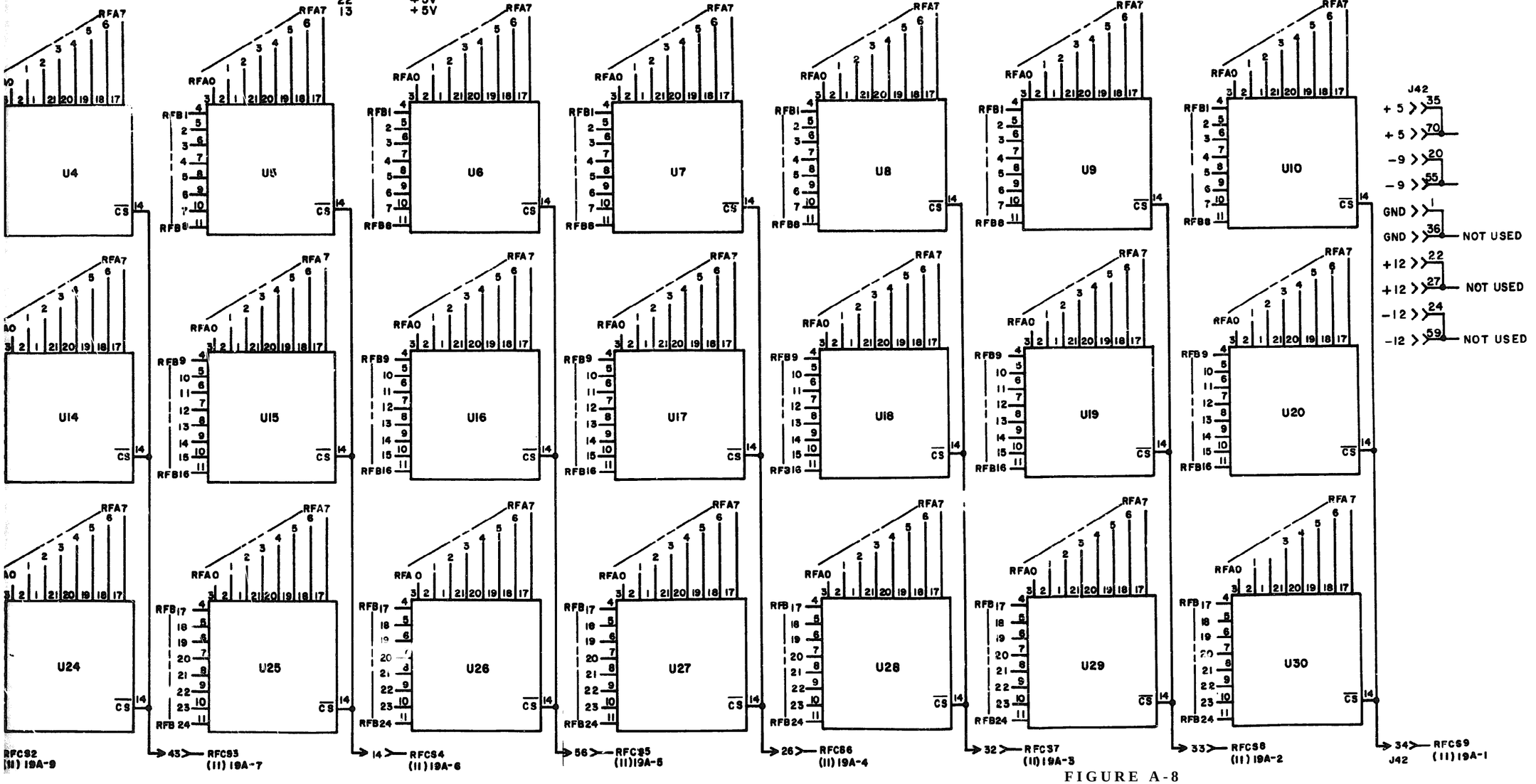
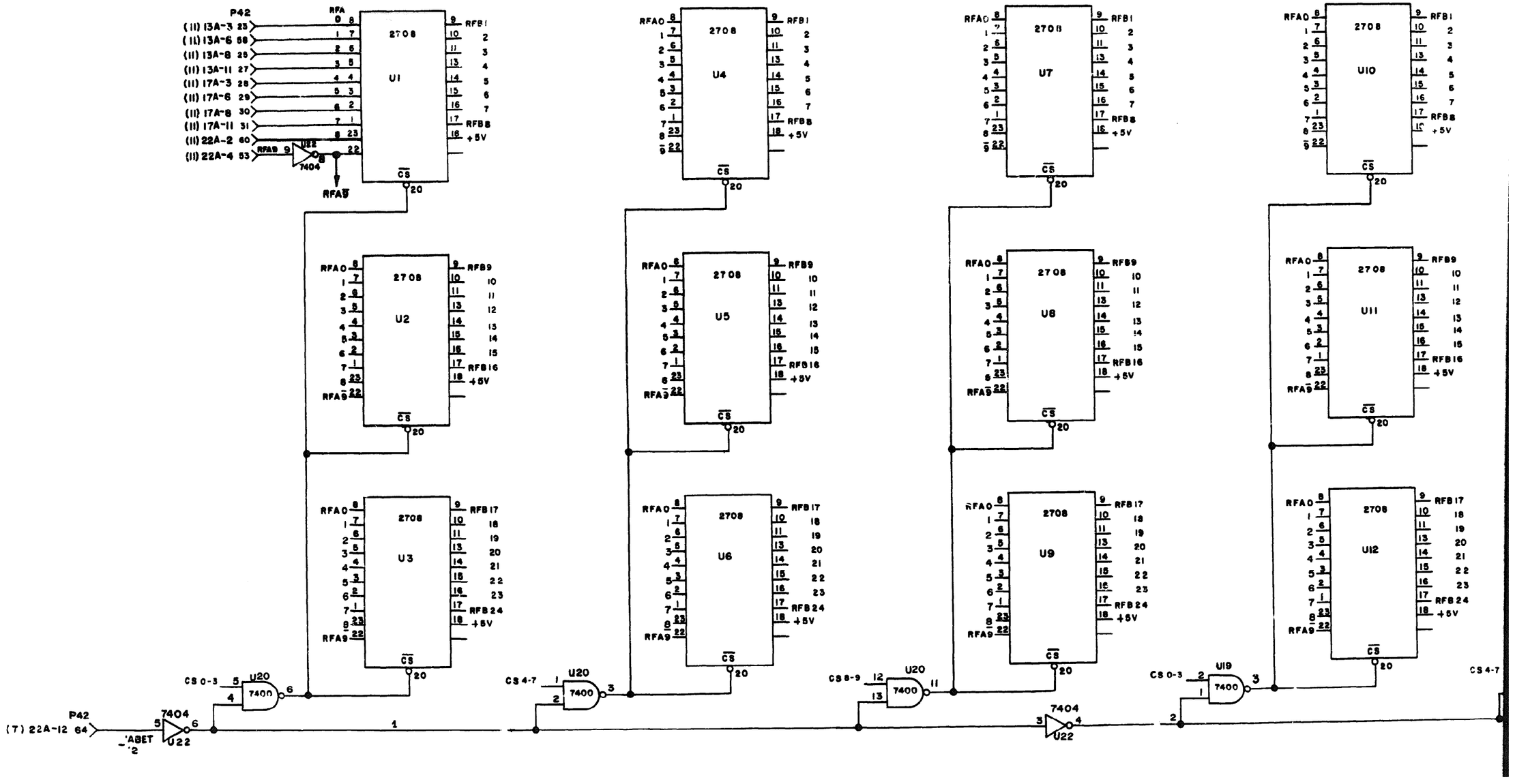
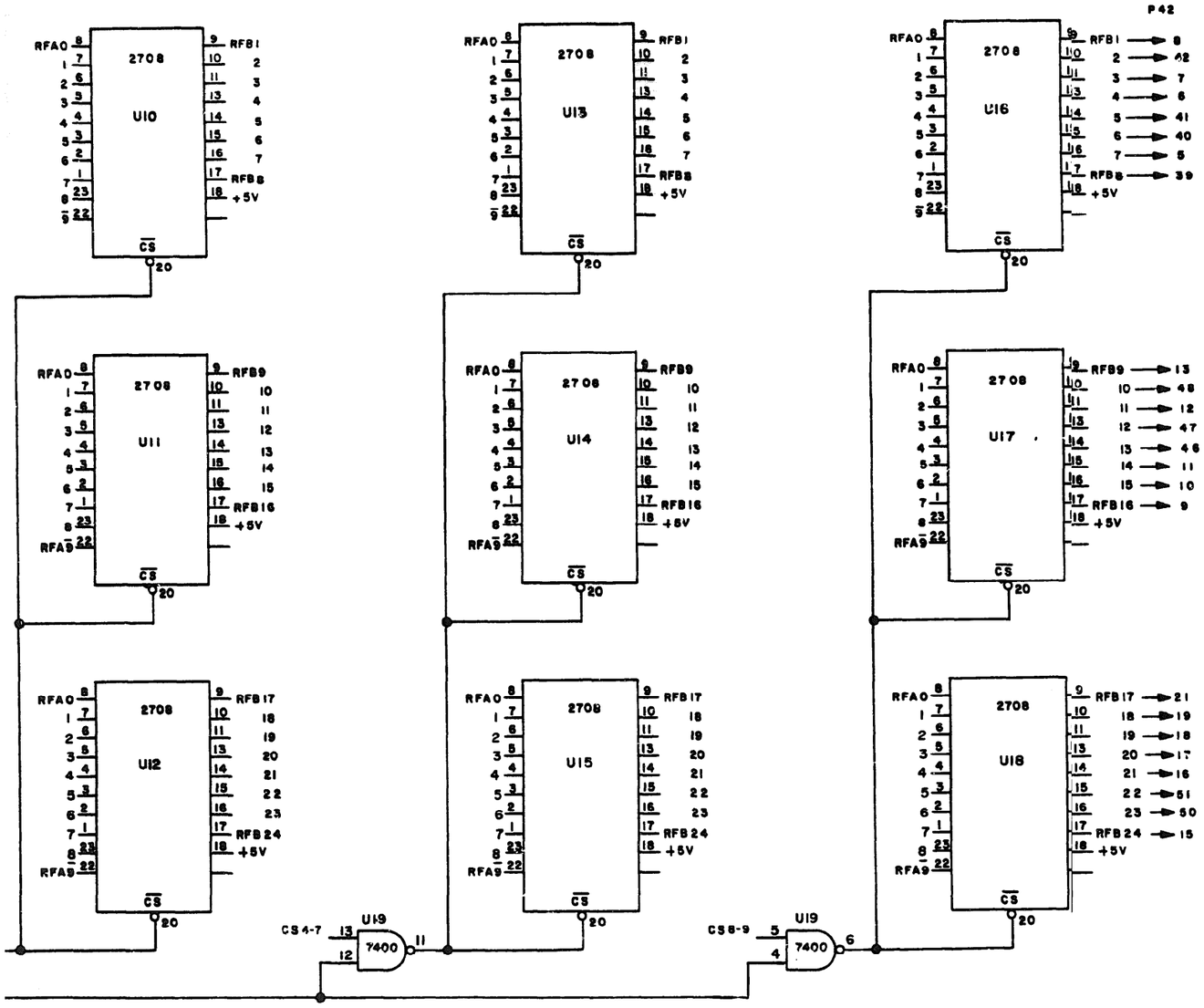


FIGURE A-8

REFERENCE ALPHABET MEMORY (SINGLE FONT)


P42
(11) 13A-3 25
(11) 13A-6 26
(11) 13A-8 28
(11) 13A-11 27
(11) 17A-3 28
(11) 17A-6 29
(11) 17A-8 30
(11) 17A-11 31
(11) 22A-2 60
(11) 22A-4 53
RFA
RFA9
U22
7404
RFA9
2708
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
CS
20
RFB1
RFB8
RFB9
RFB16
RFB17
RFB24
+5V
CS 0-3
CS 4-7
CS 8-9
U20
7400
U19
P42
(7) 22A-12 64
7404
U22
1

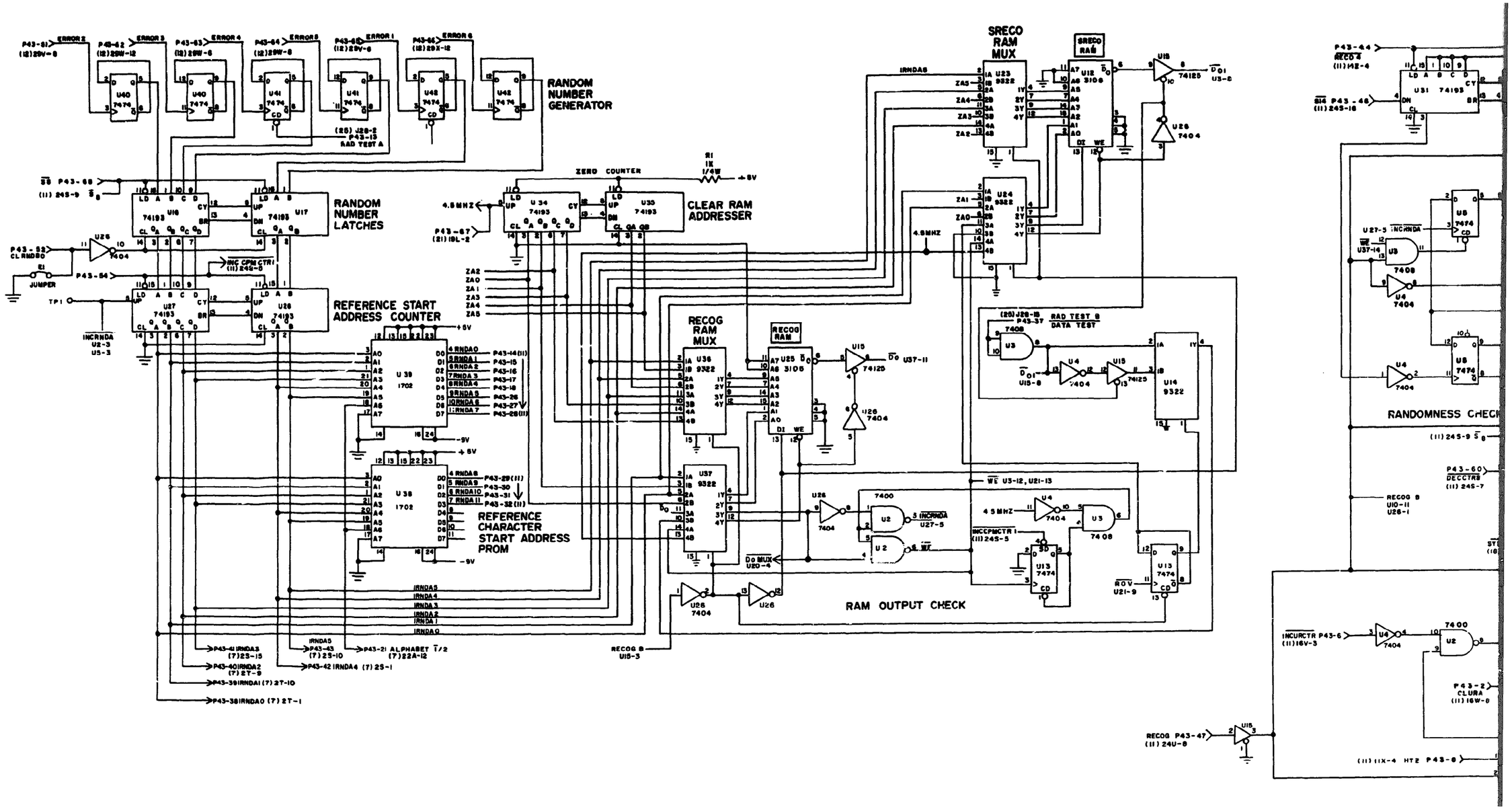


POWER DISTRIBUTION

DEVICE	PIN	VOLTAGE
2708	12	GND
	19	+12V
	21	-5V*
	24	+5V
7400	7	GND
	14	+5V
7404	7	GND
	14	+5V
7440	7	GND
	14	+5V

FIGURE A-9

REFERENCE ALPHABET MEMORY (DUAL FONT)


RANDOM NUMBER GENERATOR
RANDOM NUMBER LATCHES
REFERENCE START ADDRESS COUNTER
CLEAR RAM ADDRESSER
ZERO COUNTER
REFERENCE CHARACTER START ADDRESS PROM
RECOG RAM MUX
RECOG RAM
SRECO RAM MUX
SRECO RAM
RAM OUTPUT CHECK
RAD TEST B DATA TEST
RANDOMNESS CHECK
JUMPER
INCRNDA
WE U3-12, U21-13
RECOG B U10-11 U26-1
P43-60 DECCTR8 (11) 24S-7
P43-2 CLURA (11) 16W-8
RECOG P43-47 (11) 24U-8
INCURCTR P43-6 (11)16V-3
(11) 11X-4 HTZ P43-8

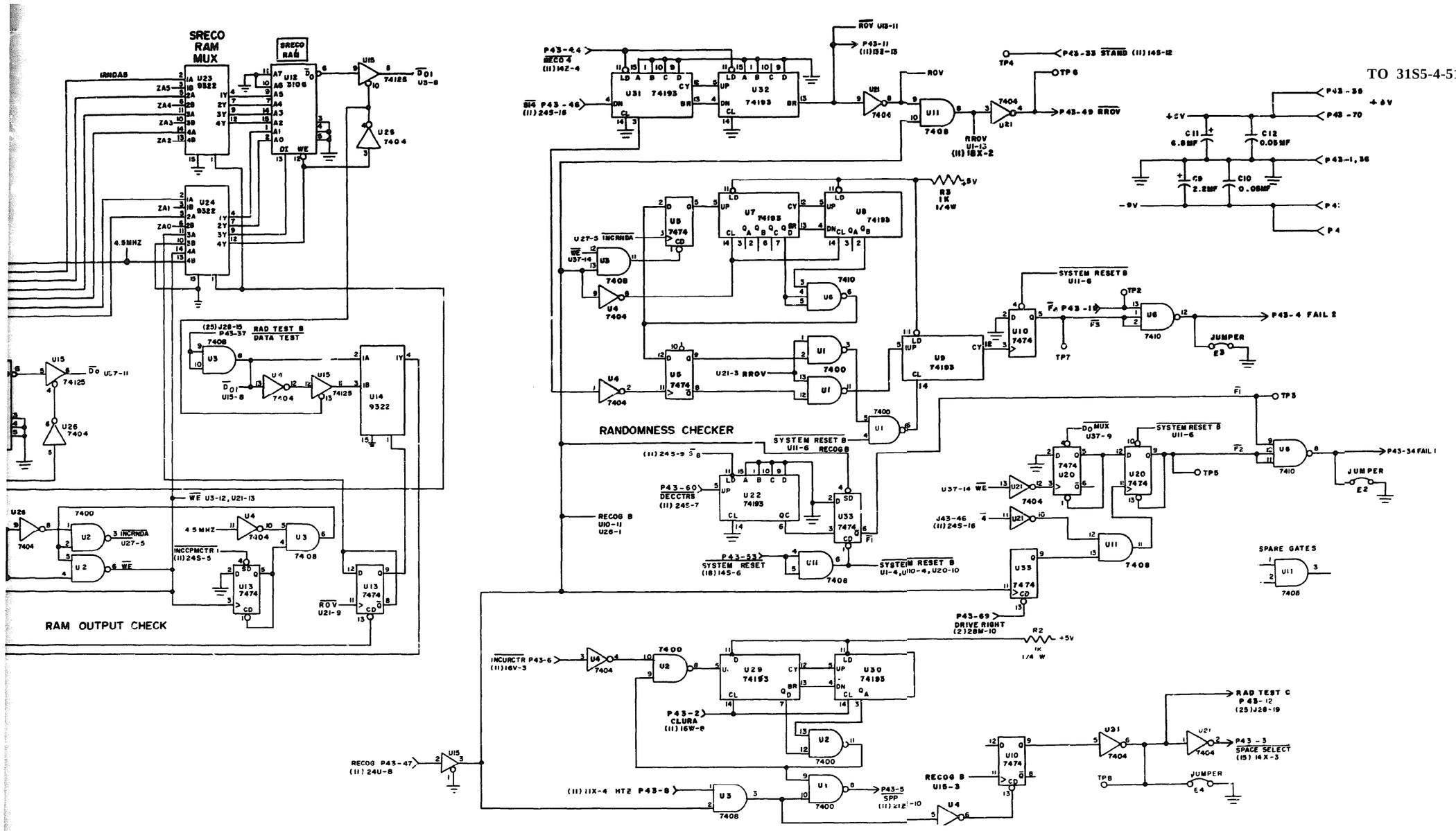
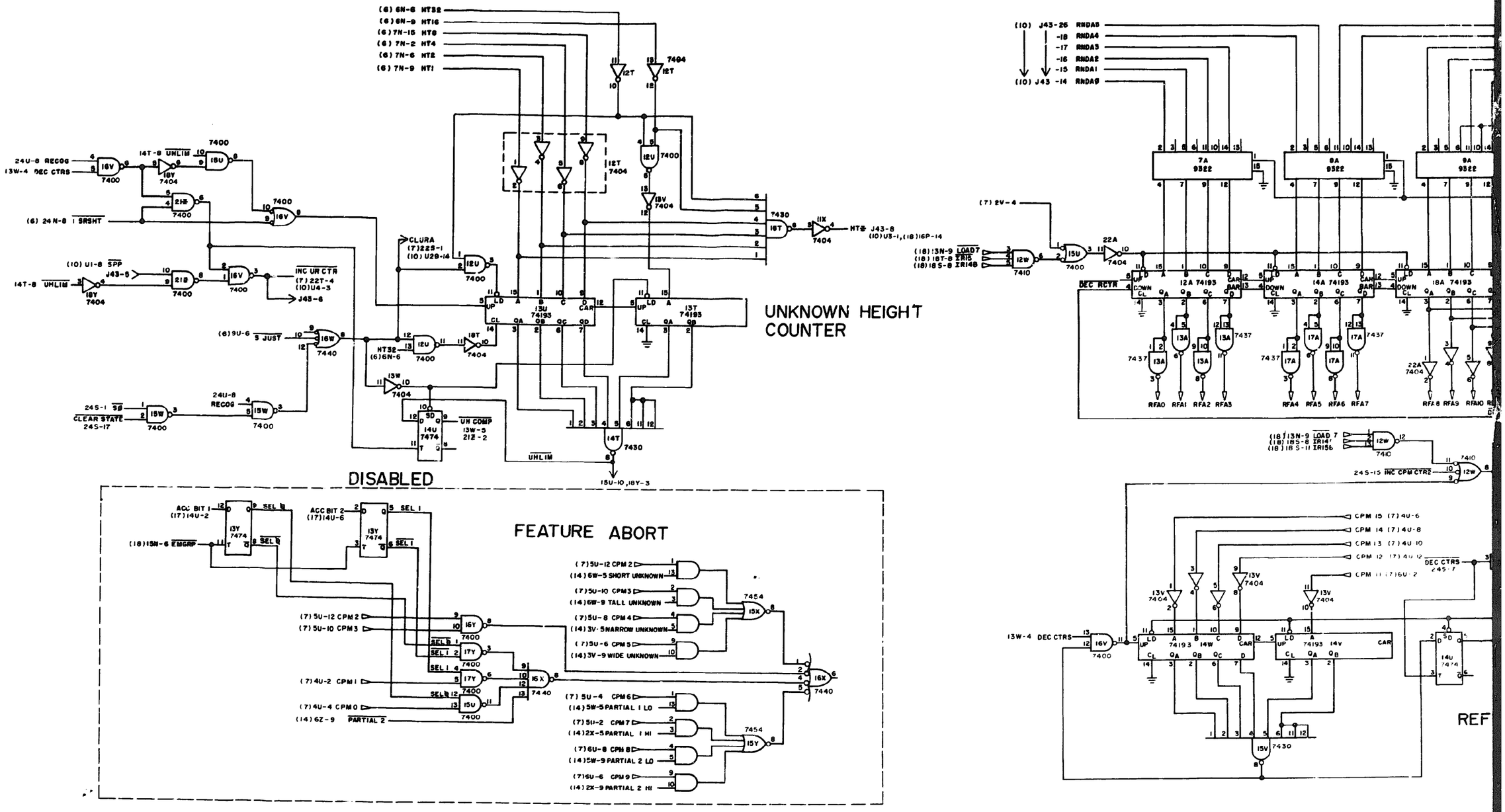
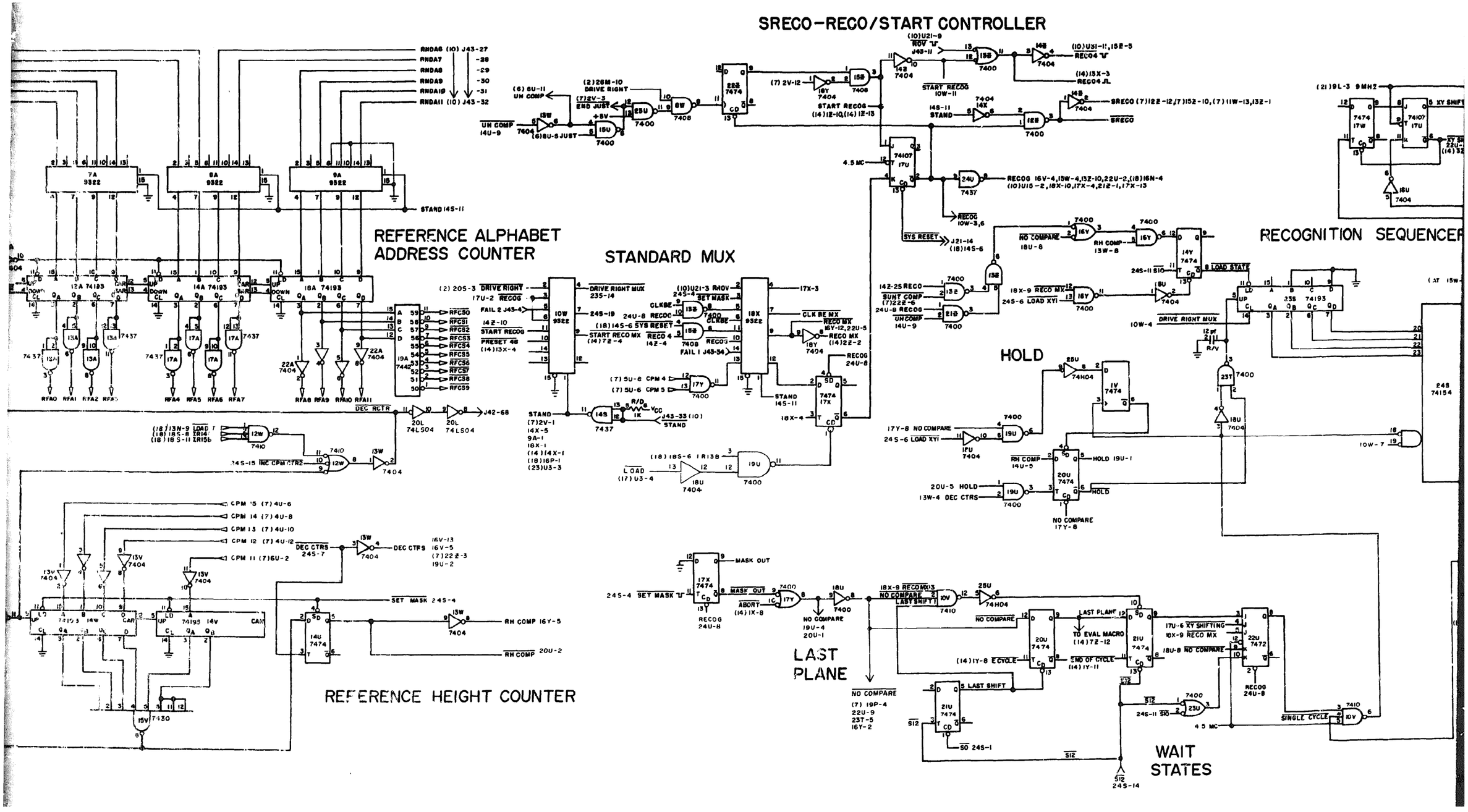


FIGURE A-10
SIMULATED RECOGNITION CONTROLLER
AND RANDOM REFERENCE CHARACTER SELECT


UNKNOWN HEIGHT COUNTER
DISABLED
FEATURE ABORT
REF
DEC RCTR
UHLIM
CLEAR STATE
INC UR CTR
UH COMP
CLURA
LOAD7
INC CPM CTR2
DEC CTRS
CPM 15 (7) 4U-6
CPM 14 (7) 4U-8
CPM 13 (7) 4U-10
CPM 12 (7) 4U-12
(7) 2V-4
(10) J43-26 RNDA9
-18 RNDA8
-17 RNDA7
-16 RNDA6
-15 RNDA5
(10) J43 -14 RNDA4
(6) 6N-8 MT32
(6) 6N-9 MT16
(6) 7N-15 MT8
(6) 7N-2 MT4
(6) 7N-6 MT2
(6) 7N-9 MT1
(6) 24N-8 I SRSHT
(10) U1-8 SPP
(6) 9U-6 S JUST
(14) 6Z-9 PARTIAL 2
(14) 6W-5 SHORT UNKNOWN
(14) 6W-9 TALL UNKNOWN
(14) 3V-5 NARROW UNKNOWN
(14) 3V-9 WIDE UNKNOWN
(14) 5W-5 PARTIAL 1 LO
(14) 2X-5 PARTIAL 1 HI
(14) 5W-9 PARTIAL 2 LO
(14) 2X-9 PARTIAL 2 HI
ACC BIT 1 (17) 14U-2
ACC BIT 2 (17) 14U-6
(18) 15N-6 EMGRP
7A 9322
9A 9322
12A 74193
14A 74193
18A 74193
13U 74193
13T 74193
14U 7474
13Y 7474
12T 7404
7400
7404
7410
7430
7440
7454
7437


SRECO-RECO/START CONTROLLER
REFERENCE ALPHABET ADDRESS COUNTER
STANDARD MUX
RECOGNITION SEQUENCER
HOLD
REFERENCE HEIGHT COUNTER
LAST PLANE
WAIT STATES
RNDA6 (10) J43-27
RNDA7 -28
RNDA8 -29
RNDA9 -30
RNDA10 -31
RNDA11 (10) J43-32
STAND 14S-11
RFA0 RFA1 RFA2 RFA3 RFA4 RFA5 RFA6 RFA7 RFA8 RFA9 RFA10 RFA11
RFC50 RFC51 RFC52 RFC53 RFC54 RFC55 RFC56 RFC57 RFC58 RFC59
DEC RGTR J42-68
(2) 205-3 DRIVE RIGHT
17U-2 RECOG
FAIL 2 J43-4
142-10 START RECOG
PRESET 4G (14)13X-4
DRIVE RIGHT MUX 23S-14
24S-19 24U-8 RECOG
(18)14S-6 SYS RESET
START RECO MX (14)7Z-4
RECO 14Z-4
(10)U21-3 RNOV 24S-4 SET MASK
CLKBE 9
RECOG
FAIL 1 J43-34
17X-3
CLK BE MX
RECO MX 16V-12,22U-5
RECO MX (14)12Z-2
RECOG 24U-8
(7) 5U-6 CPM 4
(7) 5U-6 CPM 5
STAND 14S-11
18X-4
STAND (7)12V-1 14X-5 9A-1 18X-1 (14)14X-1 (18)16P-1 (23)U3-3
R/D 1K
J43-33 (10) STAND
(18) 18S-6 1R138
LOAD (17) U3-4
(6) 8U-11 UH COMP
UH COMP 14U-9
(2) 28M-10 DRIVE RIGHT
(7)2V-5 END JUST
+8V
(6)8U-5 JUST
(7) 2V-12
START RECOG (14)12-10,(14) 12-13
(10)U21-9 NOV "L"
J43-11
(10)U31-11, 15Z-5 RECO4 "L"
(14)13X-3 RECO4 JL
START RECOG 10W-11
14S-11 STAND
SRECO (7)12Z-12,(7)15Z-10,(7) 11W-13,13Z-1
SRECO
4.5 MC
RECOG 16V-4,15W-4,15Z-10,22U-2,(18)16N-4 (10)U15-2,18X-10,17X-4,21Z-1,17X-13
RECOG 10W-3,6
SYS RESET
J21-14 (18)14S-6
NO COMPARE 18U-8
RH COMP 13W-8
(21)9L-3 9MHZ
XY SHIFT
LOAD STATE
245-11 S10
142-25 RECO (7)22Z-5 24U-8 RECO UNCOMP 14U-9
18X-9 RECO MX
245-6 LOAD XYI
10W-4 DRIVE RIGHT MUX
12 pf R/V
245 74154
17Y-8 NO COMPARE
24S-6 LOAD XYI
RH COMP 14U-5
20U-5 HOLD
13W-4 DEC CTRS
HOLD 19U-1
HOLD
NO COMPARE 17Y-8
10W-7
CPM 15 (7)4U-6
CPM 14 (7)4U-8
CPM 13 (7)4U-10
CPM 12 (7)4U-12
CPM 11 (7)6U-2
DEC CTRS 24S-7
DEC CTRS
16V-13 16V-5 (7)22Z-3 19U-2
SET MASK 24S-4
RH COMP 16Y-5
RH COMP 20U-2
15V 7430
MASK OUT
24S-4 SET MASK
ABORT (14)1X-8
RECOG 24U-8
NO COMPARE 19U-4 20U-1
NO COMPARE (7) 19P-4 22U-9 23T-5 16Y-2
18X-9 RECOMX13
NO COMPARE
LAST SHIFT
NO COMPARE
LAST PLANE
TO EVAL MACRO (14)7Z-12
(14)11Y-8 ECYCLE
END OF CYCLE (14)11Y-11
S LAST SHIFT
S12
S0 24S-1
S12
S12 24S-14
17U-6 XY SHIFTING
18X-9 RECO MX
18U-8 NO COMPARE
24S-11 S10
RECOG 24U-8
SINGLE CYCLE
4.5 MC

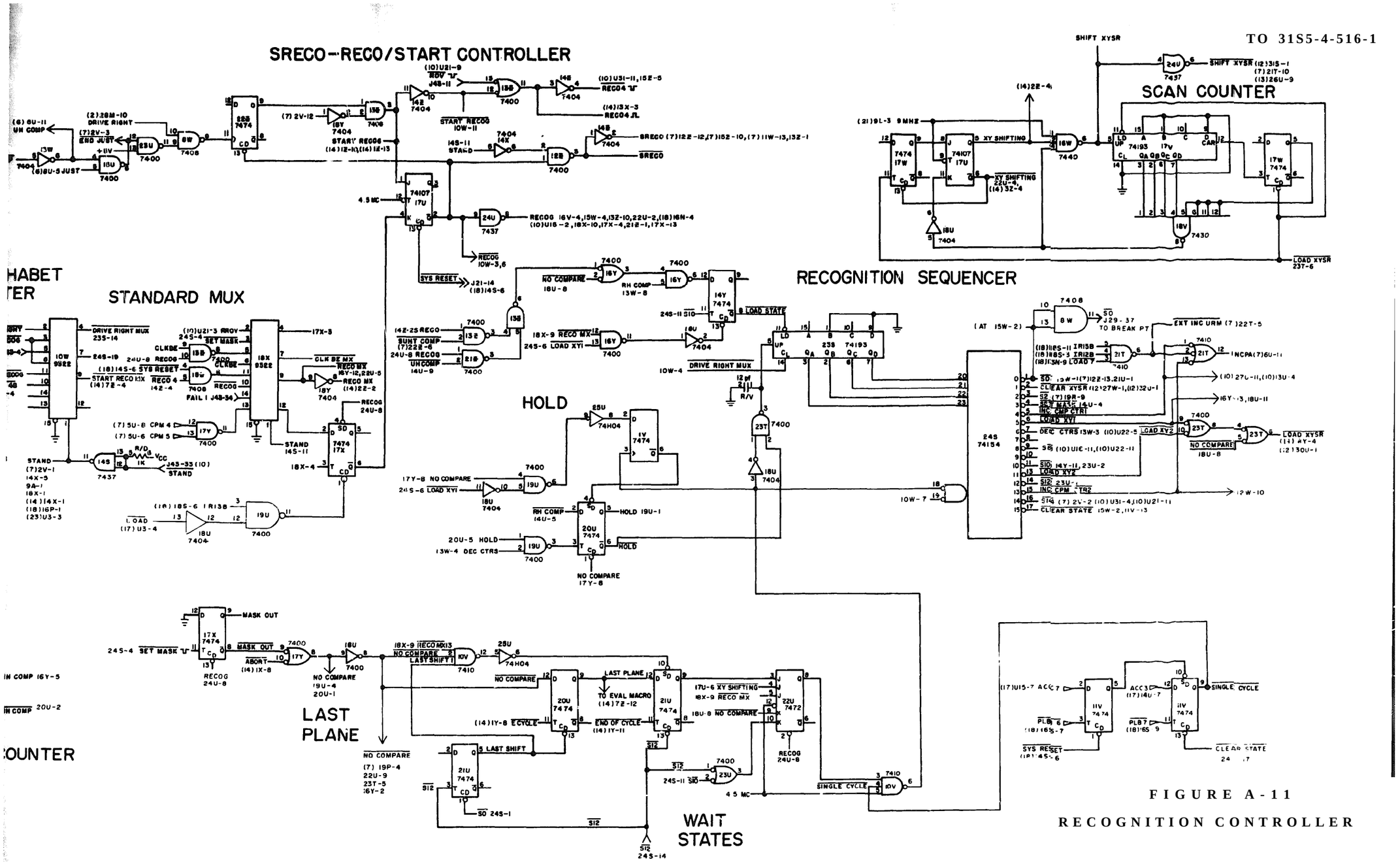
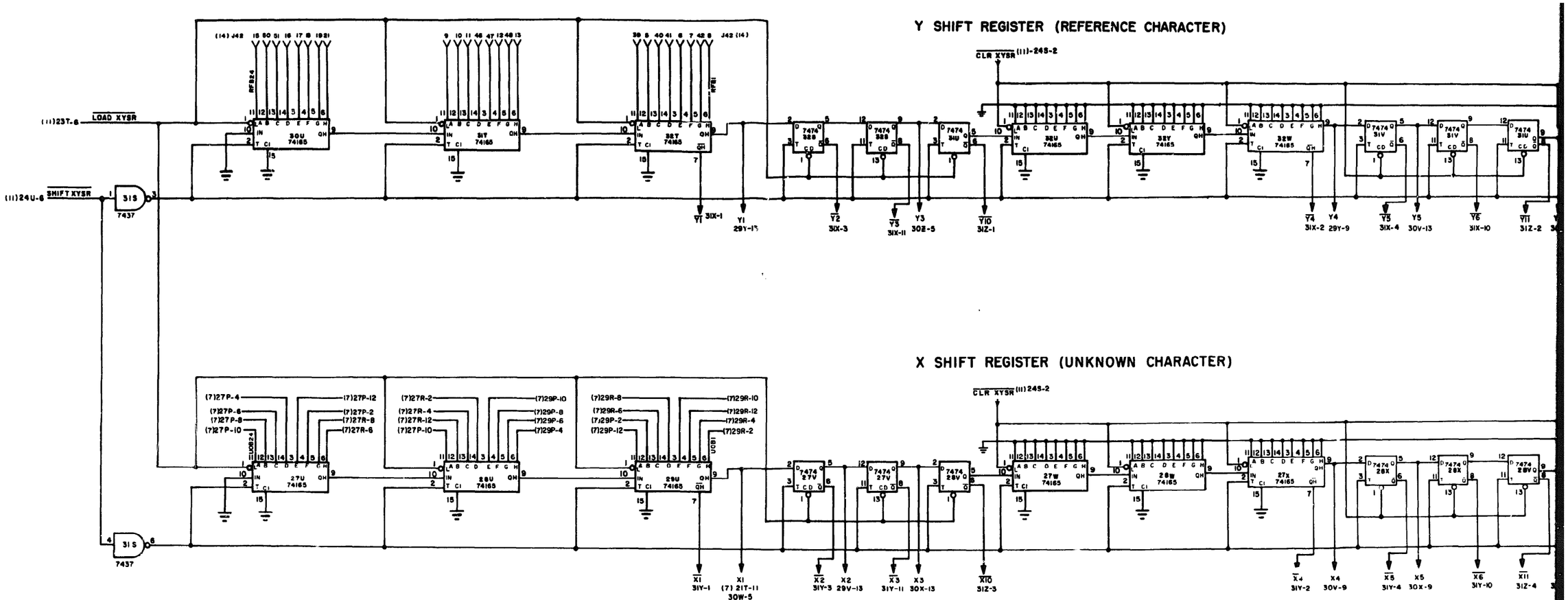
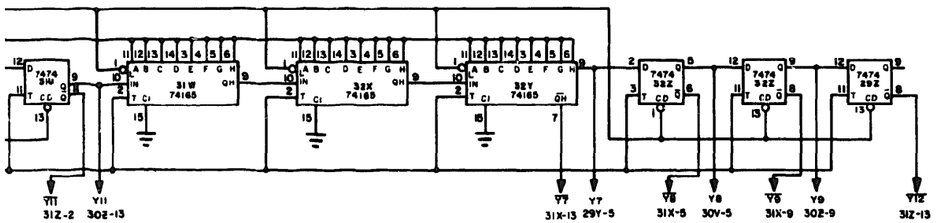
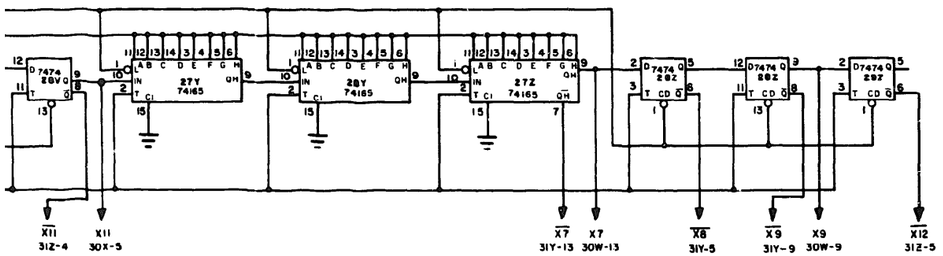


FIGURE A-11

RECOGNITION CONTROLLER


Y SHIFT REGISTER (REFERENCE CHARACTER)
X SHIFT REGISTER (UNKNOWN CHARACTER)
LOAD XYSR
SHIFT XYSR
CLR XYSR
7437
7474
74165





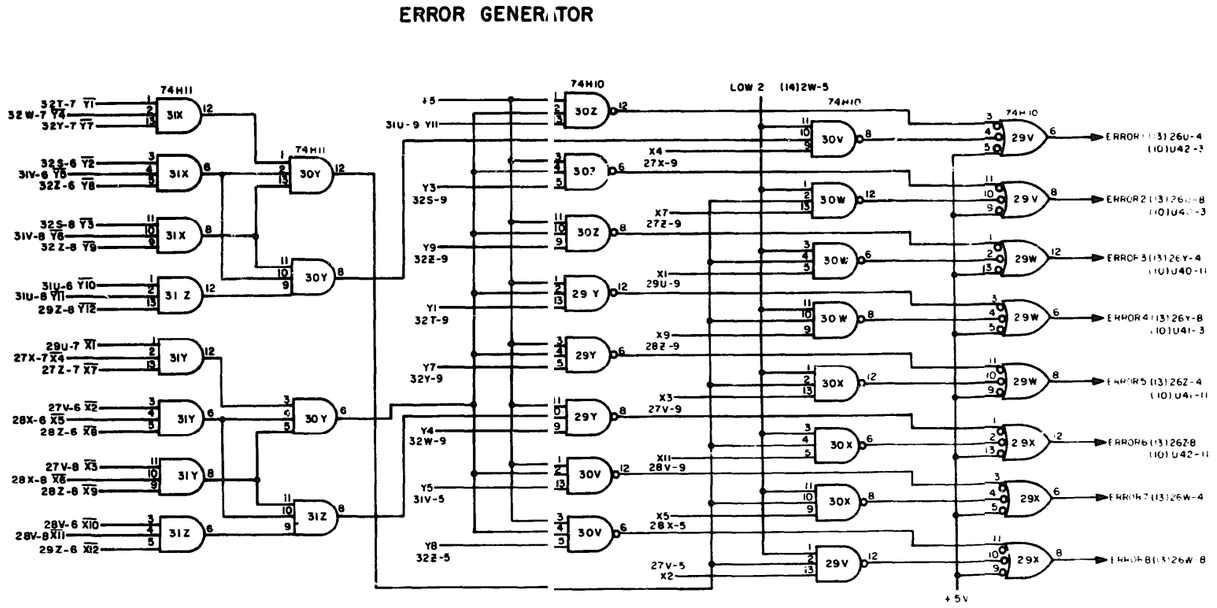


FIGURE A-12
SHIFT REGISTER/ ERROR GENERATOR

TO 31S5-4-516-1

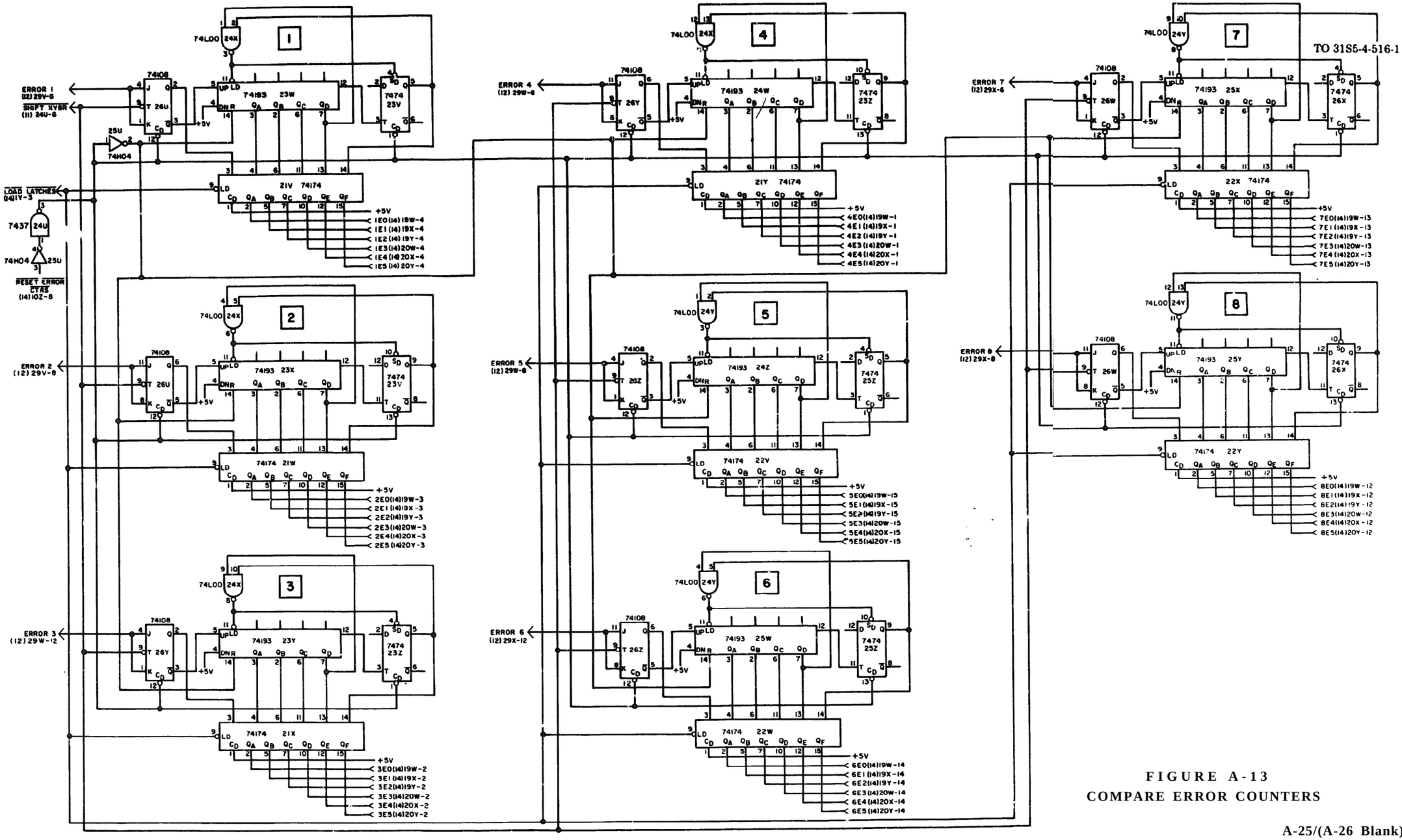


FIGURE A-13
COMPARE ERROR COUNTERS

EVALUATION SEQUENCER

ERROR MUX

ERROR COMPARATOR

BEST ERROR LATCH

DISABLED

NOMINAL BOTTOM SPACE

EARLY ABORT

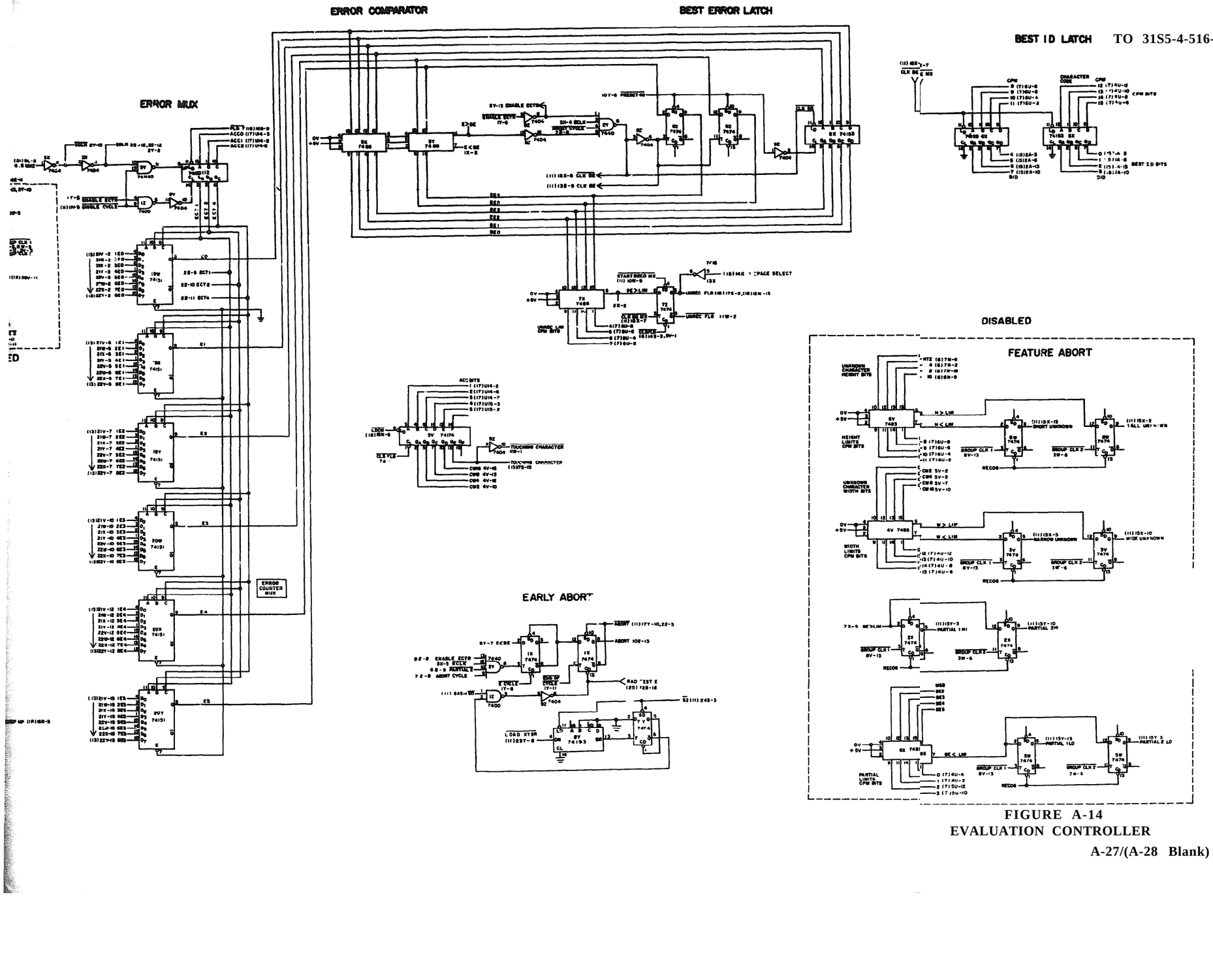
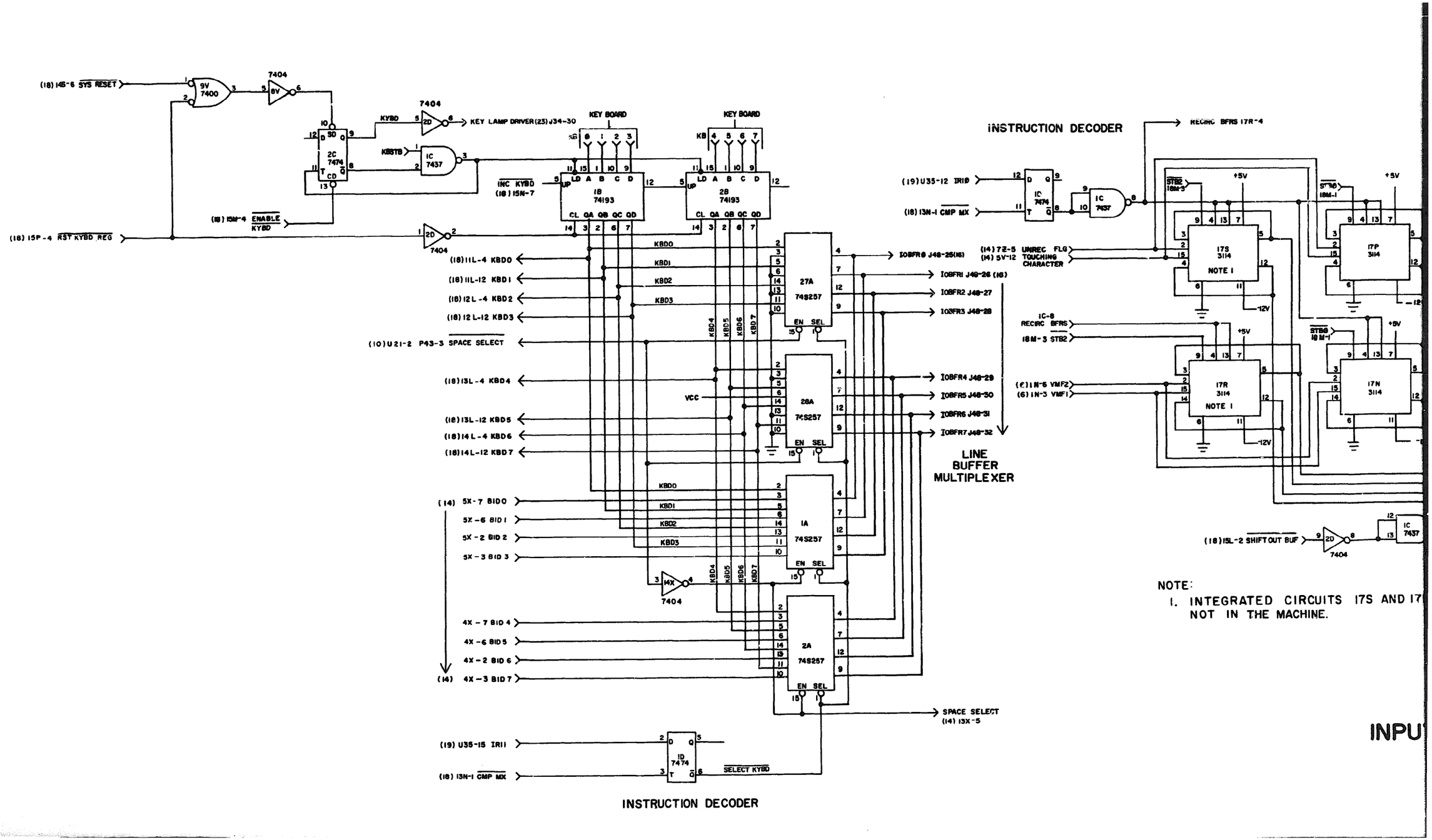


FIGURE A-14
EVALUATION CONTROLLER

KEY BOARD LATCH

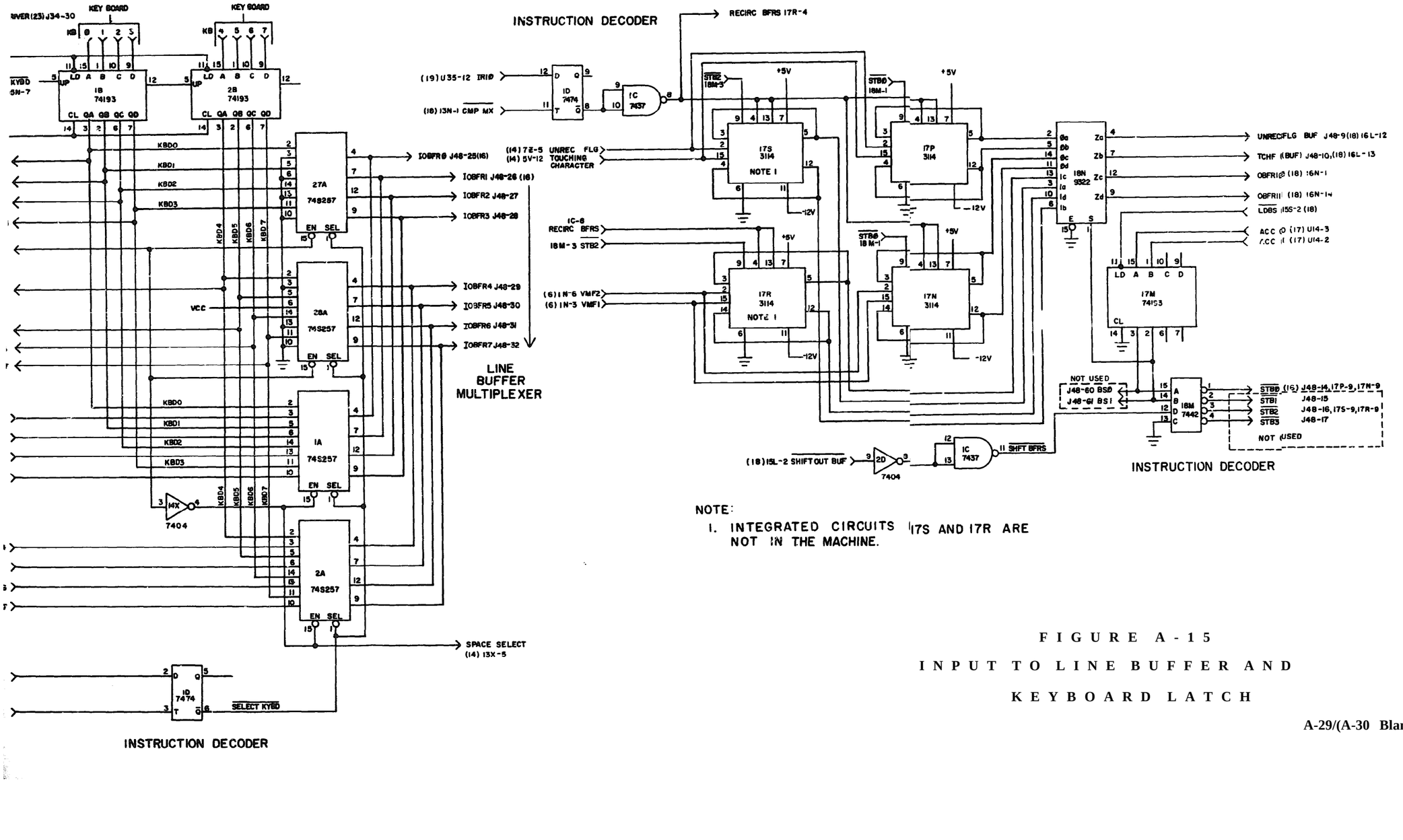
FLAG BUFFERS



NOTE:

1. INTEGRATED CIRCUITS I7S AND I7
   NOT IN THE MACHINE.

INPU

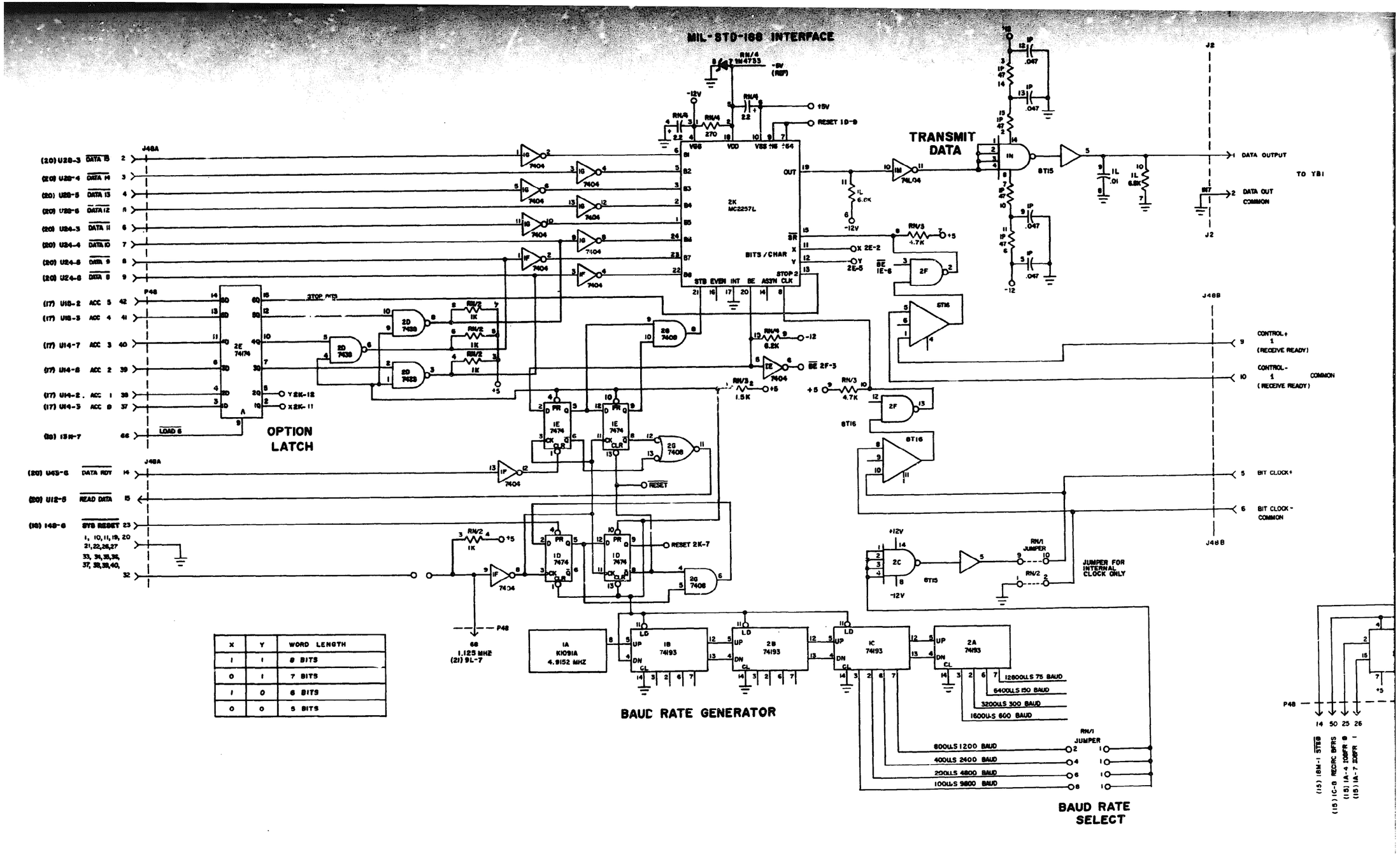


NOTE:

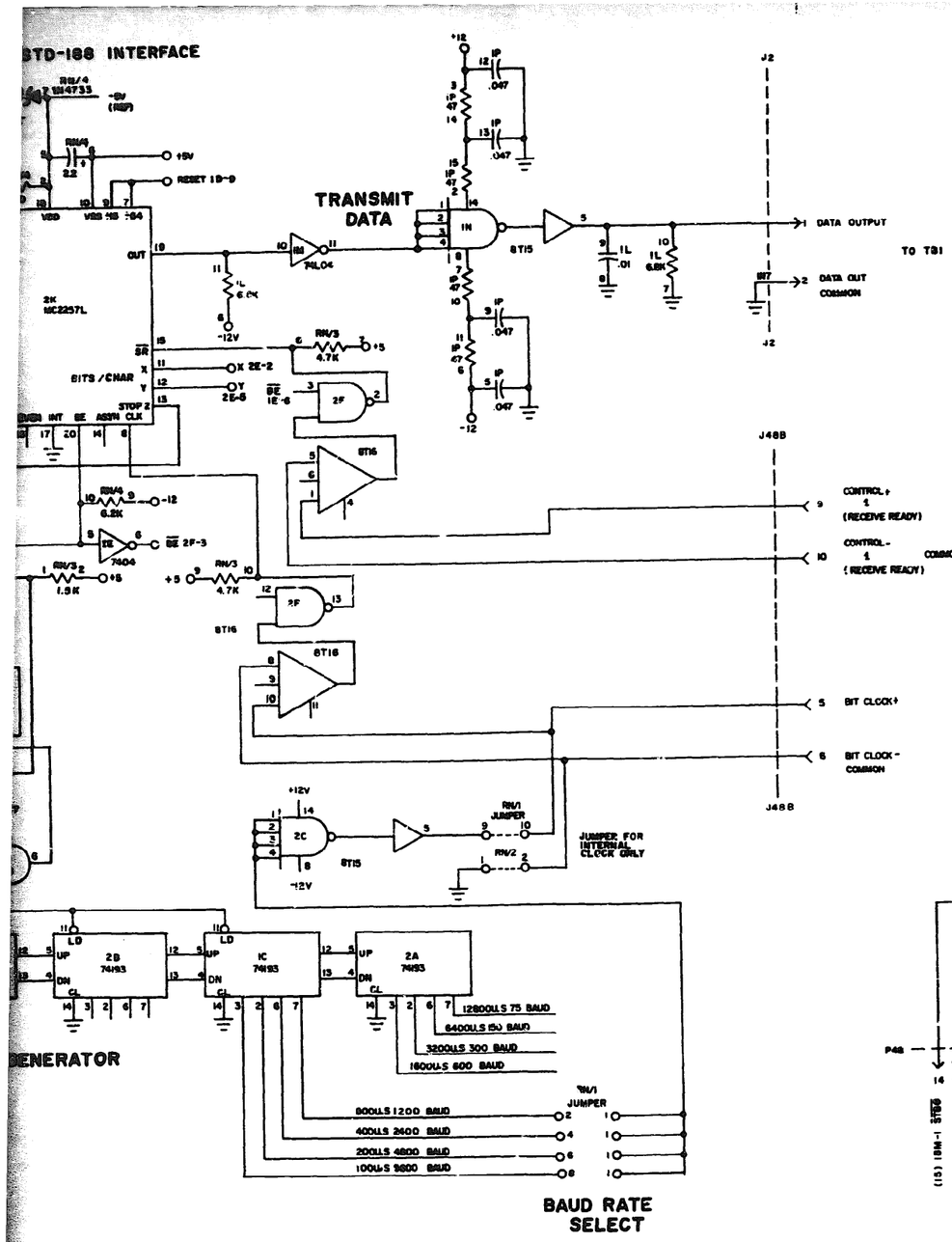
1. INTEGRATED CIRCUITS 17S AND 17R ARE NOT IN THE MACHINE.

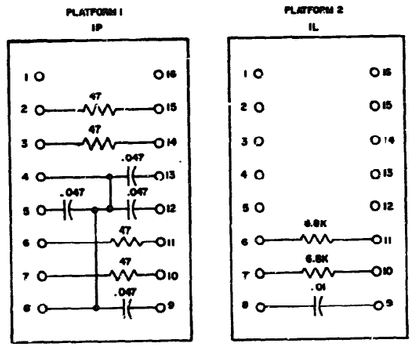
FIGURE A-15

INPUT TO LINE BUFFER AND KEYBOARD LATCH



X	Y	WORD LENGTH
1	1	8 BITS
0	1	7 BITS
1	0	6 BITS
0	0	5 BITS





NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS 1/4 W, 5%.
   B. ALL CAPACITOR VALUES ARE IN MICROFARADS.

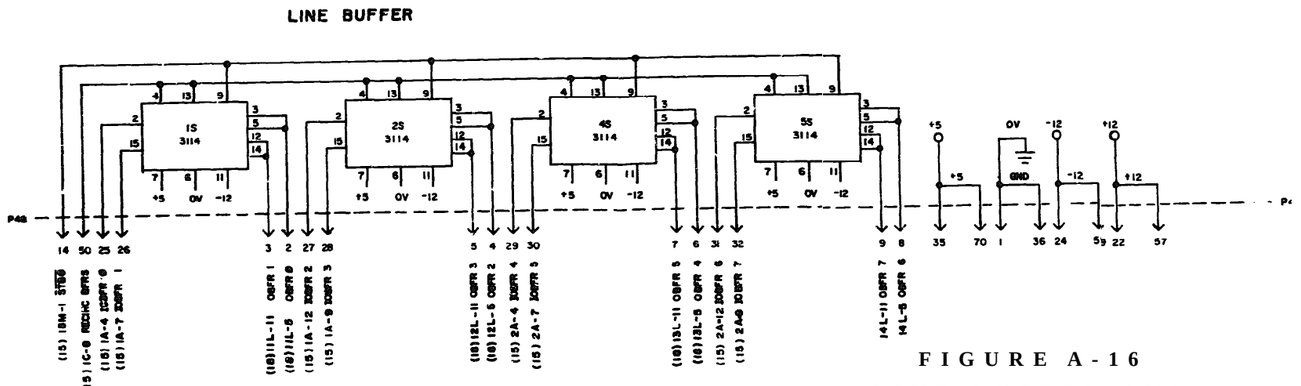


FIGURE A-16

LINE BUFFER AND MIL-STD-188 INTERFACE

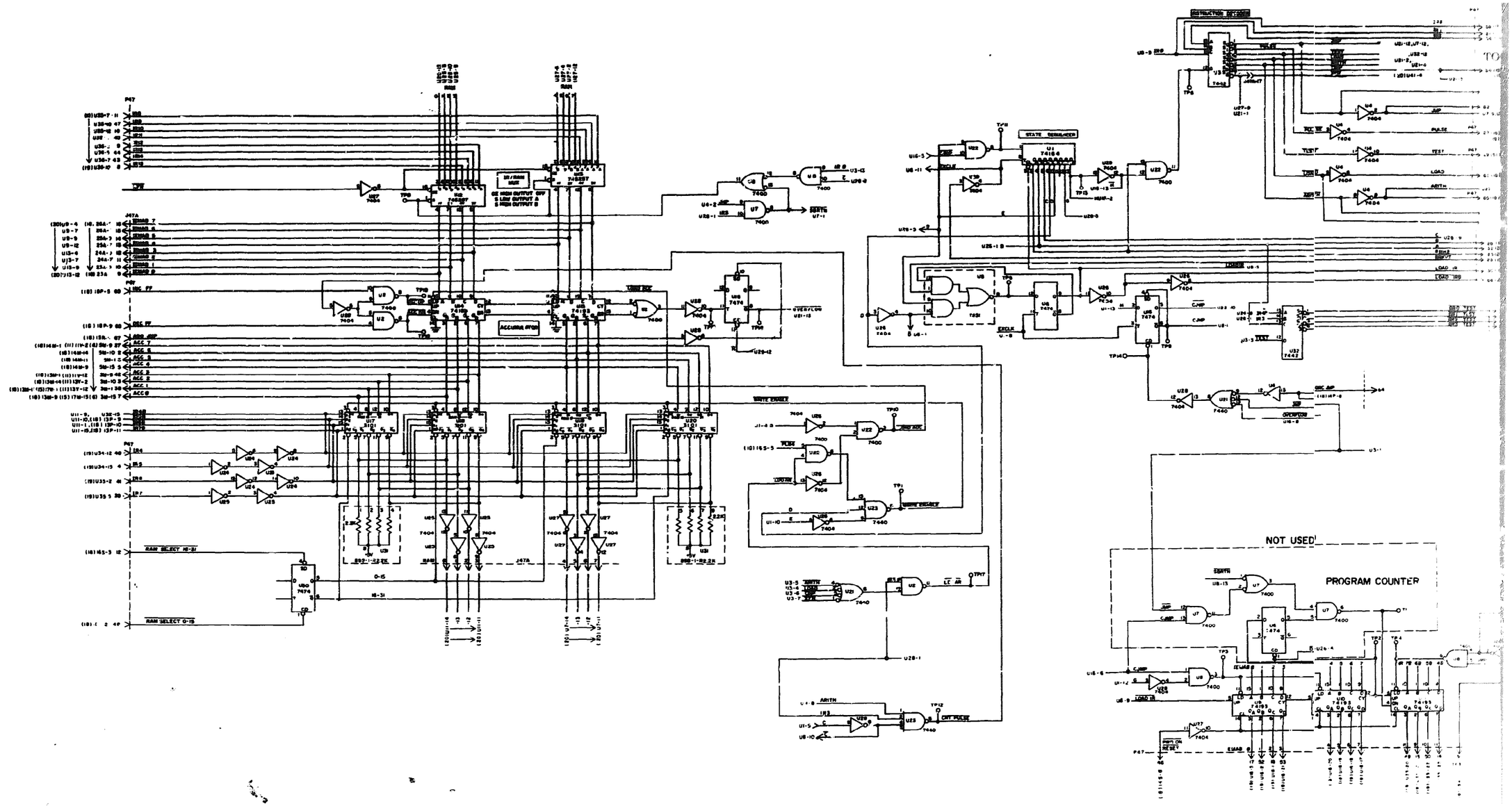


FIGURE A-17
EXECUTIVE MACRO
CONTROLLER (MICROPROCESSOR)

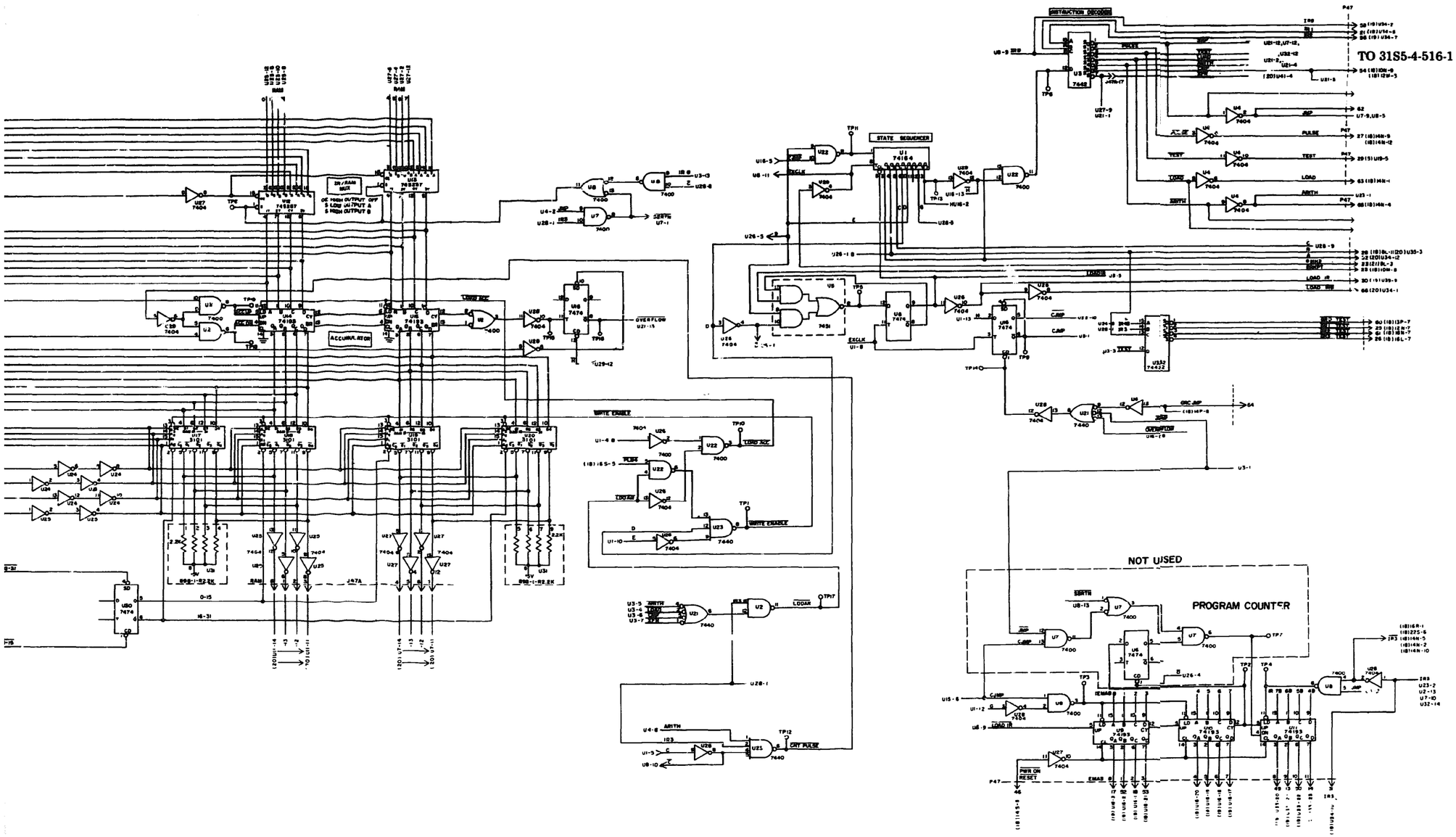
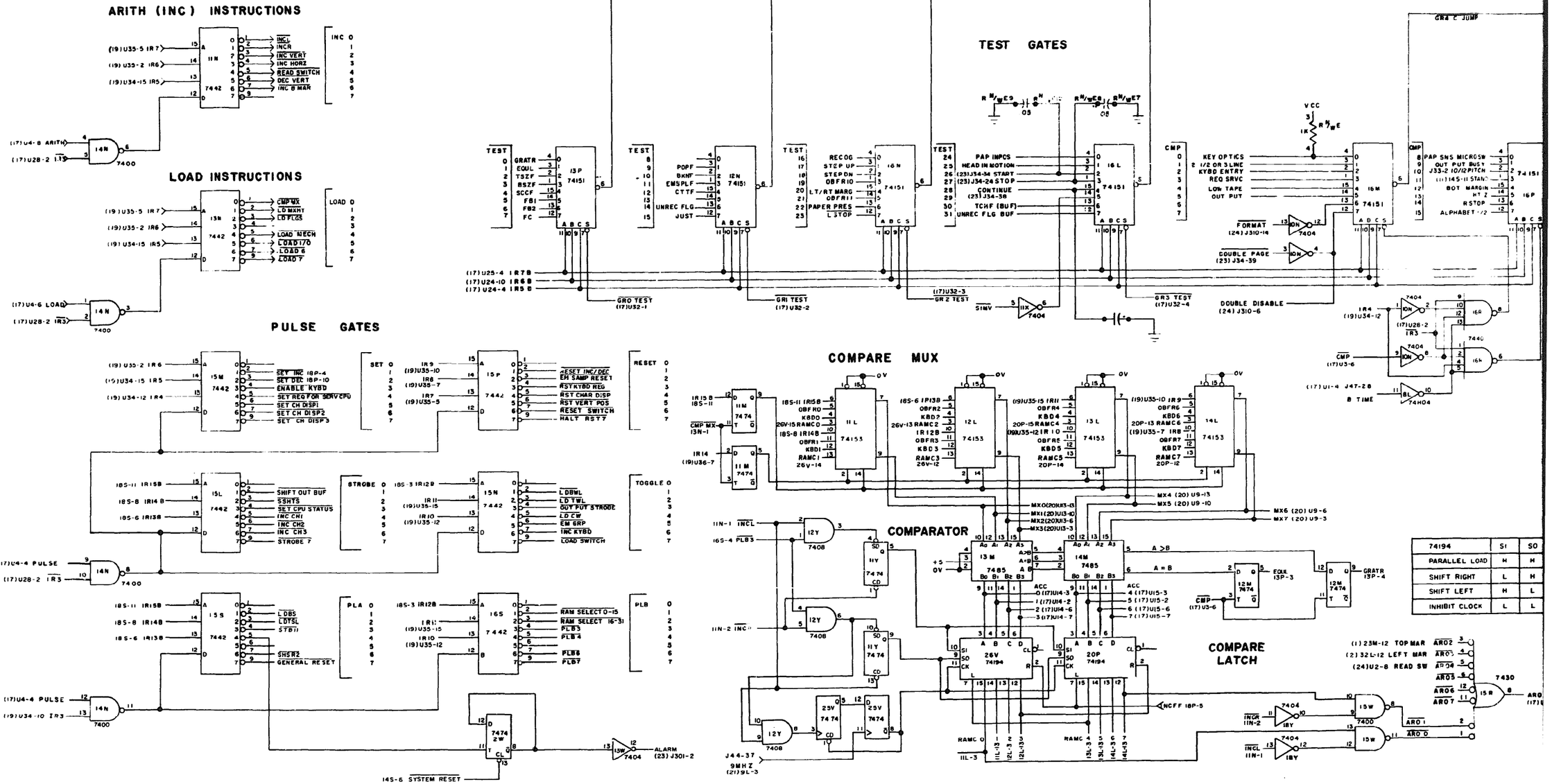
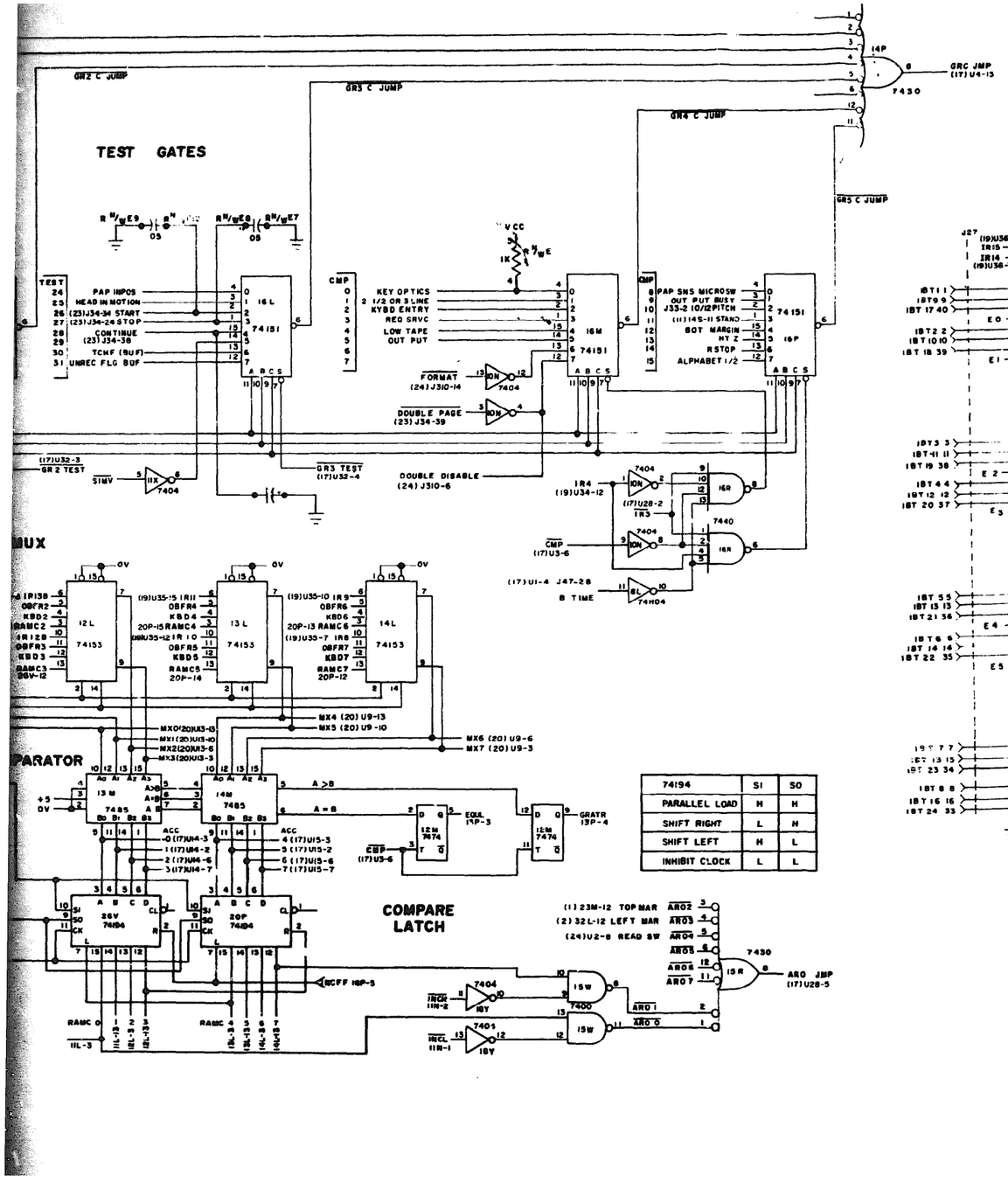
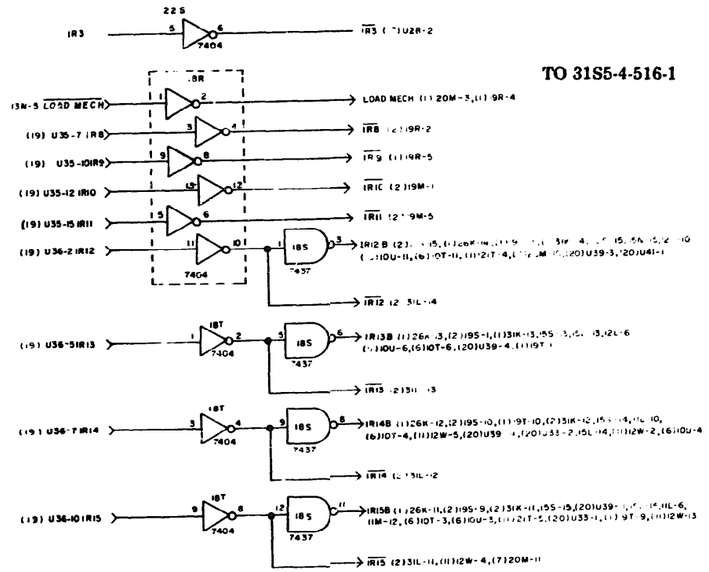


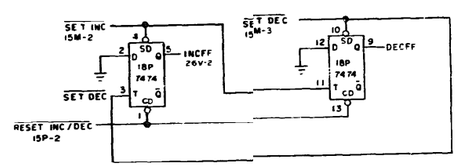
FIGURE A-17
EXECUTIVE MACRO
CONTROLLER (MICROPROCESSOR)
A-33/(A-34 Blank)


ARITH (INC) INSTRUCTIONS
LOAD INSTRUCTIONS
PULSE GATES
TEST GATES
COMPARE MUX
COMPARATOR
COMPARE LATCH
GR0 C JUMP
GR1 C JUMP
GR2 C JUMP
GR3 C JUMP
GR4 C JUMP
GR0 TEST
GR1 TEST
GR2 TEST
GR3 TEST
DOUBLE DISABLE
ALARM
9MHZ
B TIME
74194 S1 S0
PARALLEL LOAD H H
SHIFT RIGHT L H
SHIFT LEFT H L
INHIBIT CLOCK L L



74194	S1	S0
PARALLEL LOAD	H	H
SHIFT RIGHT	L	H
SHIFT LEFT	H	L
INHIBIT CLOCK	L	L





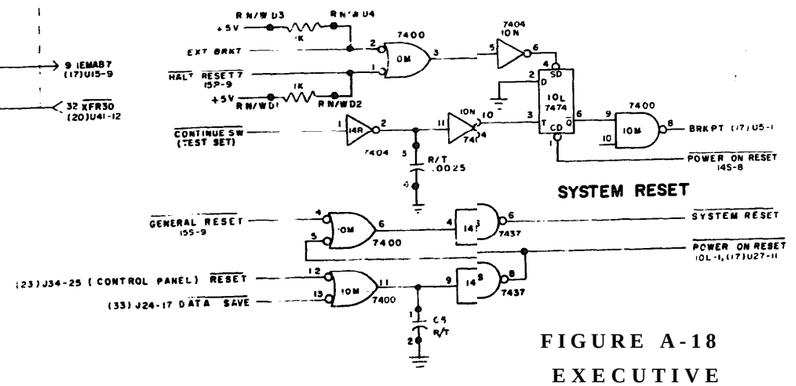
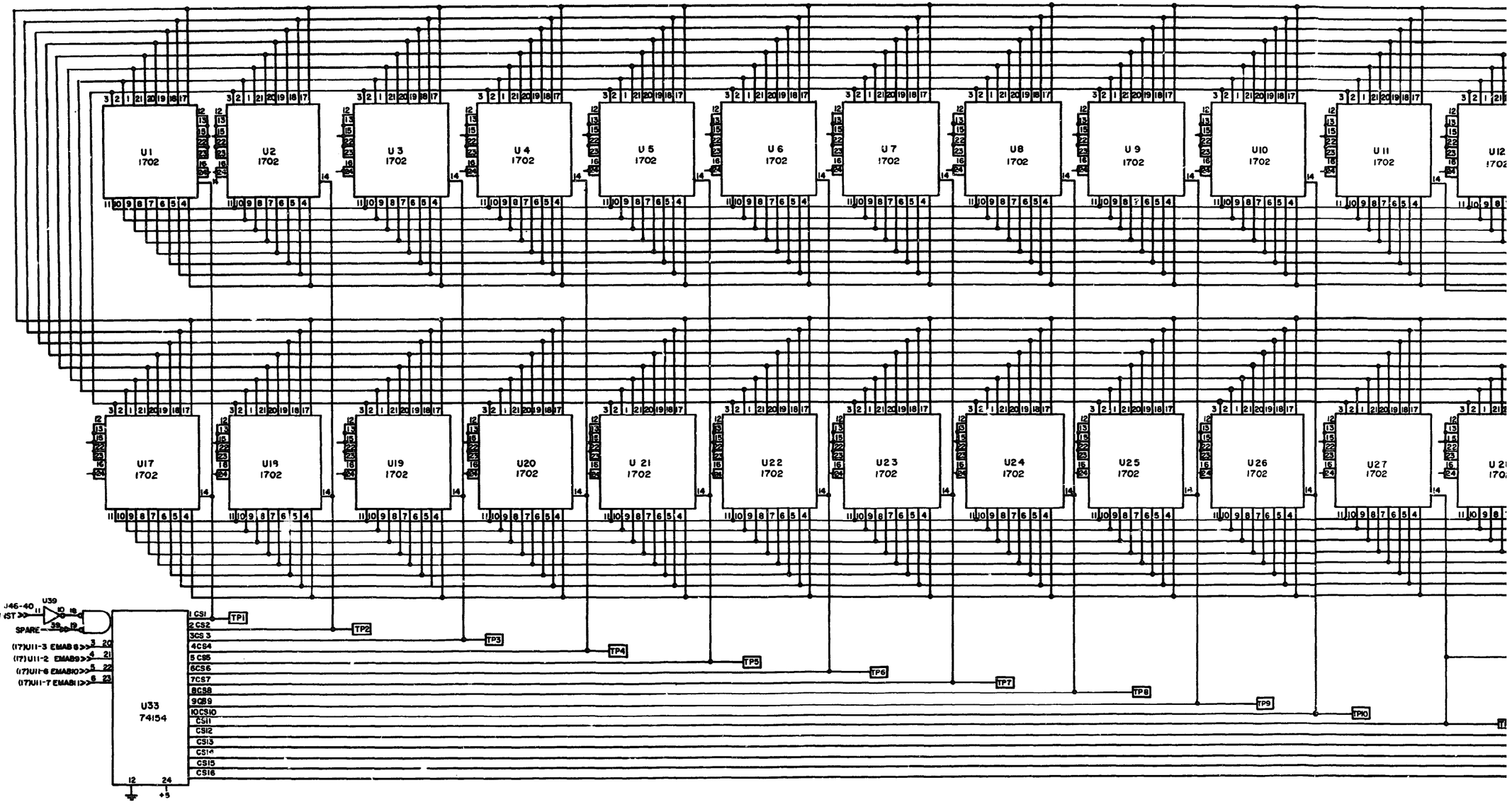
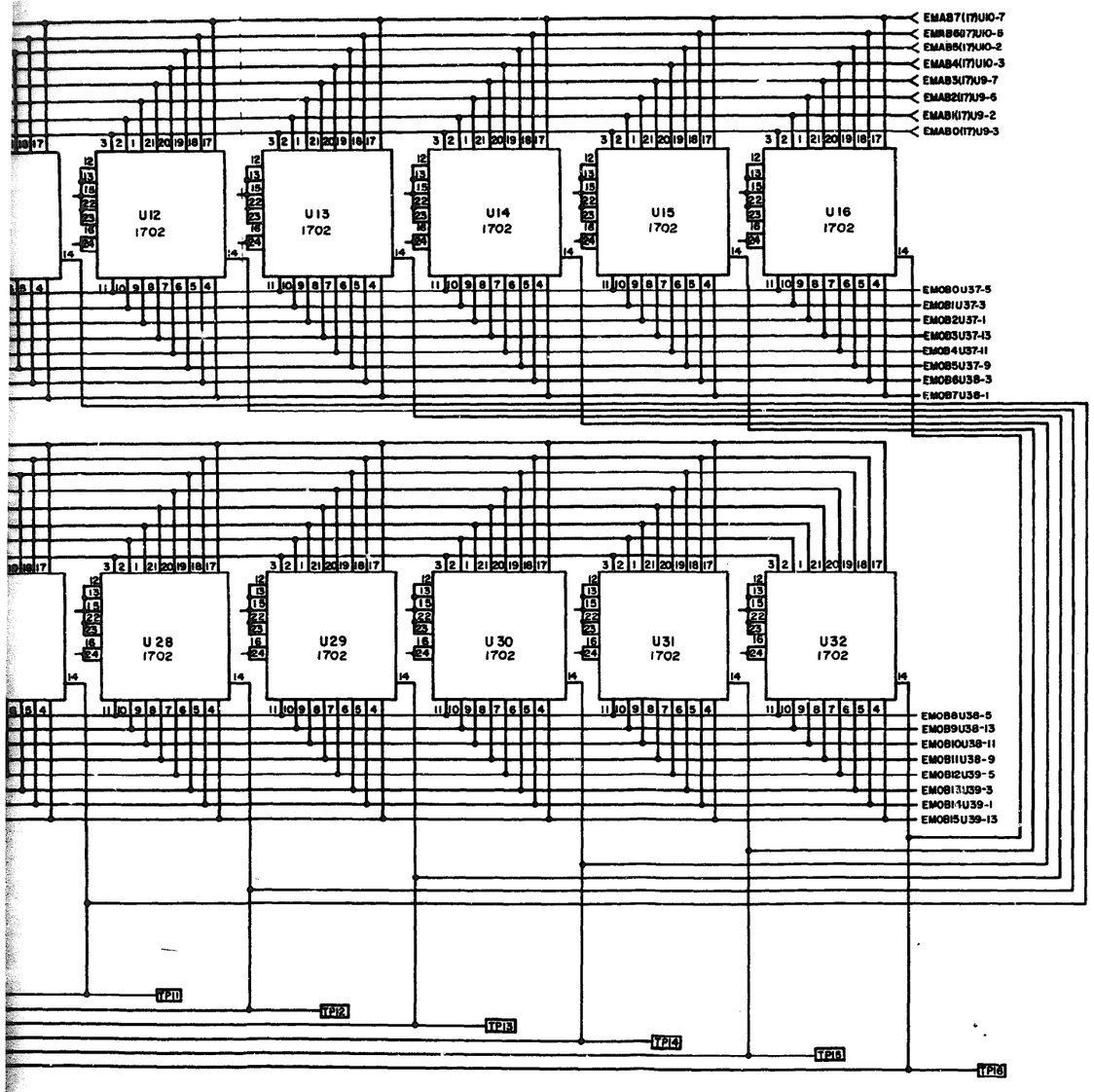


FIGURE A-18

EXECUTIVE MACRO CONTROLLER


U1 1702
U2 1702
U3 1702
U4 1702
U5 1702
U6 1702
U7 1702
U8 1702
U9 1702
U10 1702
U11 1702
U12 1702
U17 1702
U19 1702
U19 1702
U20 1702
U 21 1702
U22 1702
U23 1702
U24 1702
U25 1702
U26 1702
U27 1702
U 21 1702
(FROM TEST SET) EXT TEST >>
J46-40
U39
SPARE
(17)U11-3 EMAB 6 >>
(17)U11-2 EMAB9 >>
(17)U11-6 EMAB10 >>
(17)U11-7 EMAB11 >>
U33 74154
1 CS1
2 CS2
3CS 3
4CS4
5 CS5
6CS6
7CS7
8CS8
9CS9
10CS10
CS11
CS12
CS13
CS14
CS15
CS16
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10



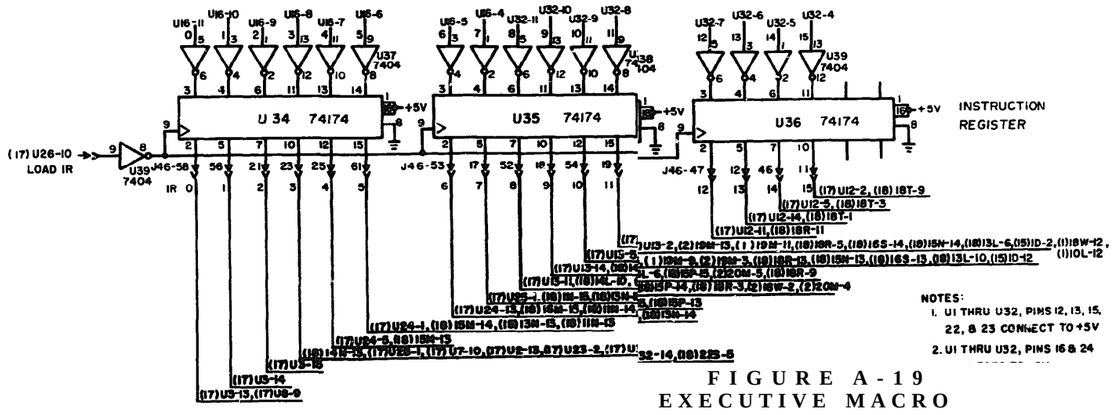
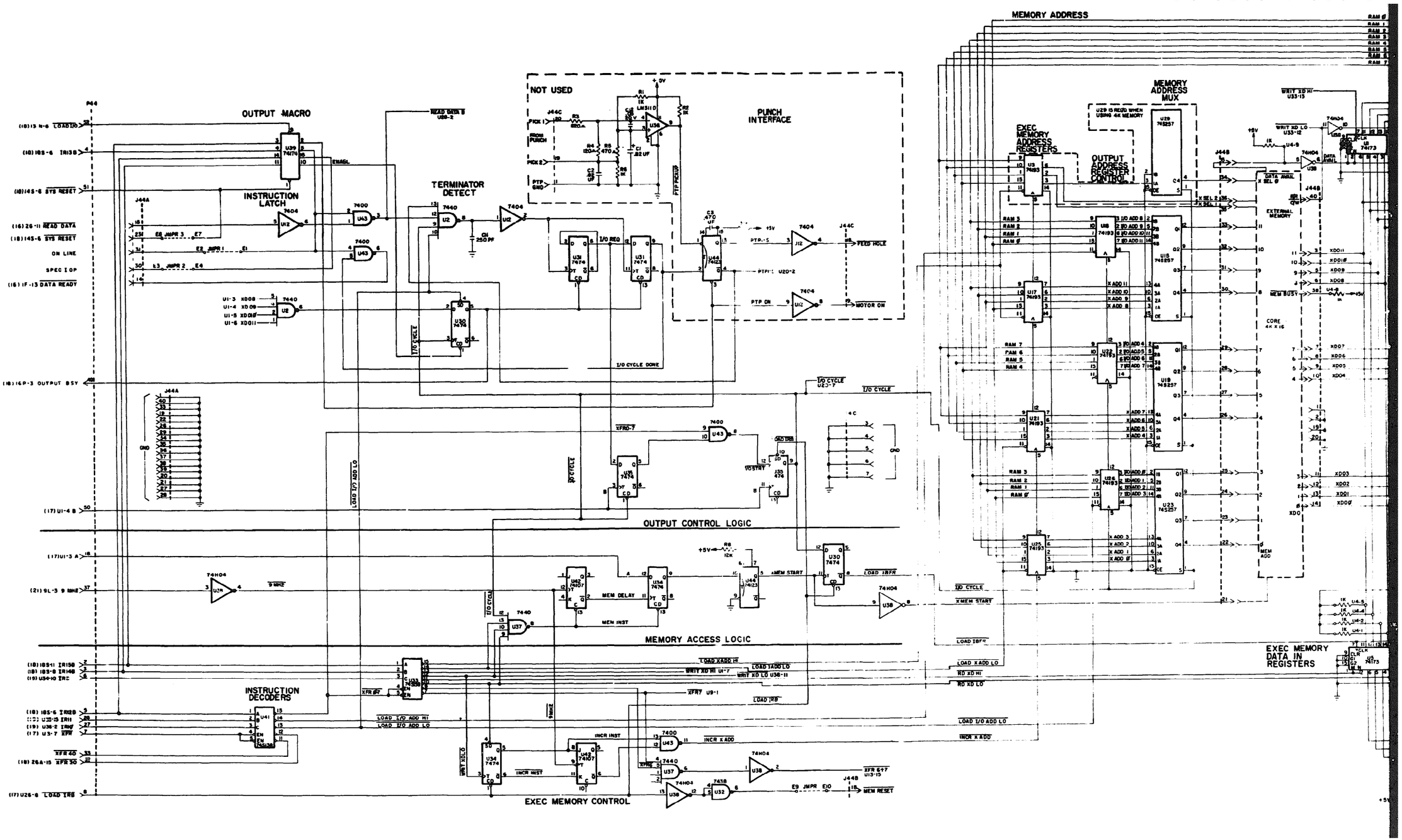


FIGURE A-19
EXECUTIVE MACRO
(PROGRAM) MEMORY


OUTPUT MACRO
INSTRUCTION LATCH
TERMINATOR DETECT
NOT USED
PUNCH INTERFACE
MEMORY ADDRESS
MEMORY ADDRESS MUX
EXEC MEMORY ADDRESS REGISTERS
OUTPUT ADDRESS REGISTER CONTROL
EXTERNAL MEMORY
CORE 4K X 16
OUTPUT CONTROL LOGIC
MEMORY ACCESS LOGIC
EXEC MEMORY CONTROL
INSTRUCTION DECODERS
EXEC MEMORY DATA IN REGISTERS
I/O CYCLE
XMEM START
LOAD IBFR
LOAD XADD HI
LOAD XADD LO
LOAD I/O ADD LO
INCR X ADD
MEM RESET
MEM BUSY
MEM ADD

TO 31S5-4-516-1

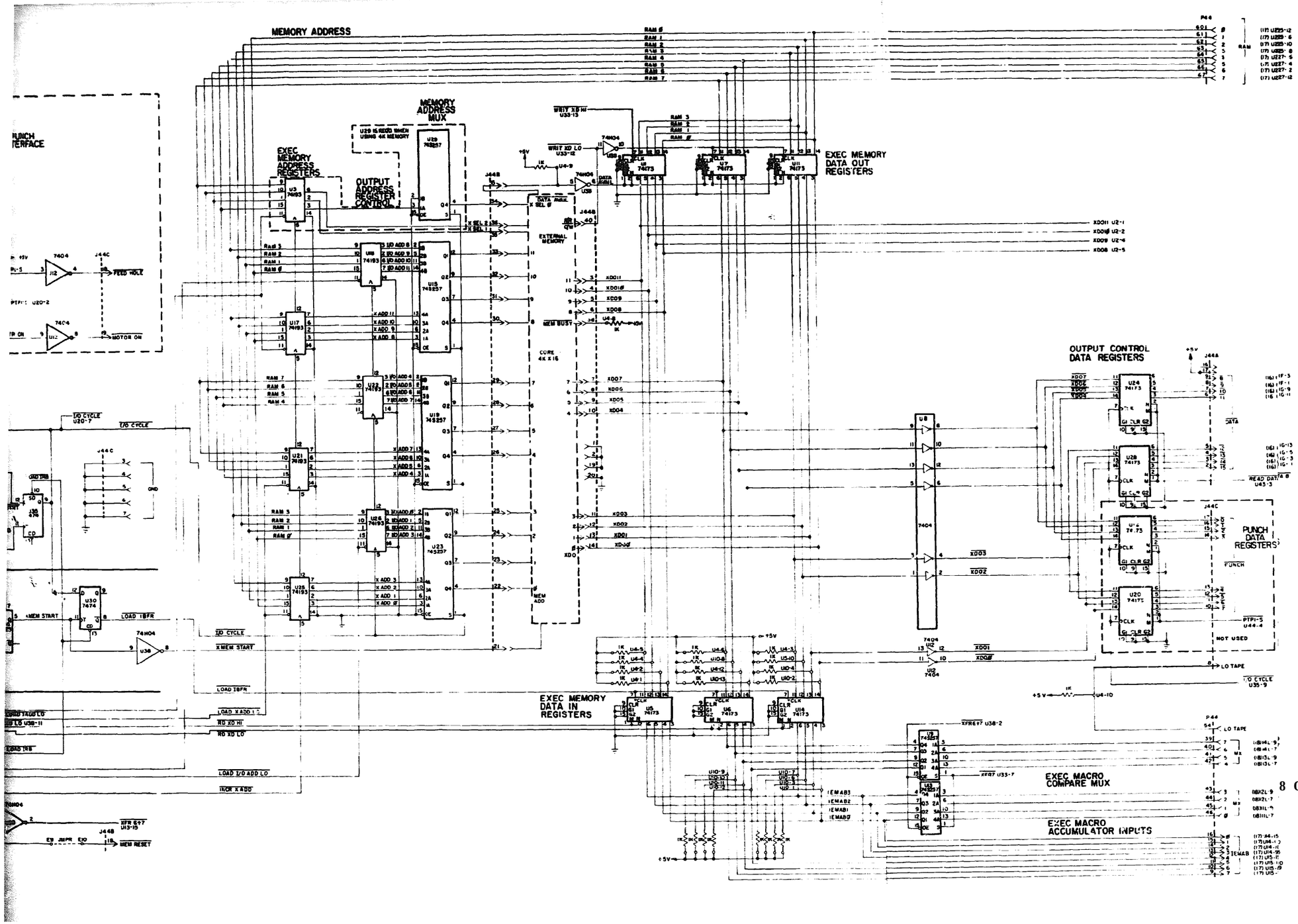
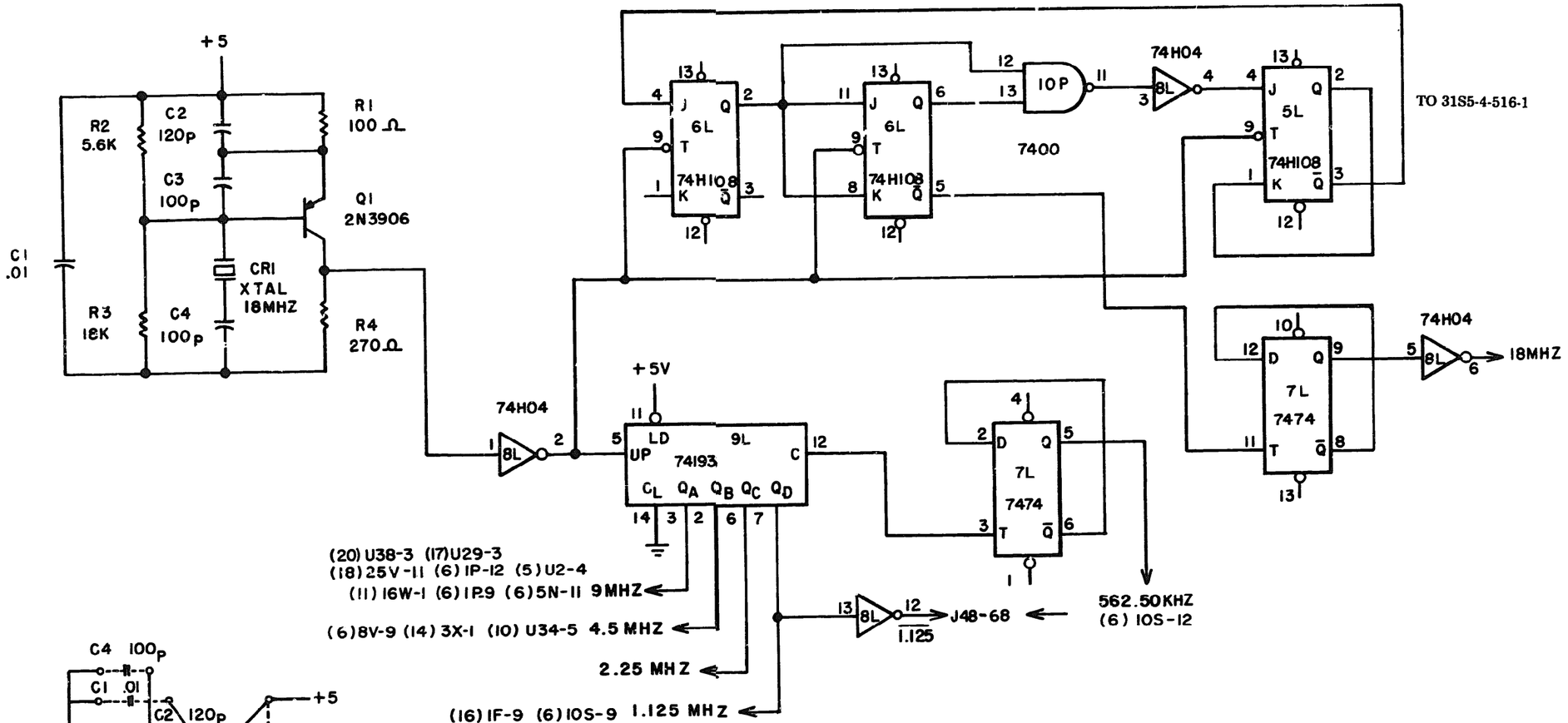
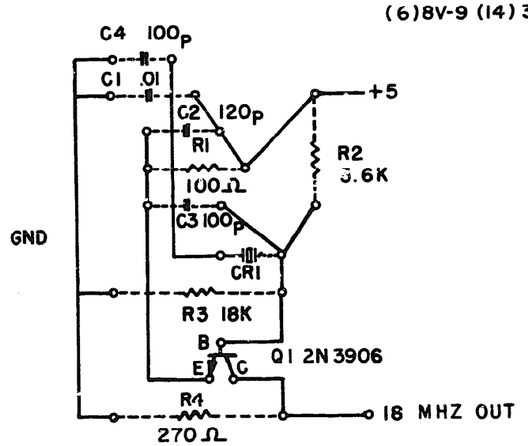


FIGURE A-20
CORE MEMORY
8 OUTPUT CONTROL



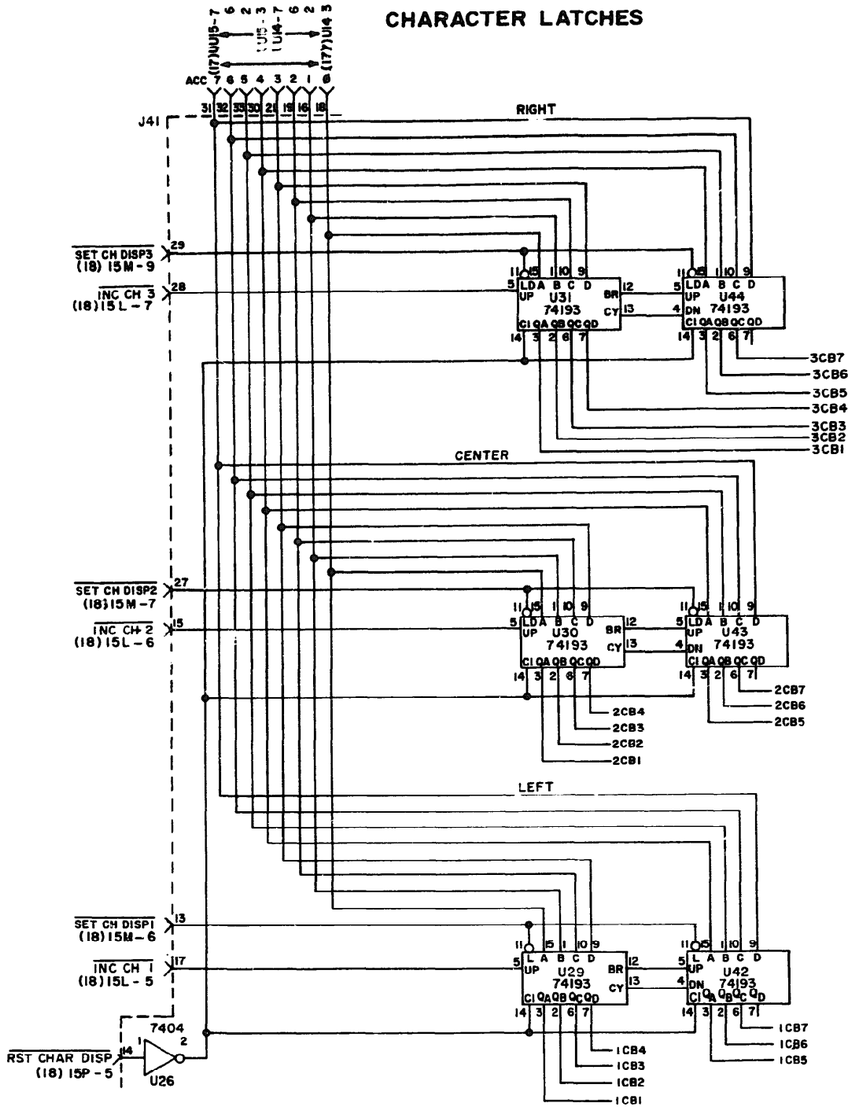


BACK VIEW OF MAIN WIRE WRAP P.C. BD
18MHZ XTAL OSCILLATOR CIRCUIT

FIGURE A-21

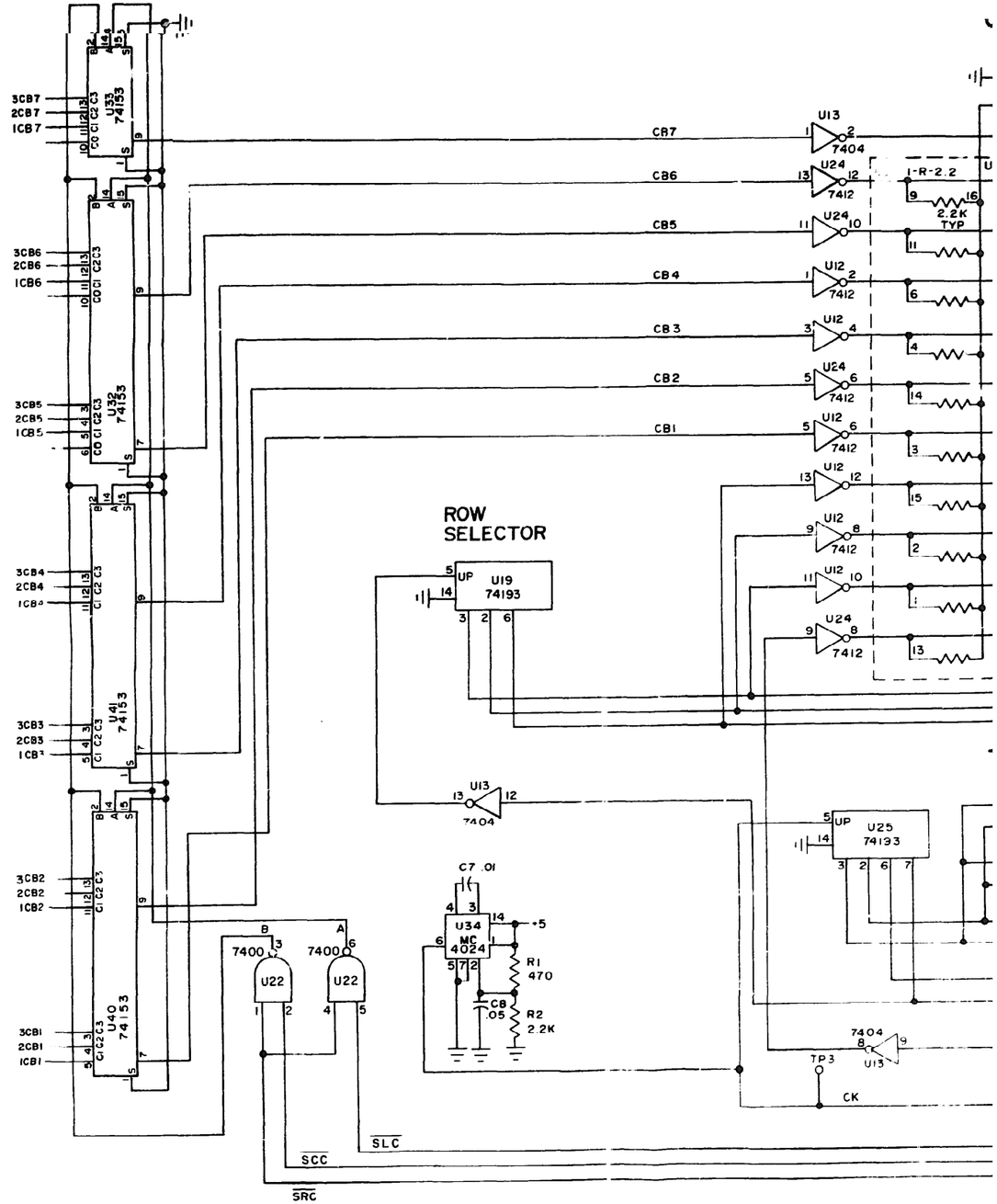
MASTER CLOCK GENERATOR AND DIVIDERS

CHARACTER LATCHES



	A	B
LEFT	1	0
MID	0	1
RIGHT	1	1
177	0	0

CHARACTER MUX



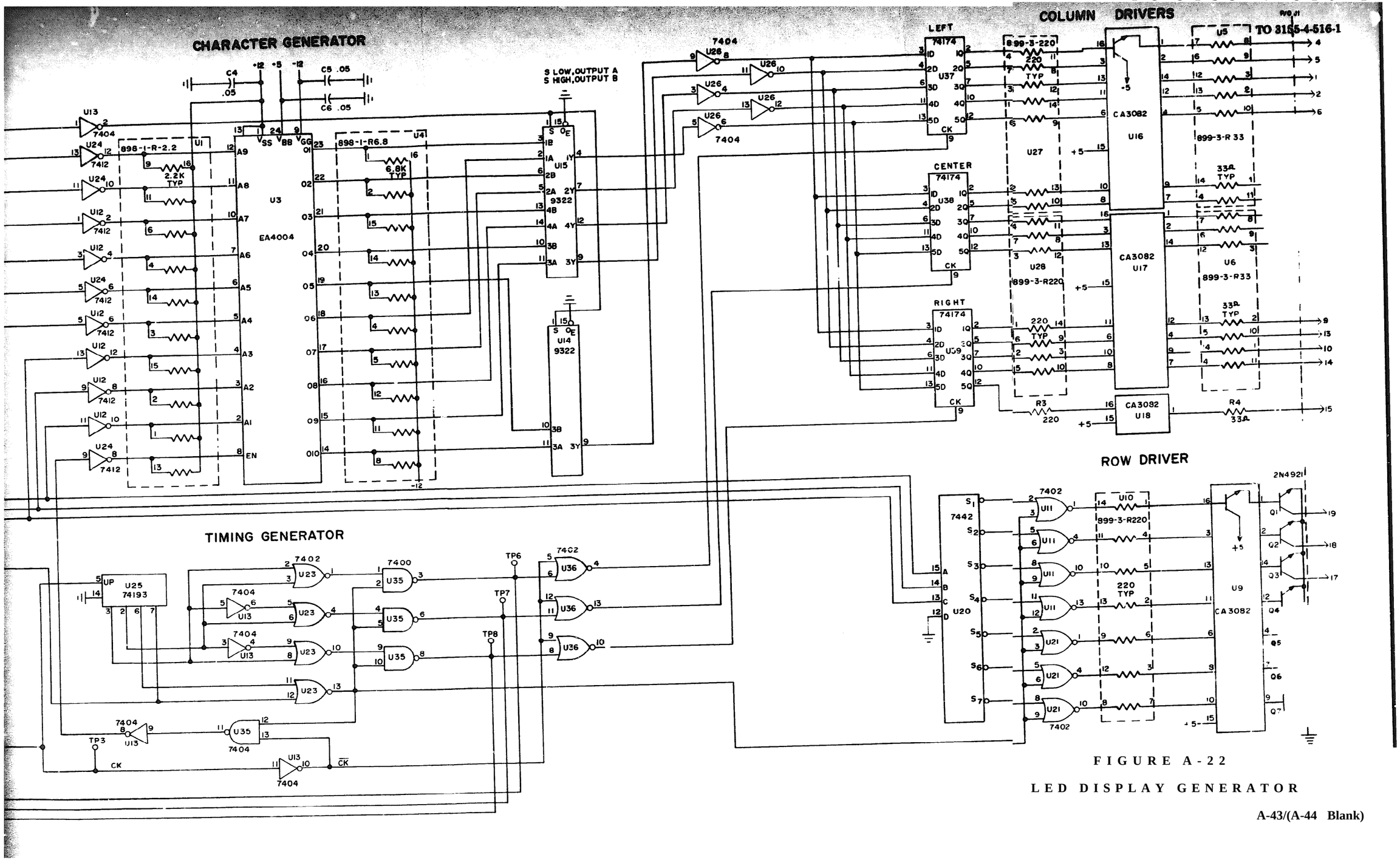


FIGURE A-22

LED DISPLAY GENERATOR

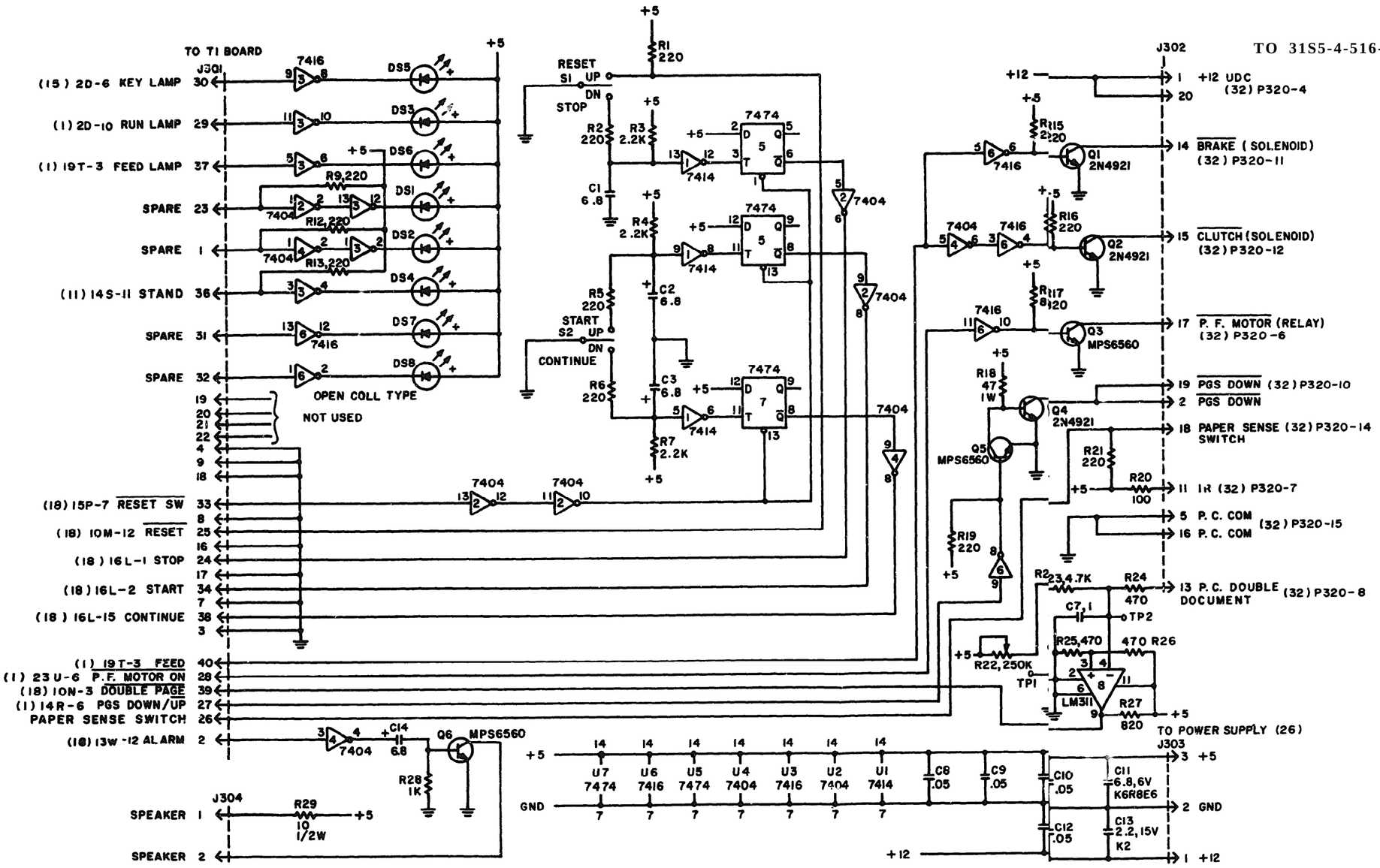
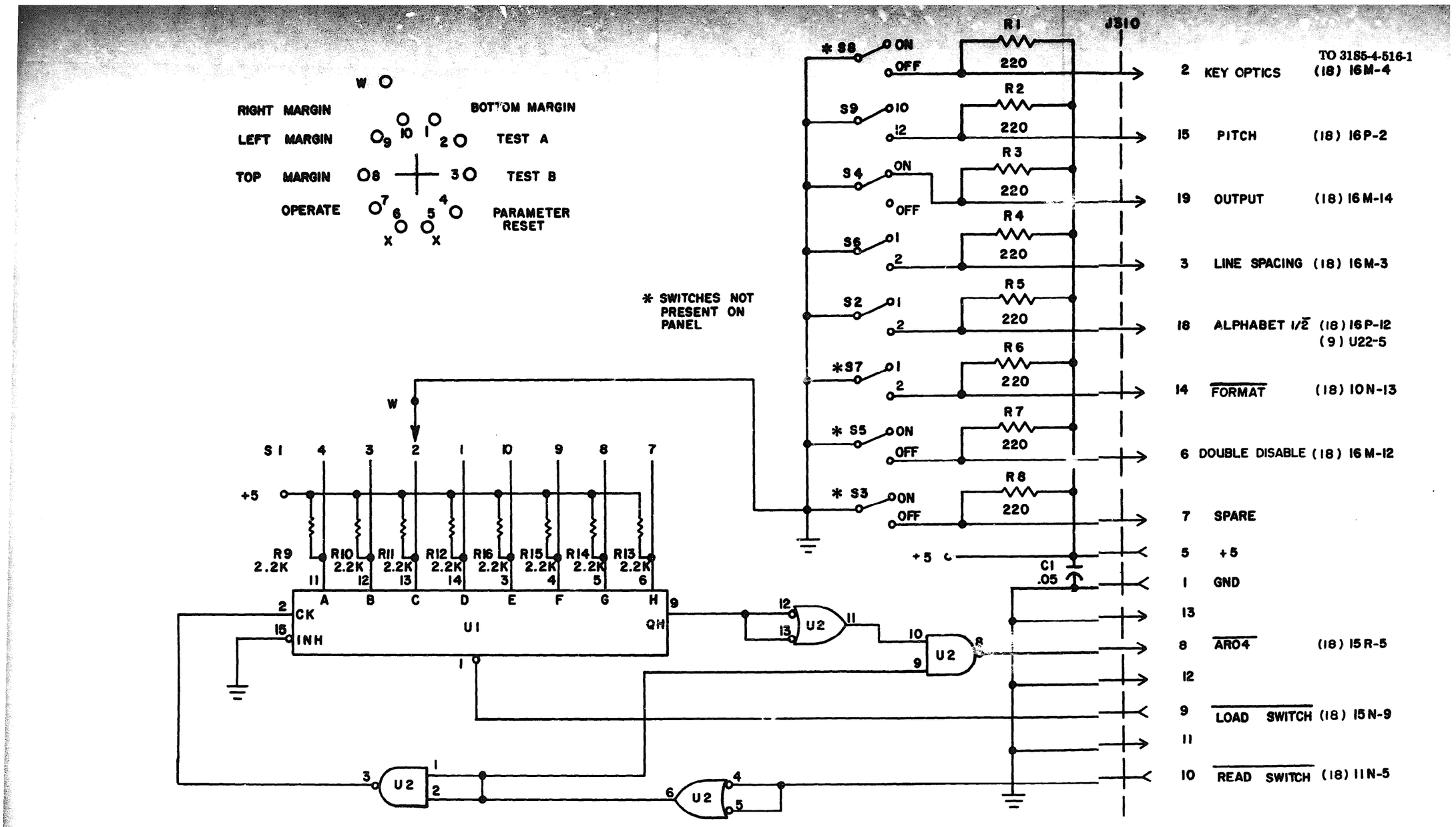


FIGURE A-23

CONTROL PANEL



ALL RESISTORS ARE 1/4 W, ±5%

FIGURE A-24

FORMAT PANEL

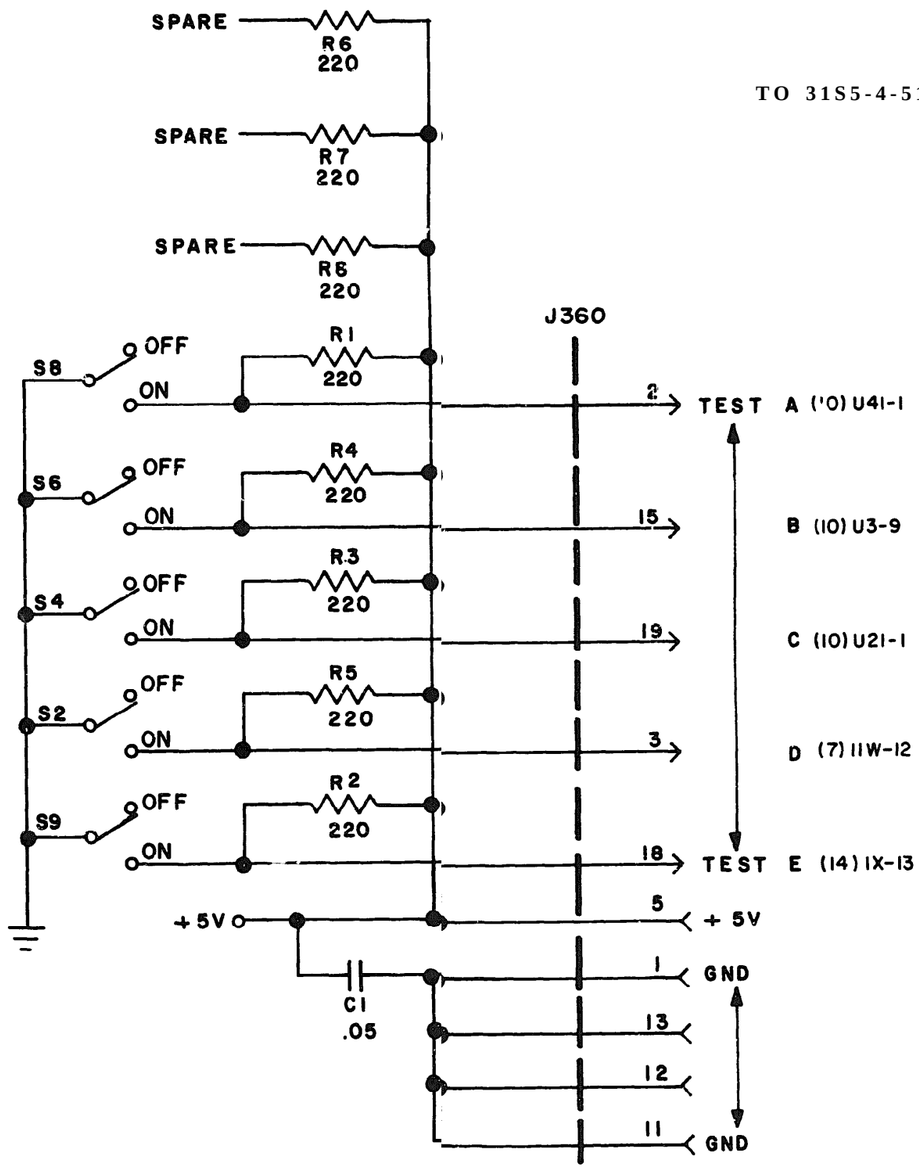
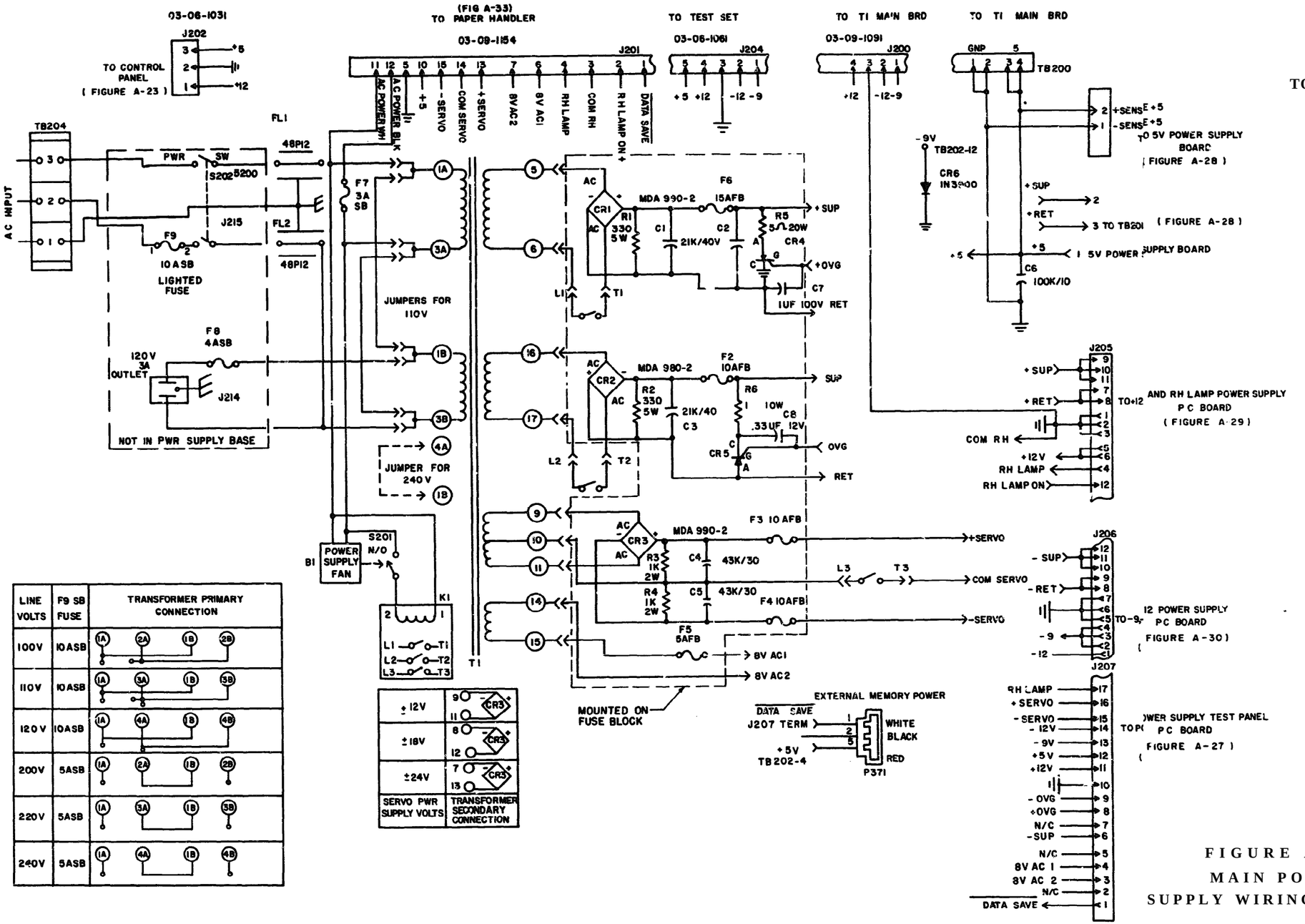


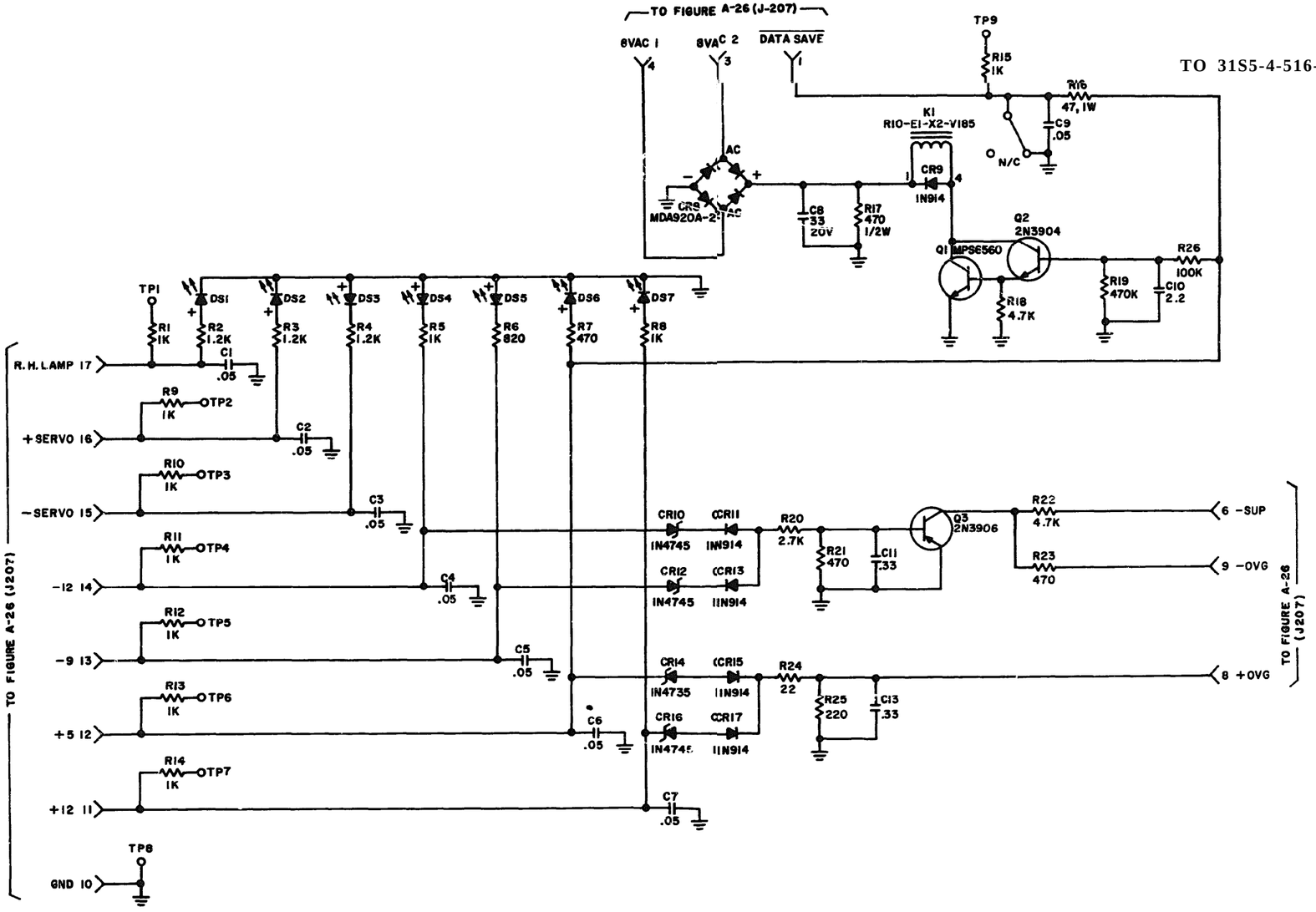
FIGURE A-25

RAD TEST PANEL



LINE VOLTS	F9 SB FUSE	TRANSFORMER PRIMARY CONNECTION
100V	10ASB	1A 2A 1B 2B
110V	10ASB	1A 3A 1B 3B
120V	10ASB	1A 4A 1B 4B
200V	5ASB	1A 2A 1B 2B
220V	5ASB	1A 3A 1B 3B
240V	5ASB	1A 4A 1B 4B

FIGURE A-26
MAIN POWER
SUPPLY WIRING DIAGRAM



NOTES:
1. * VALUE SELECTED AT TEST
2. DS1 THRU DS7 ARE LED 521-9165
3. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTOR VALUES ARE IN OHMS, 1/4W @ ±5%
   B. ALL CAPACITOR VALUES ARE IN MICROFARADS

FIGURE A-27

DATA SAVE SUPPLY TEST PANEL

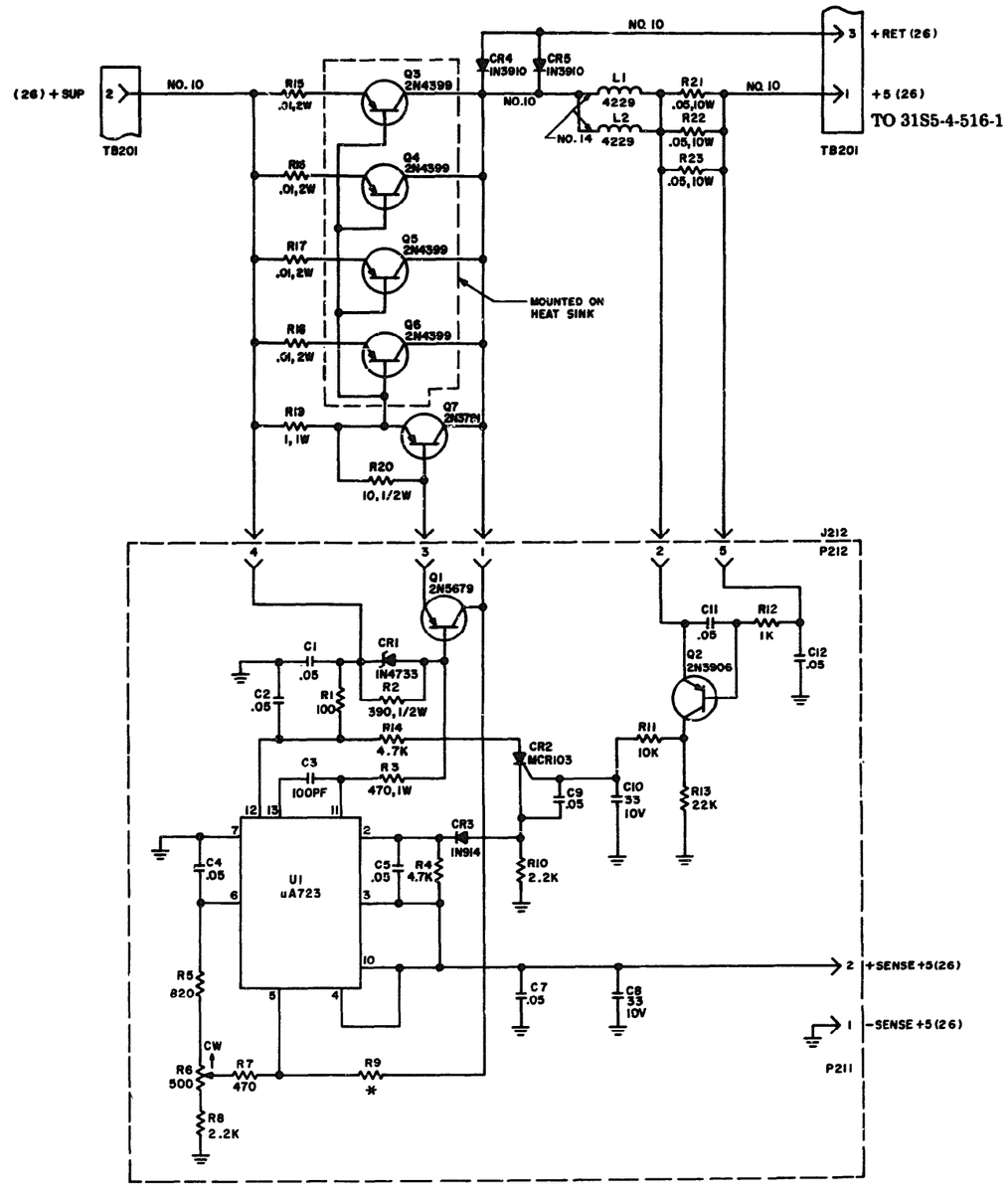
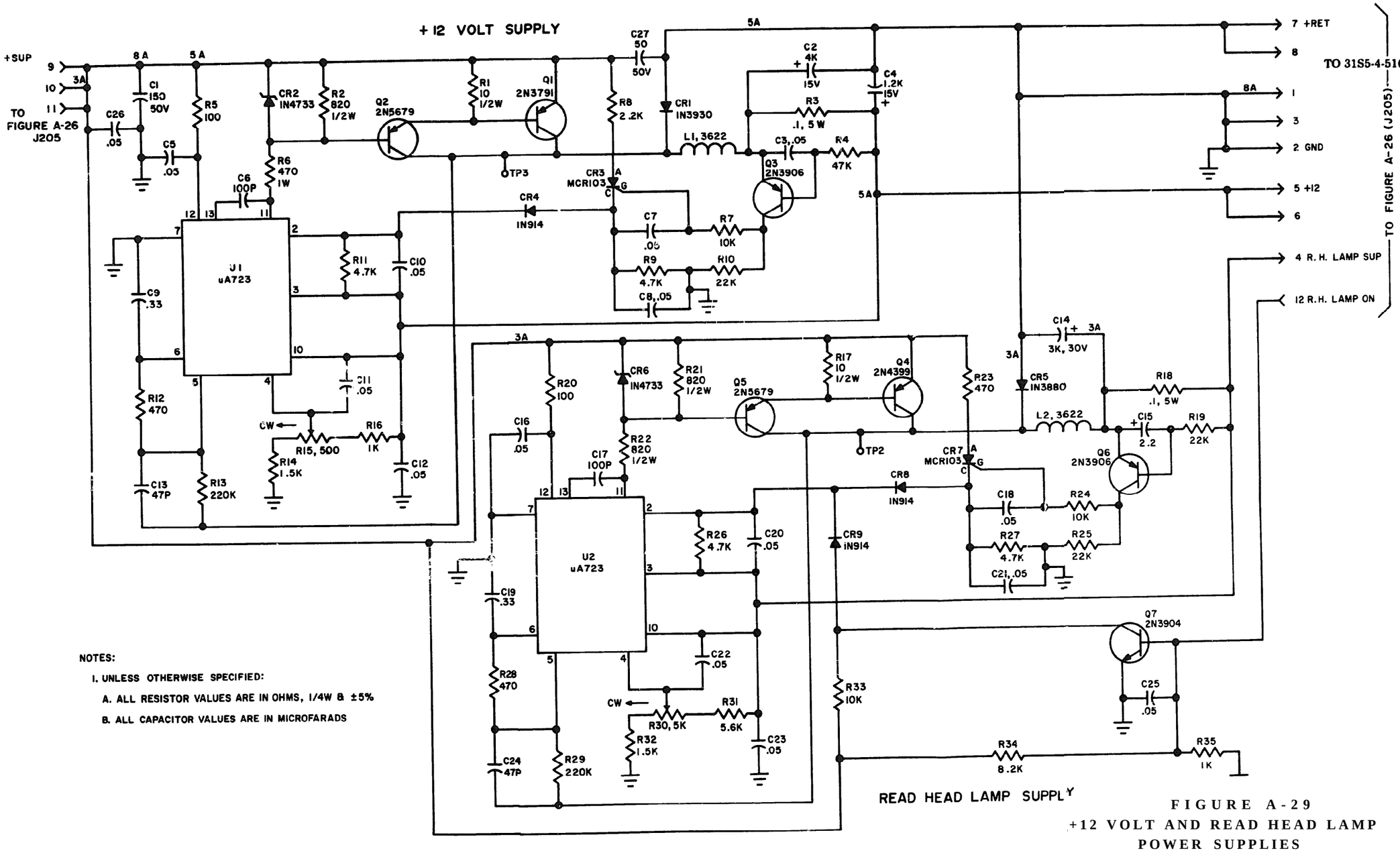


FIGURE A-28

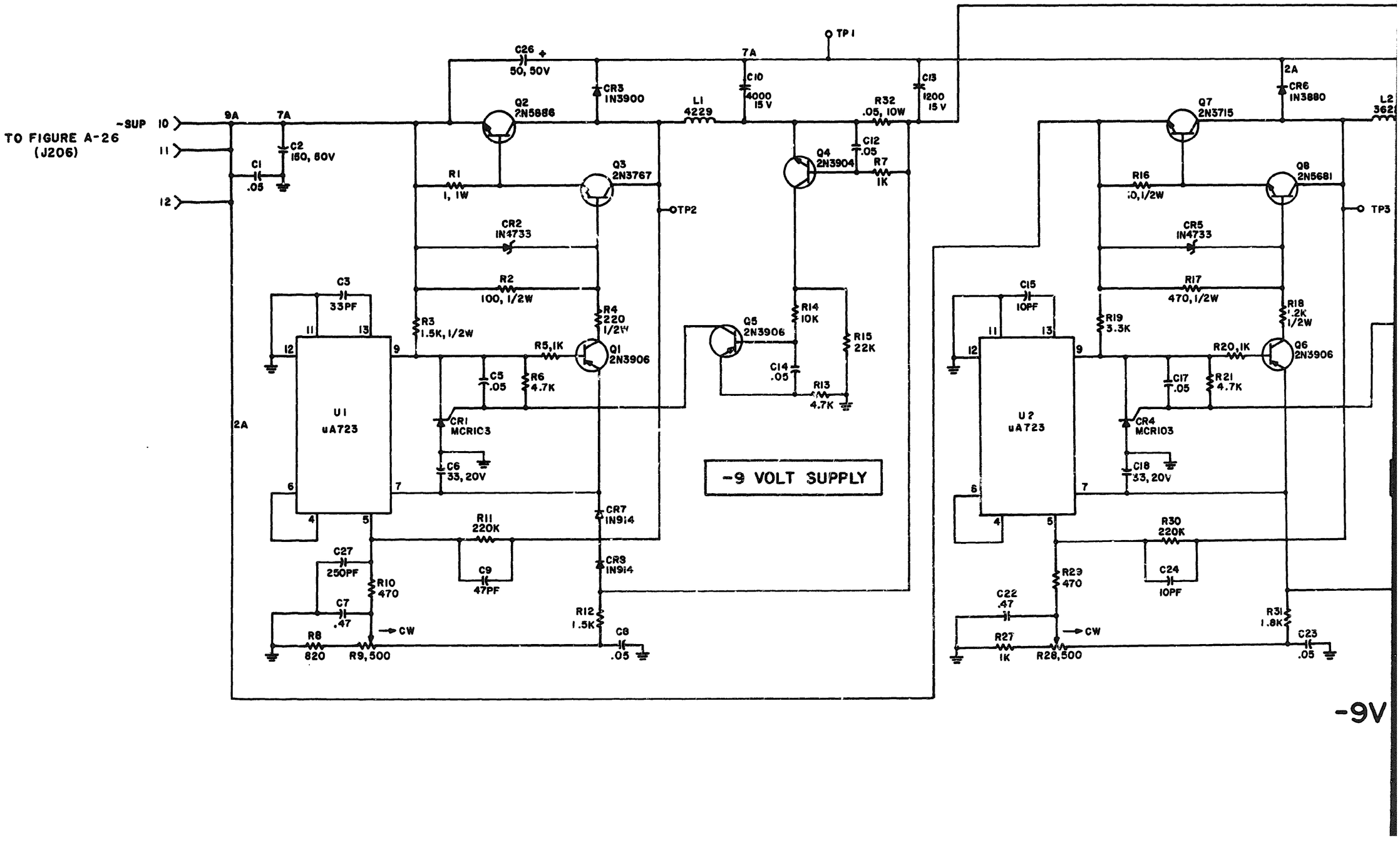
+5 VOLT POWER SUPPLY



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. ALL RESISTOR VALUES ARE IN OHMS, 1/4W & ±5%
   - B. ALL CAPACITOR VALUES ARE IN MICROFARADS

FIGURE A-29
+12 VOLT AND READ HEAD LAMP POWER SUPPLIES


TO FIGURE A-26
(J206)
-SUP
10
11
12
9A
7A
2A
C1
.05
C2
180, 60V
C26
50, 50V
Q2
2N5886
CR3
IN3900
L1
4229
C10
4000
15V
TP1
C13
1200
15V
R32
.05, 10W
C12
.05
Q4
2N3904
R7
1K
R1
1, 1W
Q3
2N3767
TP2
CR2
IN4733
R2
100, 1/2W
C3
33PF
R3
1.5K, 1/2W
R4
220
1/2W
R5, 1K
Q1
2N3906
C5
.05
R6
4.7K
Q5
2N3906
R14
10K
R15
22K
C14
.05
R13
4.7K
U1
uA723
CR1
MCR1C3
C6
33, 20V
R11
220K
C9
47PF
CR7
IN914
CR8
IN914
C27
250PF
R10
470
C7
.47
R8
820
R9, 500
CW
R12
1.5K
C8
.05
-9 VOLT SUPPLY
Q7
2N3715
CR6
IN3880
L2
362
R16
:0, 1/2W
Q8
2N5681
TP3
CR5
IN4733
R17
470, 1/2W
C15
10PF
R19
3.3K
R18
1.2K
1/2W
R20, 1K
Q6
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U2
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C18
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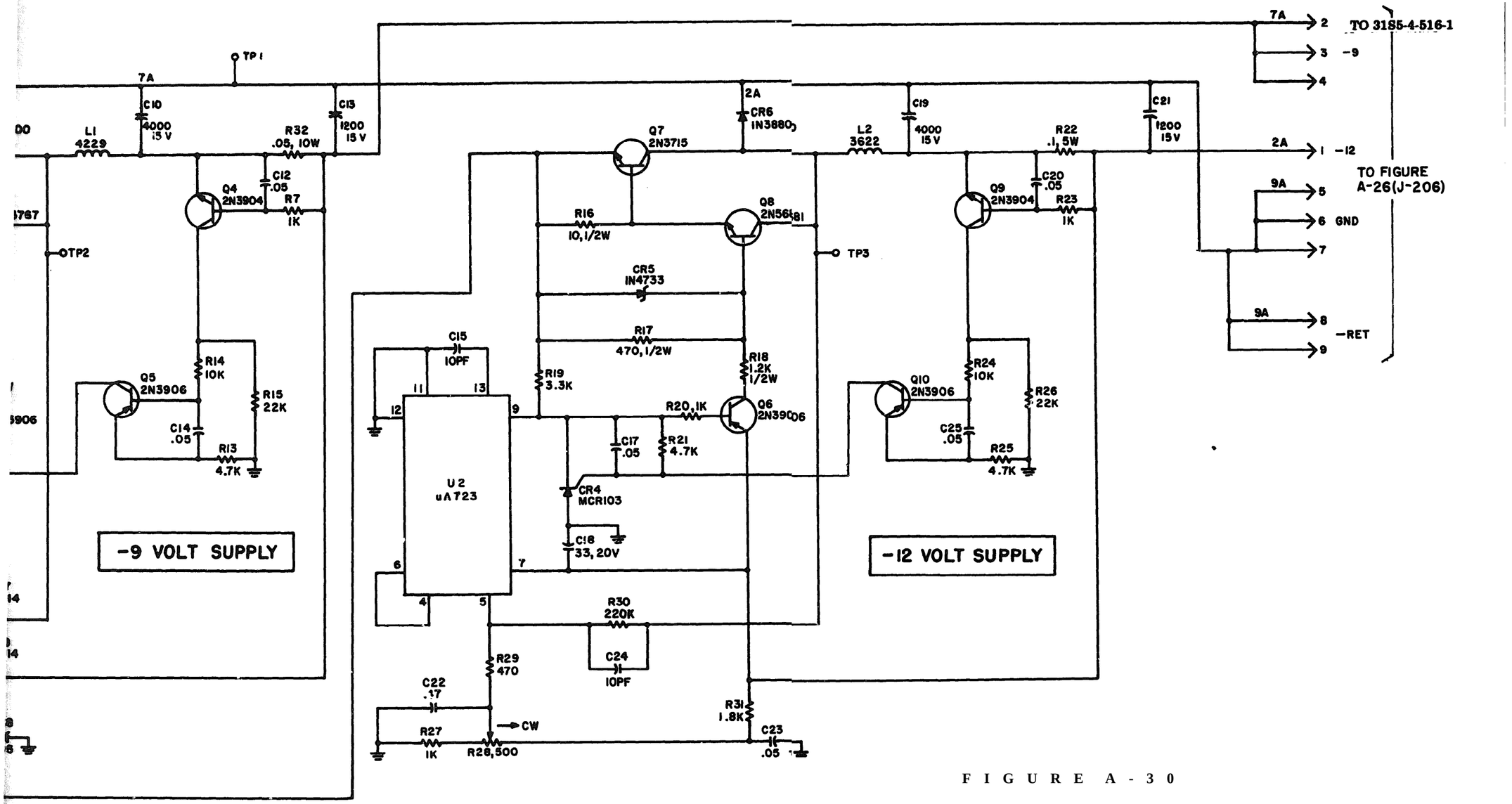

F I G U R E A - 3 0

- 9 V A N D - 1 2 V P O W E R S U P P L I E S

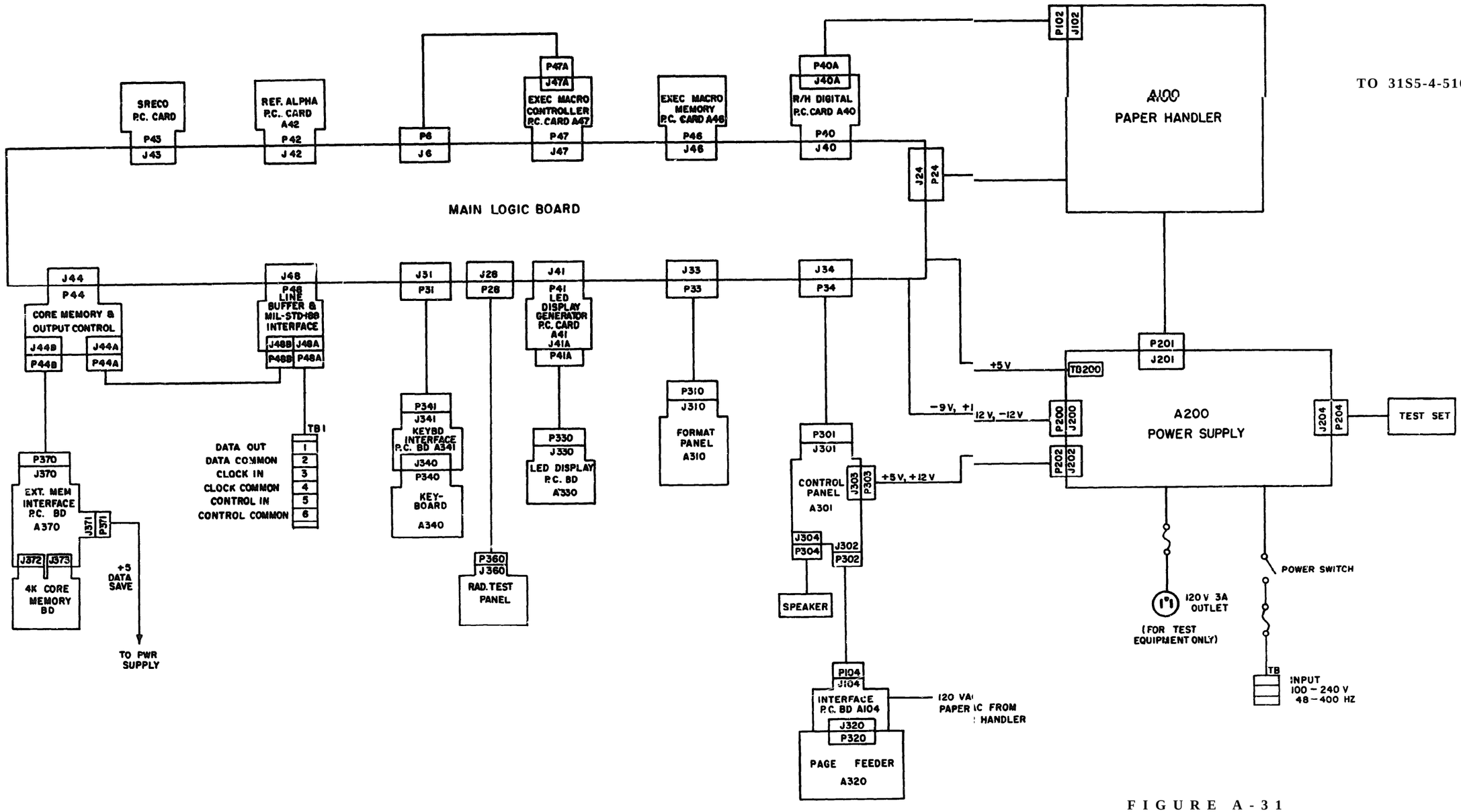

FIGURE A-31

MAIN FRAME WIRING DIAGRAM

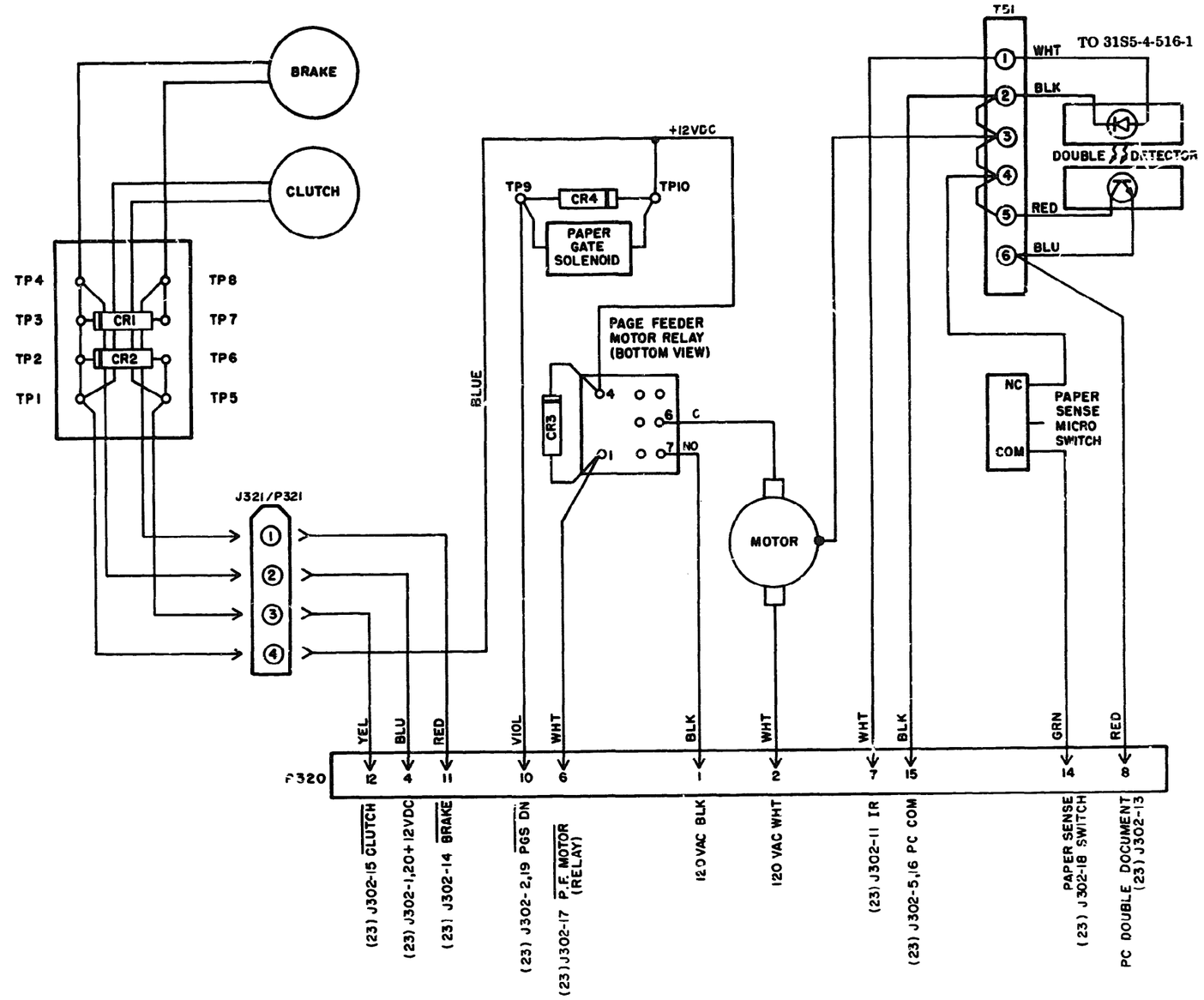

FIGURE A-32

PAGE FEEDER WIRING DIAGRAM

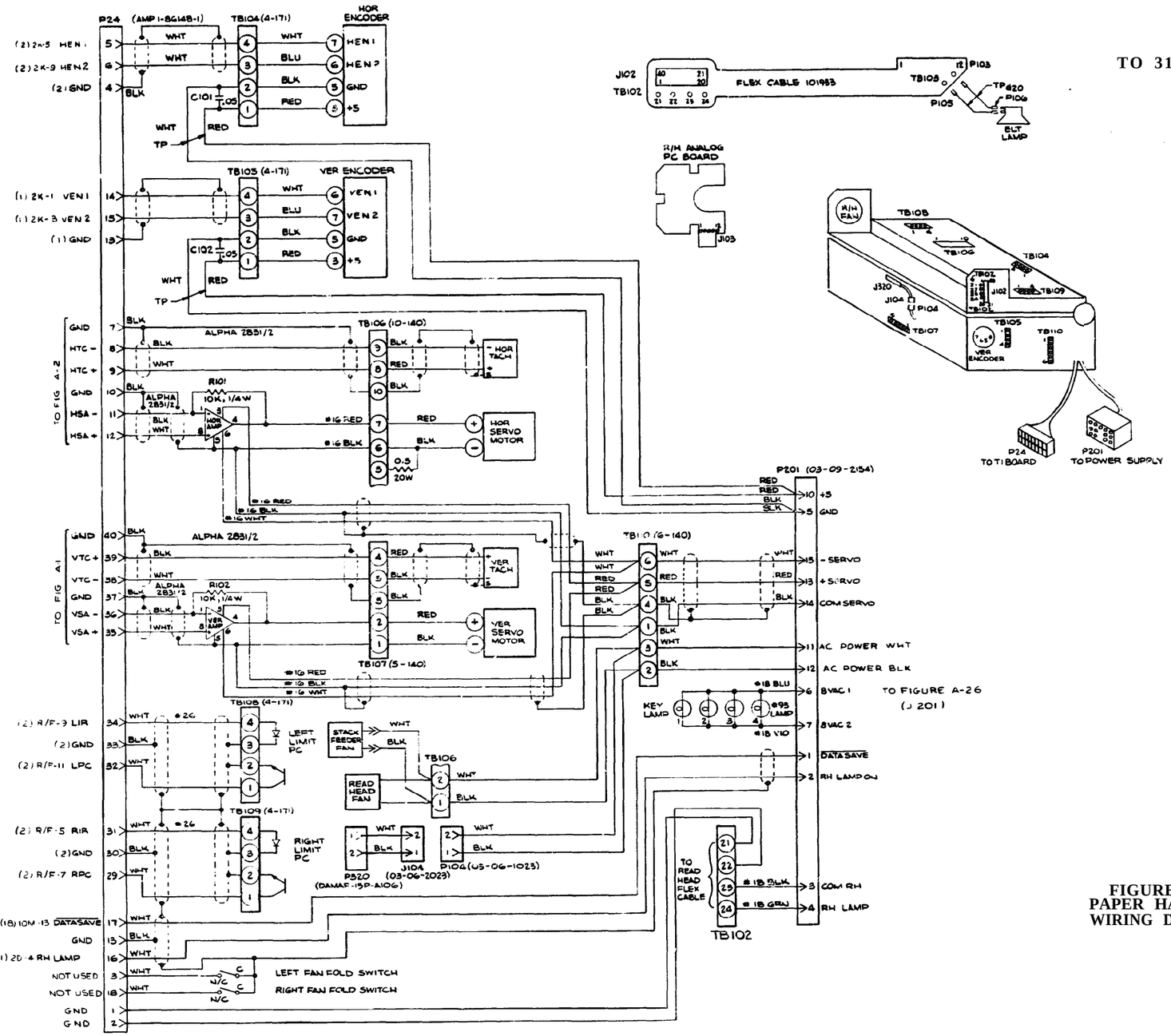

FIGURE A-33
PAPER HANDLER
WIRING DIAGRAM

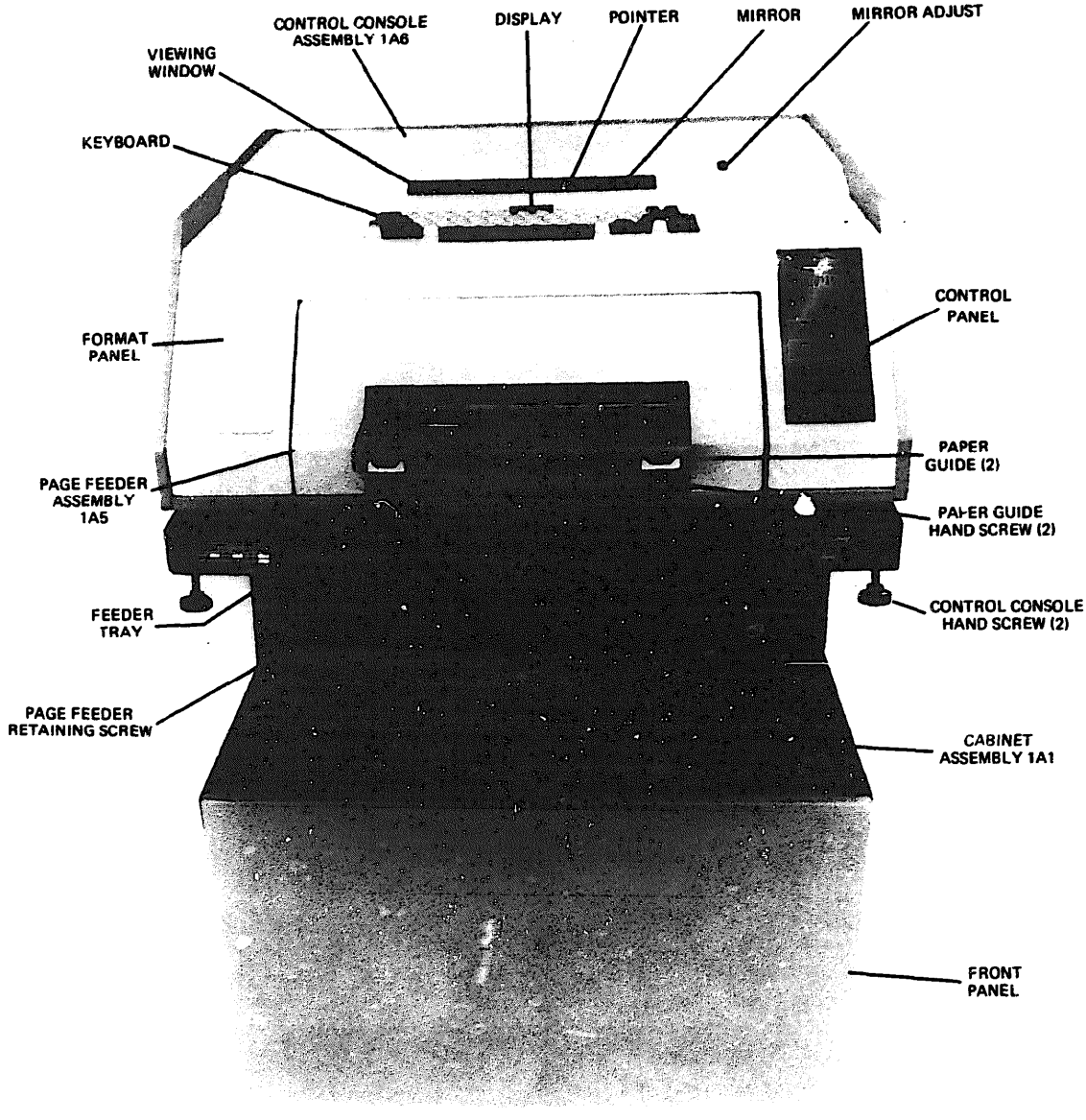

Figure A-34. ALPHA Front View

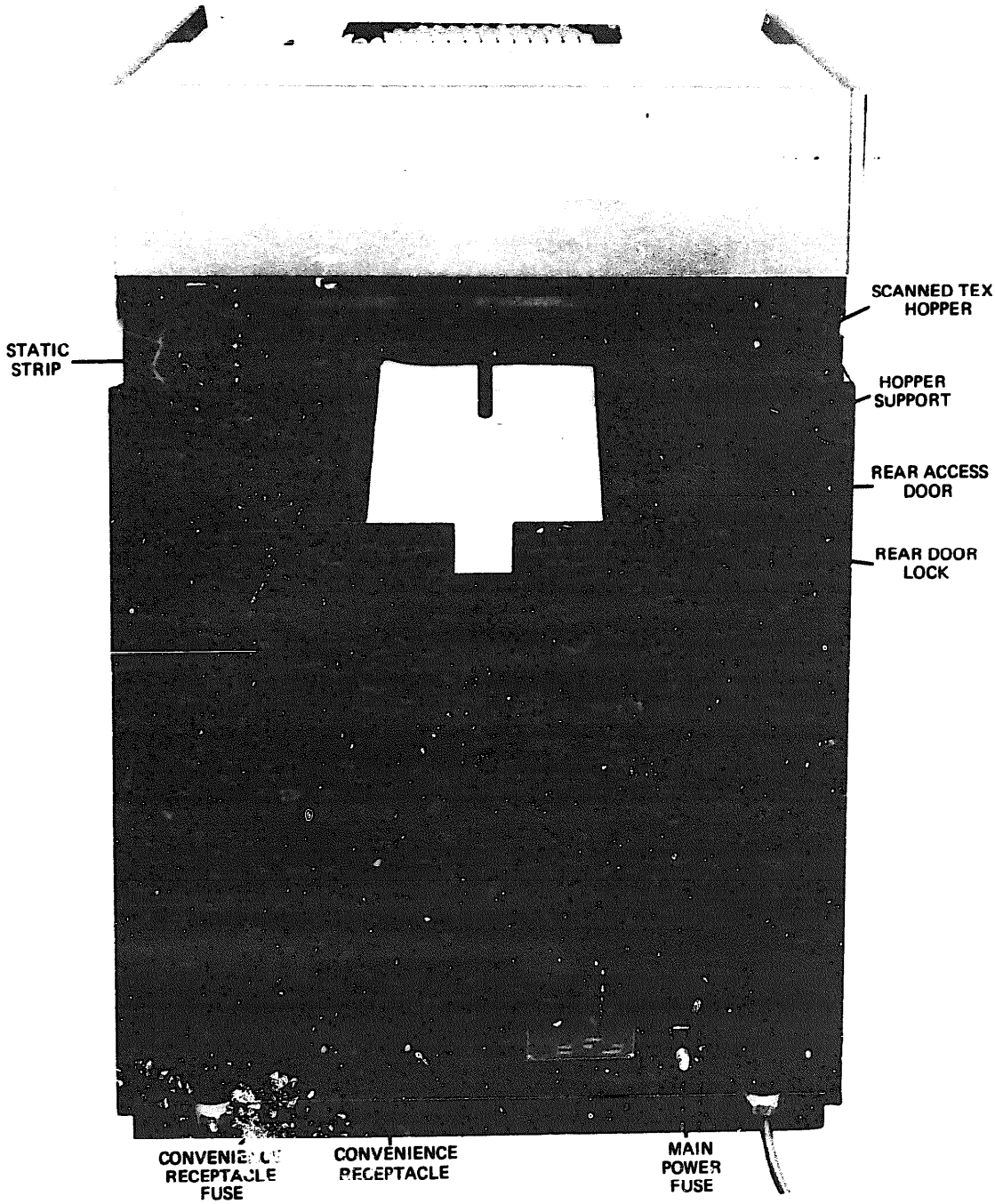

Figure A-35. ALPHA Rear View

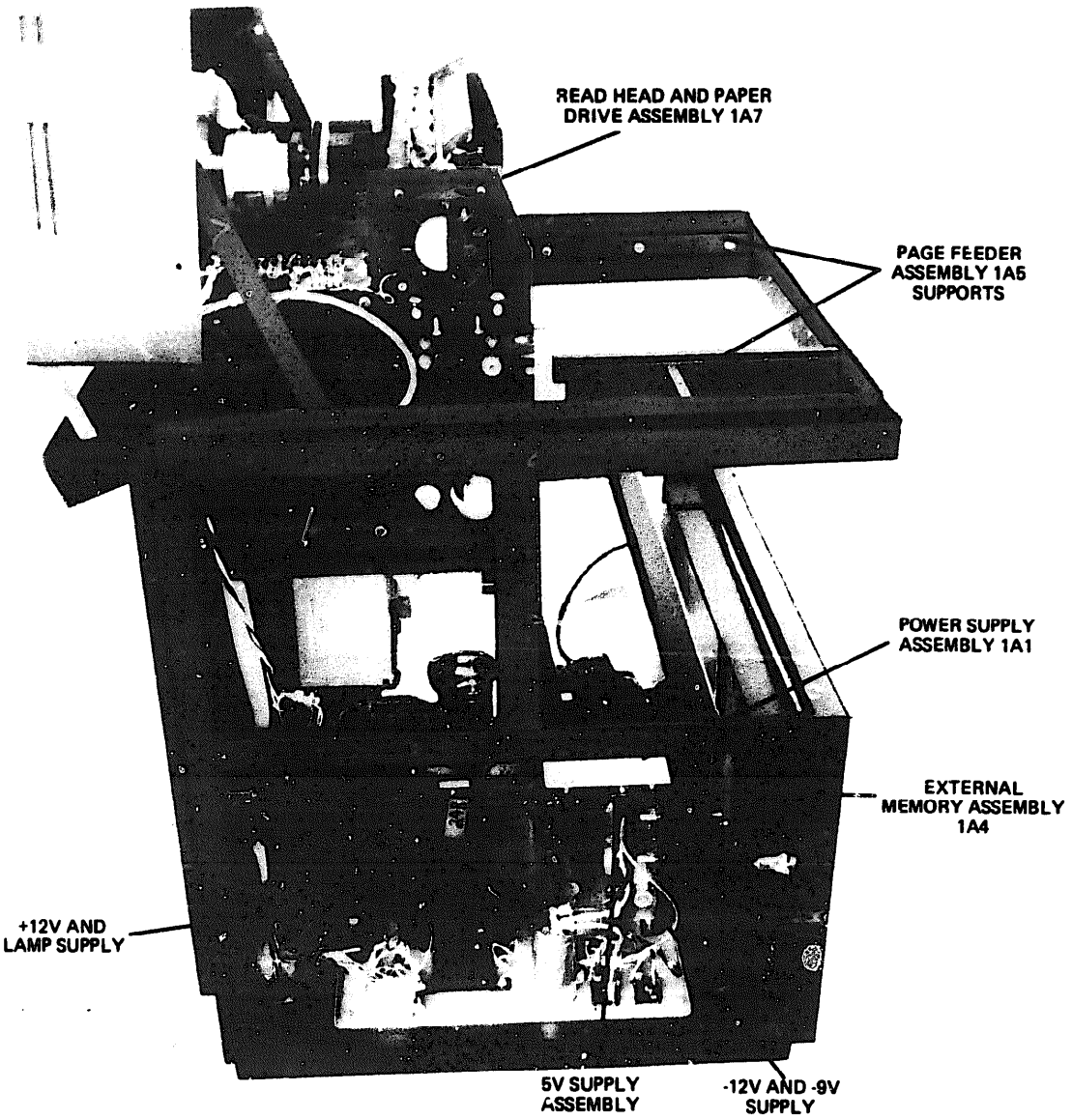

Figure A-36. ALPHA Left Side Interior View

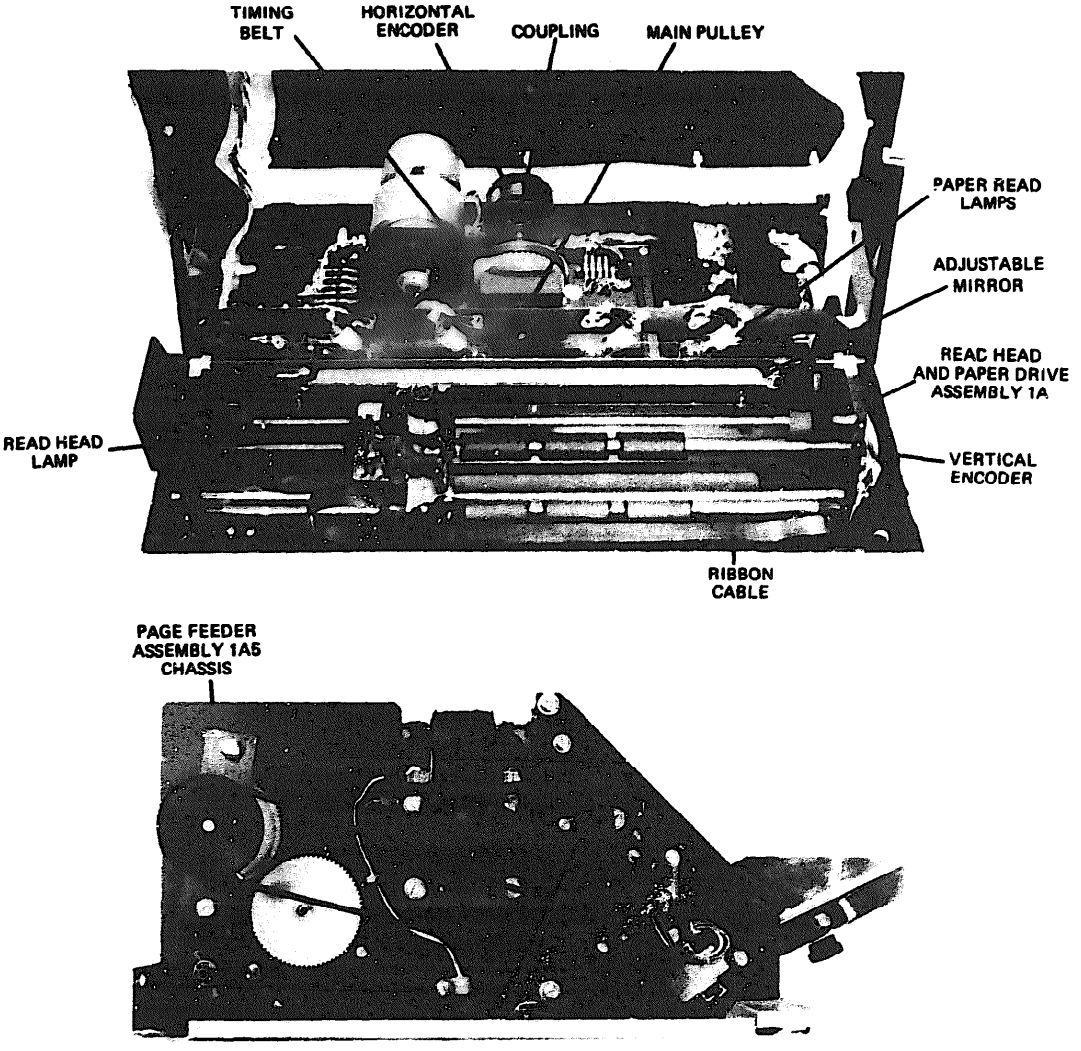

Figure A-37. ALPHA Paper Control Assemblies

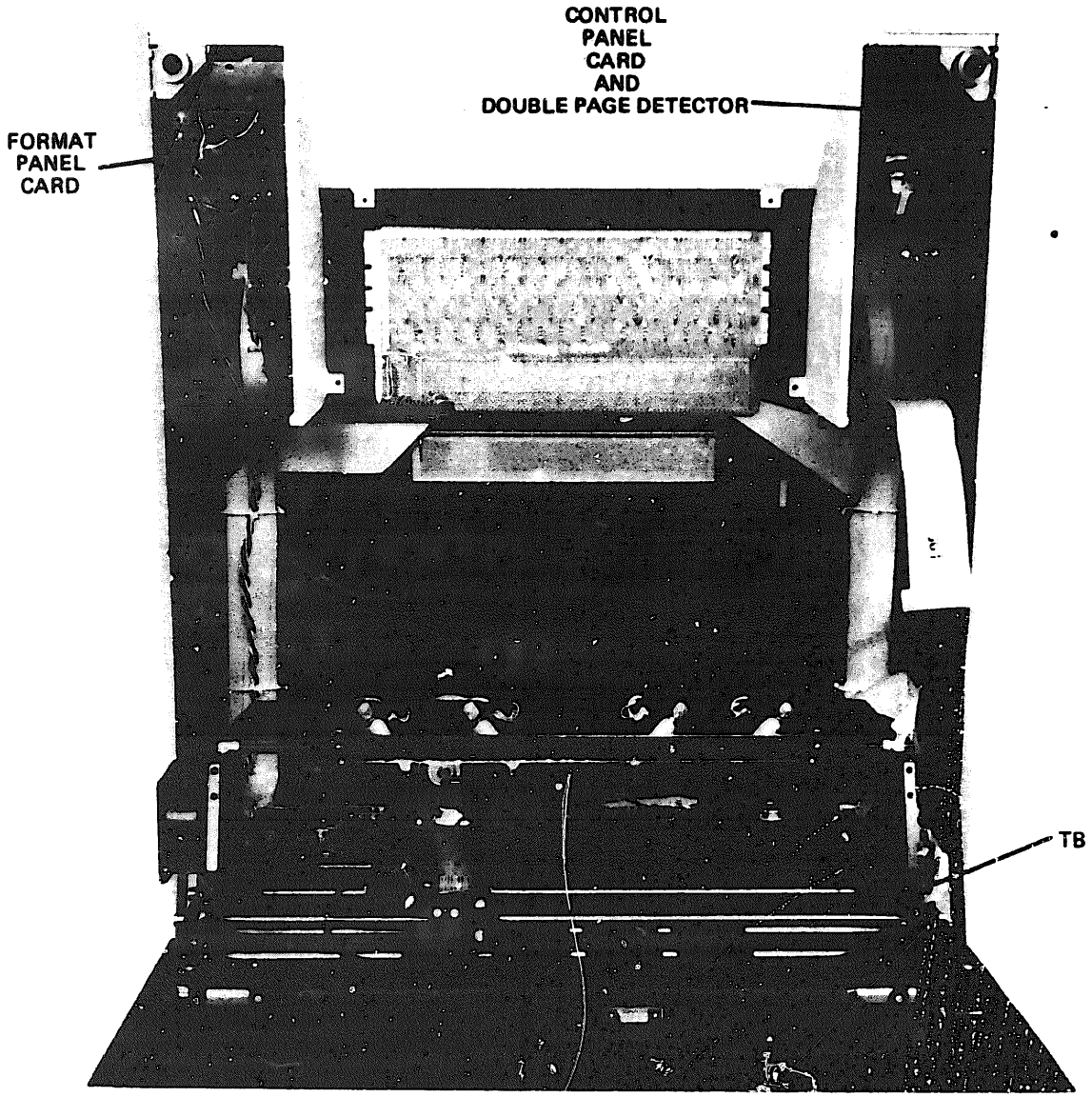

Figure A-38. ALPHA Upper Assemblies, Interior View

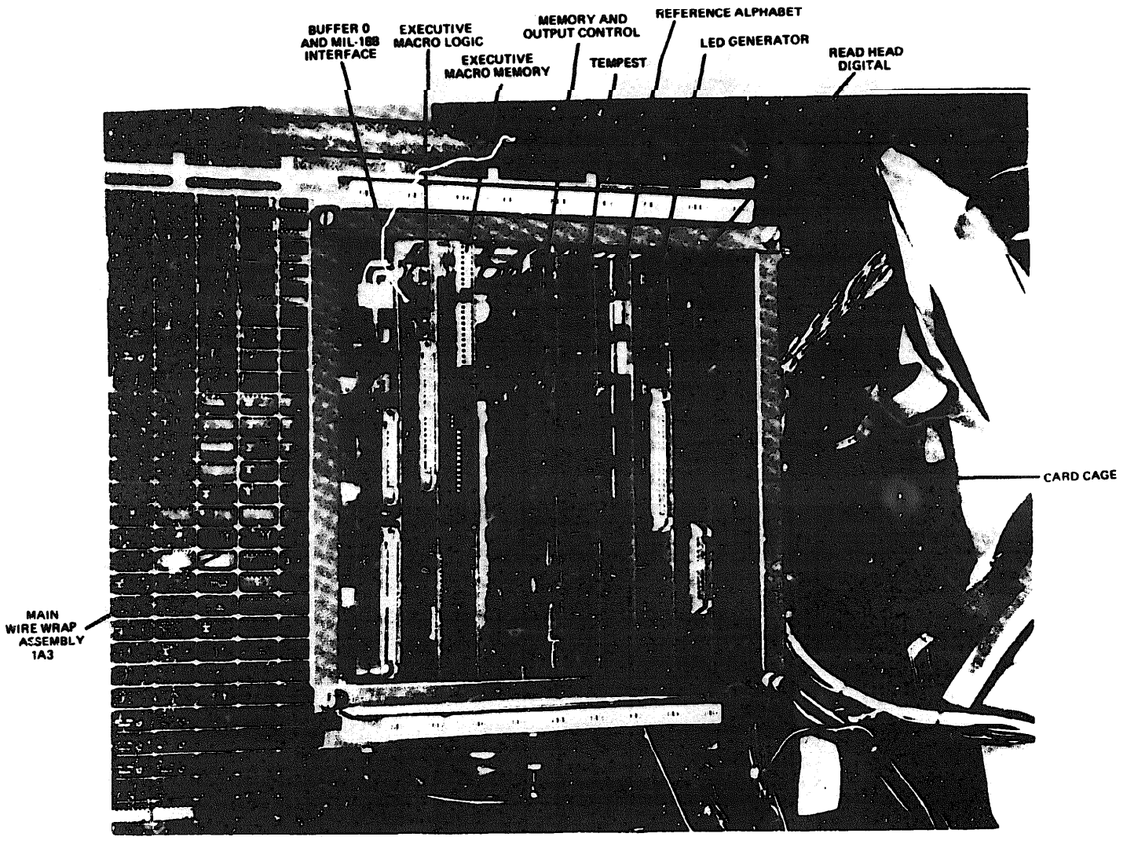

Figure A-39. Main Wire Wrap, Assembly 1A3

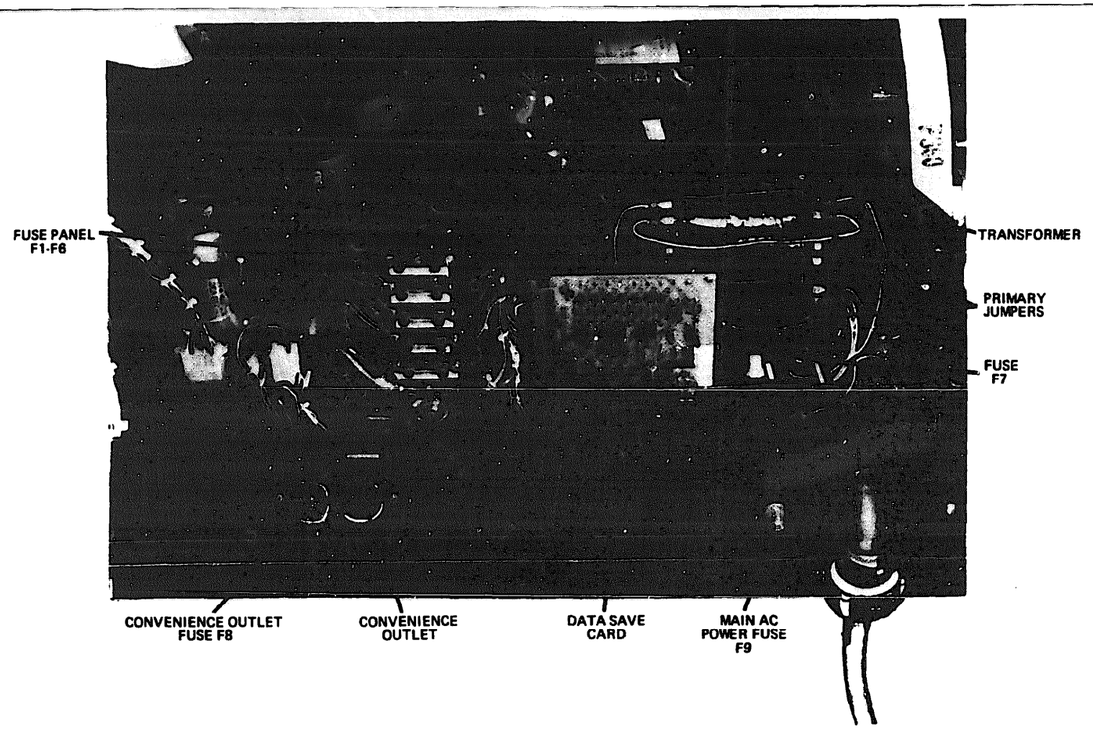

Figure A-40. ALPHA Lower Assemblies, Rear Interior View

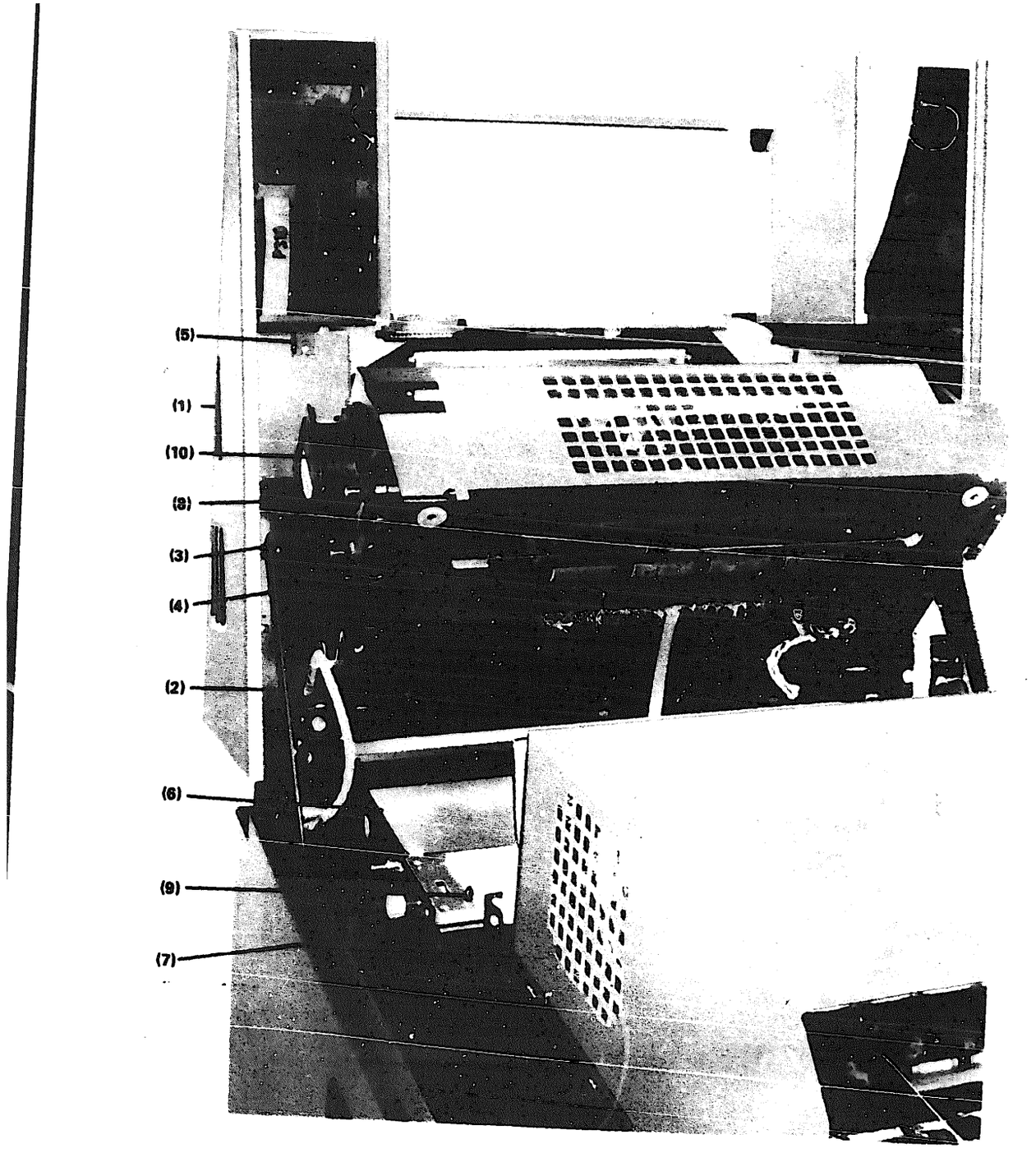

Figure A-41. Accessing the Upper Assemblies.

END

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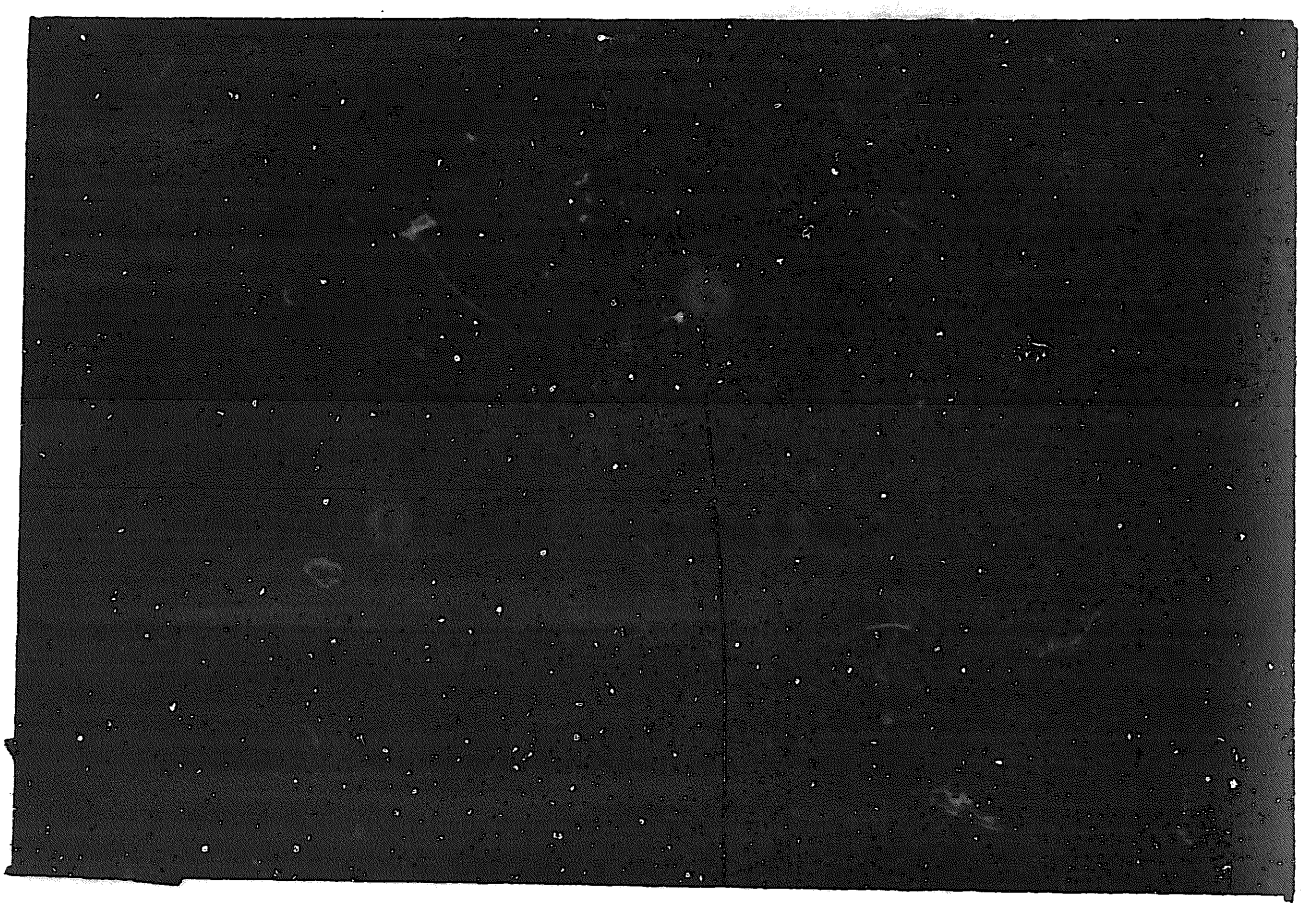
DATE



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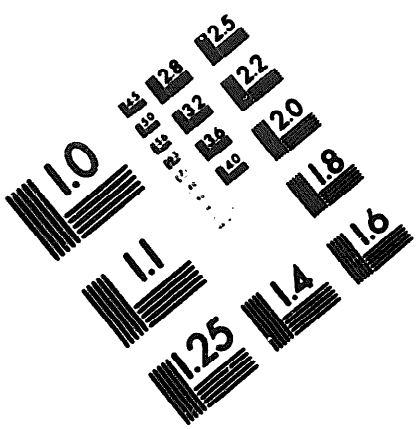
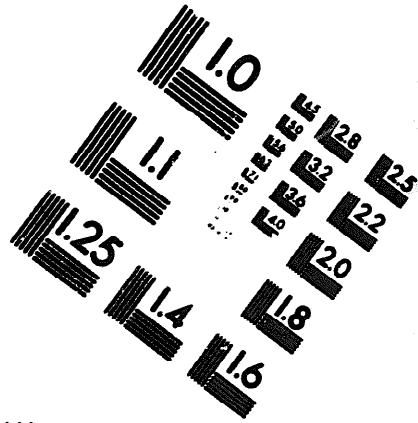
MICROFORM
TEST TARGET





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1.5 mm (e= 1.09 mm)

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2.0 mm (e= 1.37 mm)

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2.5 mm (e= 1.77 mm)

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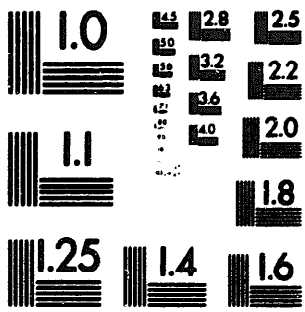

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1.5 mm (e= 1.09 mm)

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2.0 mm (e= 1.37 mm)

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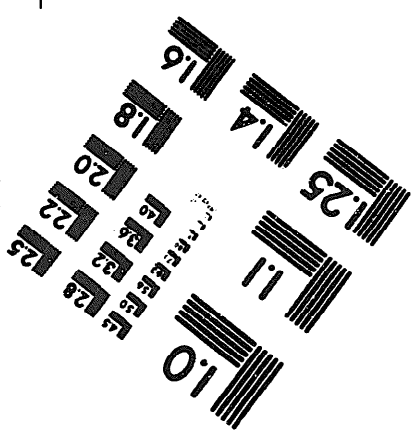

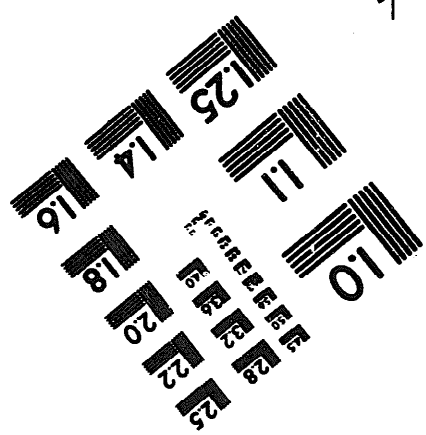

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